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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	13
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 8x8b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	20-DIP (0.300", 7.62mm)
Supplier Device Package	20-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c782-i-p

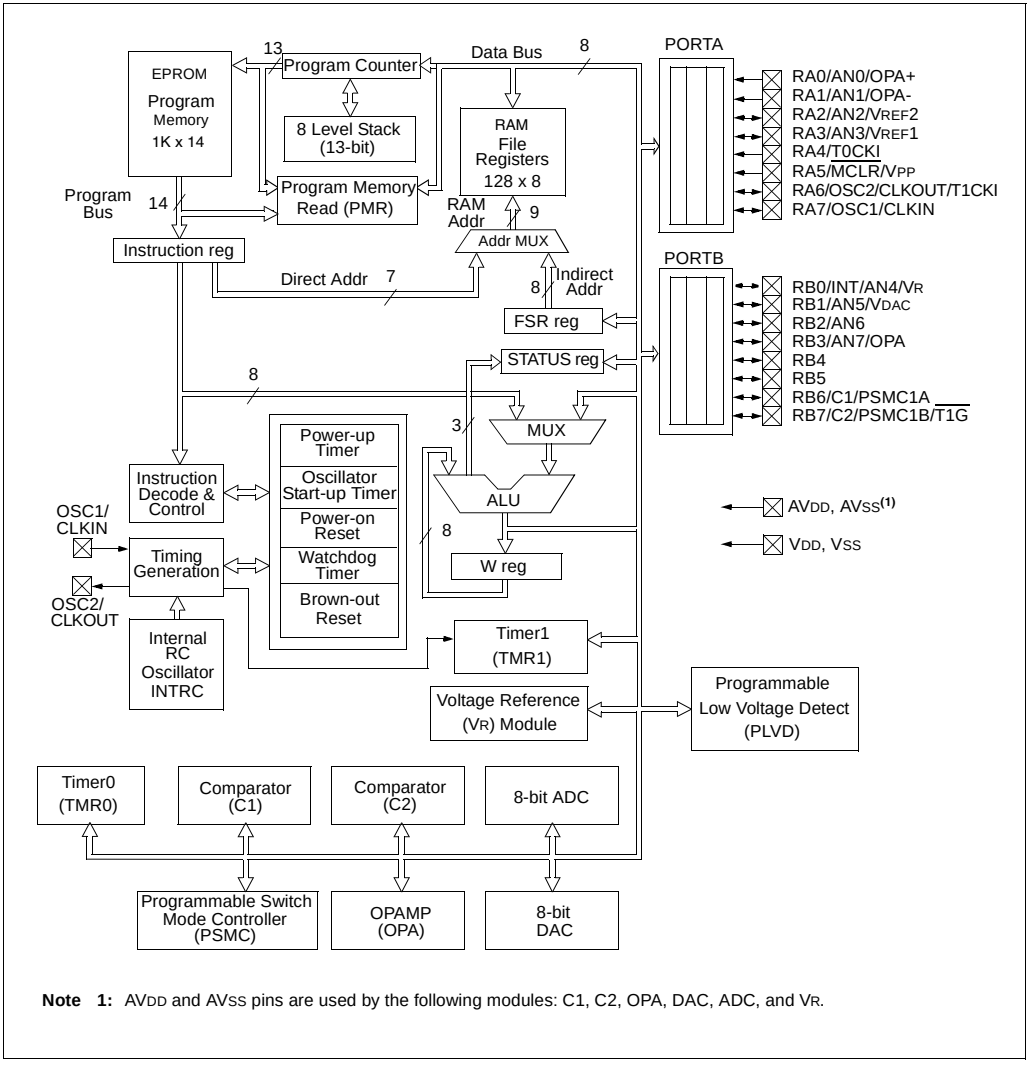
1.0 DEVICE OVERVIEW

This document contains device-specific information. Additional information may be found in the PIC Mid-Range Reference Manual (DS33023), which may be obtained from your local Microchip Sales Representative or downloaded from the Microchip website. The Reference manual should be considered a complementary document to this data sheet. The Reference manual is highly recommended reading for a better understanding of the device architecture and operation of the peripheral modules.

This data sheet covers two devices: PIC16C781 and PIC16C782. Both devices come in a variety of 20-pin packages.

The following figures are block diagrams of the PIC16C781 and the PIC16C782.

FIGURE 1-1: PIC16C781 BLOCK DIAGRAM



Note 1: AVDD and AVSS pins are used by the following modules: C1, C2, OPA, DAC, ADC, and VR.

TABLE 2-1: PIC16C781/782 SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

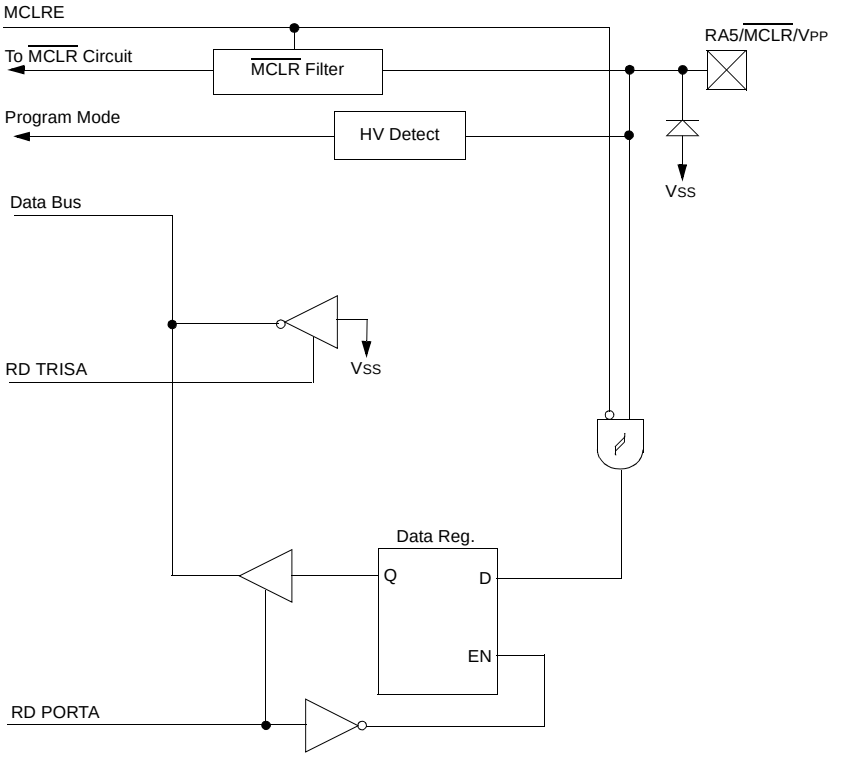
Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Details on Page:
Bank 3											
180h(2)	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								0000 0000	23
181h	OPTION_REG	$\overline{RBPU}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	18
182h(2)	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	23
183h(2)	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	17
184h(2)	FSR	Indirect Data Memory Address Pointer								xxxx xxxx	23
185h	—	Unimplemented								—	—
186h	TRISB	PORTB Data Direction Register								1111 1111	35
187h	—	Unimplemented								—	—
188h	—	Unimplemented								—	—
189h	—	Unimplemented								—	—
18Ah(1,2)	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter					---0 0000	23
18Bh(2)	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	19
18Ch	PMCON1	Reserved	—	—	—	—	—	—	RD	1--- ---0	47
18Dh	—	Unimplemented								—	—
18Eh	—	Unimplemented								—	—
18Fh	—	Unimplemented								—	—
190h	—	Unimplemented								—	—
191h	—	Unimplemented								—	—
192h	—	Unimplemented								—	—
193h	—	Unimplemented								—	—
194h	—	Unimplemented								—	—
195h	—	Unimplemented								—	—
196h	—	Unimplemented								—	—
197h	—	Unimplemented								—	—
198h	—	Unimplemented								—	—
199h	—	Unimplemented								—	—
19Ah	—	Unimplemented								—	—
19Bh	—	Unimplemented								—	—
19Ch	—	Unimplemented								—	—
19Dh	—	Unimplemented								—	—
19Eh	—	Unimplemented								—	—
19Fh	—	Unimplemented								—	—

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0'.
Shaded locations are unimplemented, read as '0'.

Note 1: The upper byte of the program counter is not directly accessible. PCLATH is a holding register for the PC<12:8> whose contents are transferred to the upper byte of the program counter. See Section 2.9 for more detail.

2: These registers can be addressed from any bank.

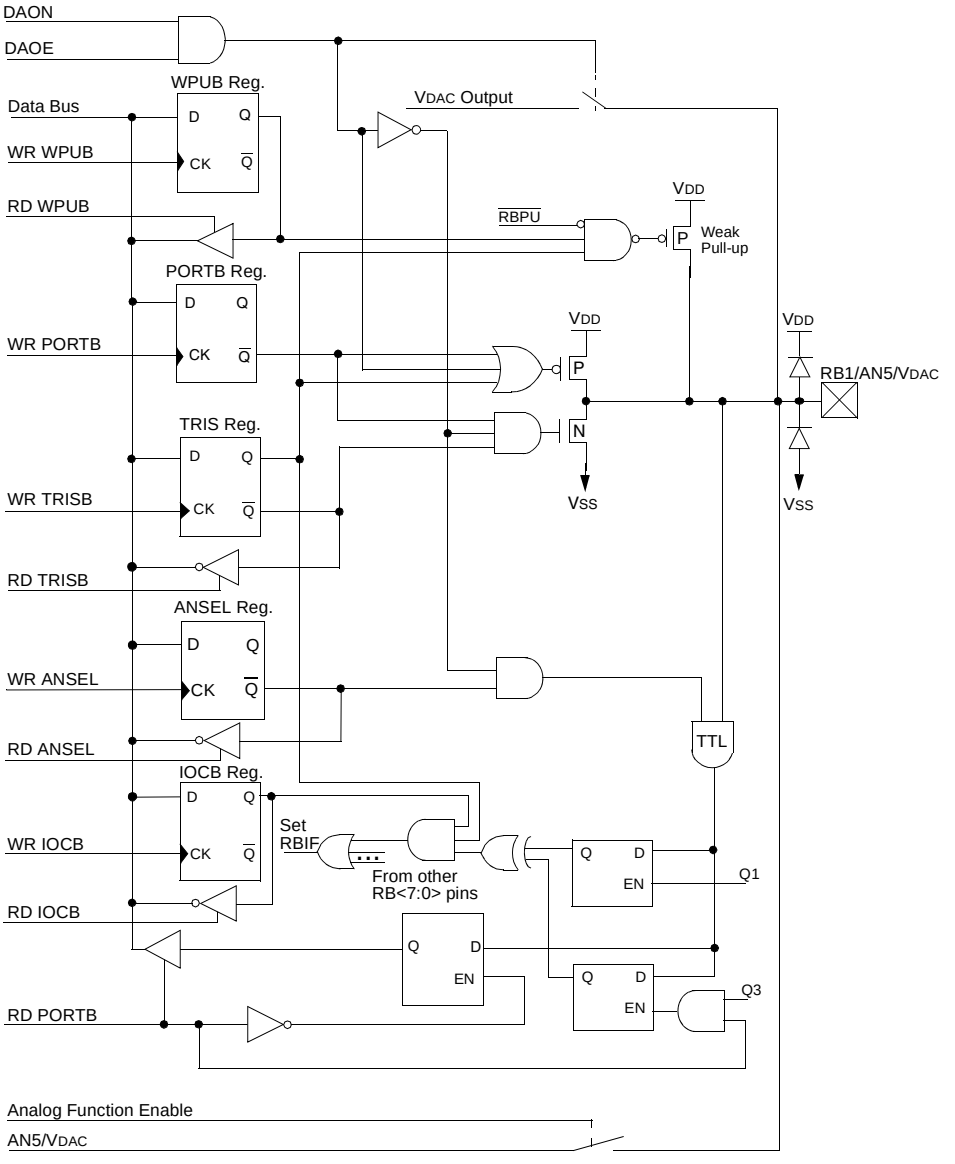
FIGURE 3-6: BLOCK DIAGRAM OF RA5/$\overline{\text{MCLR}}$/VPP PIN



MCLRE(1)	TRISA<5>	FUNCTION	PORTA<5> READ
Internal	x	Digital In	Pin
External	x	$\overline{\text{MCLR}}$	0

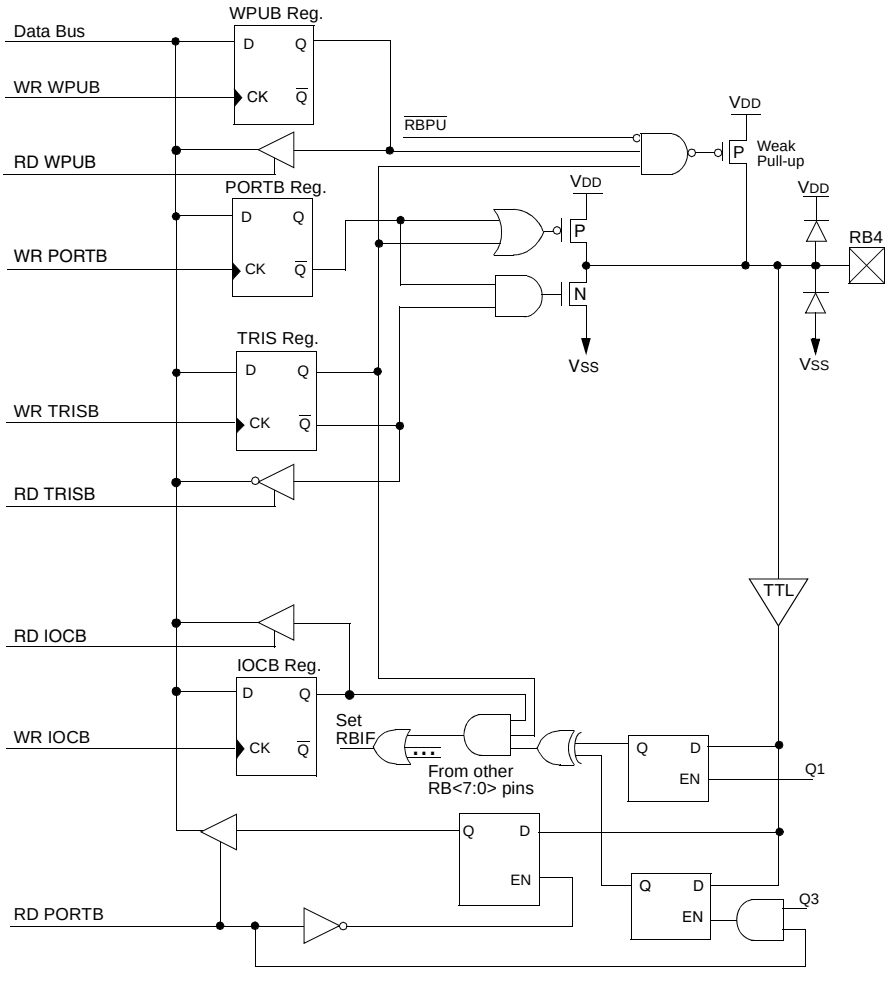
Note 1: See Configuration Word <5>, Register 14-1.

FIGURE 3-10: BLOCK DIAGRAM OF RB1/AN5/VDAC PIN



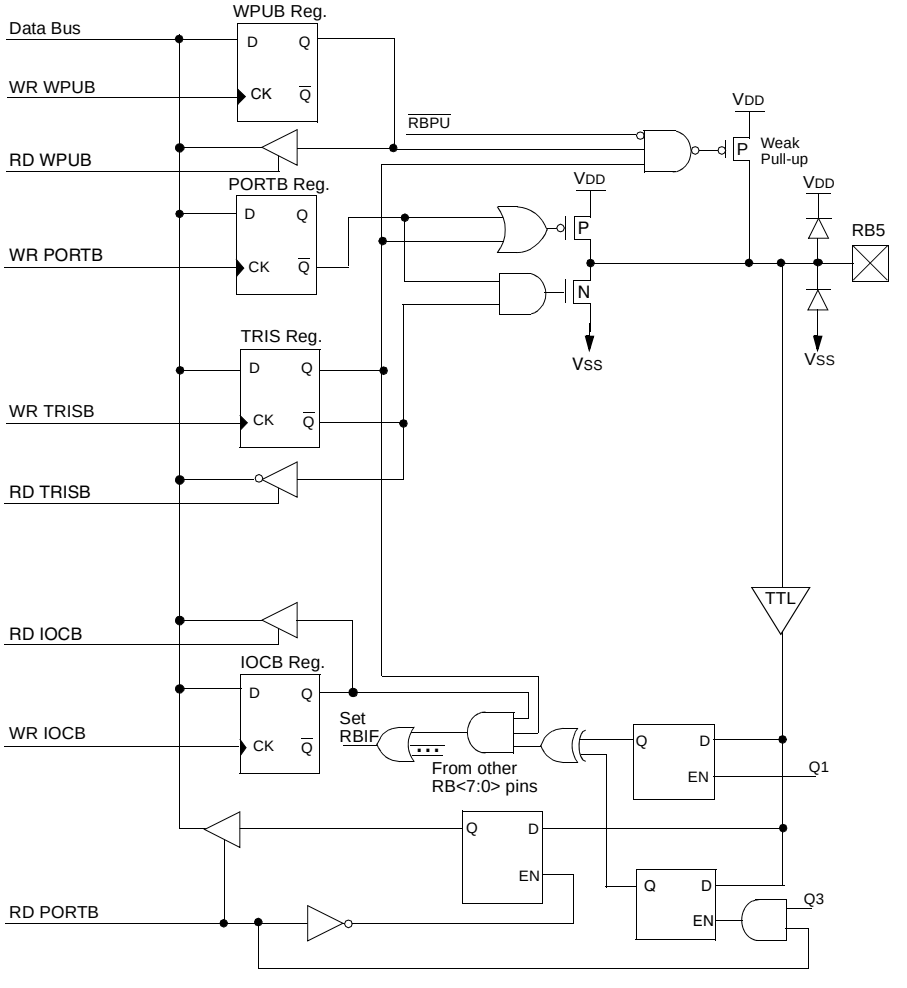
DAON & DAOE	ANSEL<5>	TRISB<1>	FUNCTION	PORTB<1> READ
0	0	1	Digital In	Pin
0	0	0	Digital Out	Pin
0	1	x	Analog In	0
1	x	x	Analog Out	0

FIGURE 3-13: BLOCK DIAGRAM OF RB4 PIN



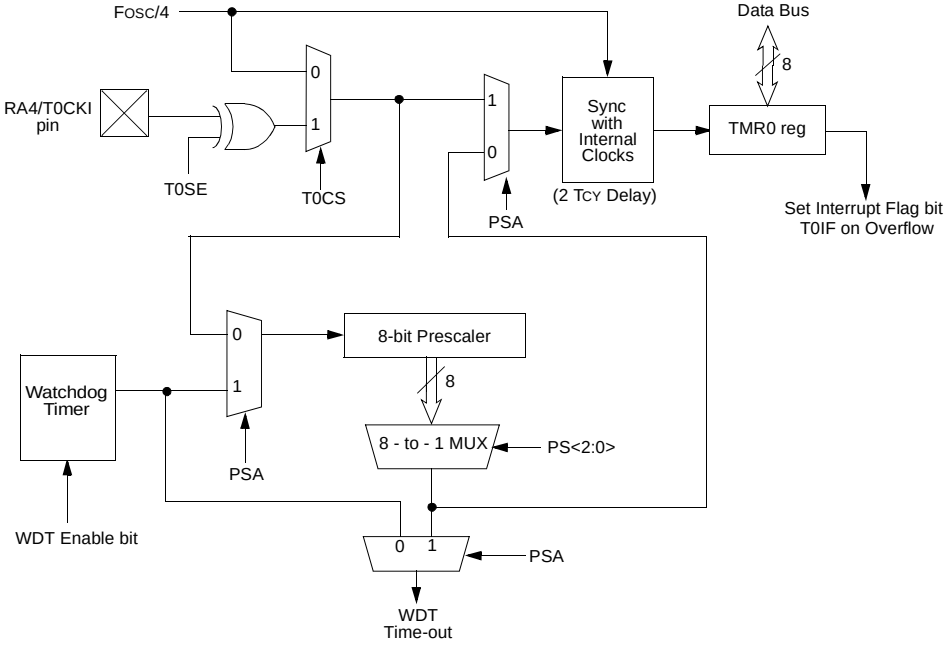
TRISB<4>	FUNCTION	PORTB<4> READ
0	Digital Out	Pin
1	Digital In	Pin

FIGURE 3-14: BLOCK DIAGRAM OF RB5 PIN



TRISB<5>	FUNCTION	PORTB<5> READ
0	Digital Out	Pin
1	Digital In	Pin

FIGURE 5-2: BLOCK DIAGRAM OF THE TIMER0/WDT PRESCALER



Note: T0CS, T0SE, PSA, PS<2:0> are (OPTION_REG<5:0>).

TABLE 5-1: REGISTERS ASSOCIATED WITH TIMER0

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other RESETS
01h,101h	TMR0	Timer0 Register								xxxx xxxx	uuuu uuuu
0Bh,8Bh, 10Bh,18Bh	INTCON	GIE	ADIF	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
81h,181h	OPTION_REG	$\overline{\text{RBPU}}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by Timer0.

7.0 VOLTAGE REFERENCE MODULE (VR)

The Voltage Reference module provides an on-chip nominal 3.072V reference voltage for the following:

- ADC converter
- DAC converter
- VR output on the RB0/INT/AN4/VR pin

The source for the reference voltage comes from a bandgap reference.

The control register for this module is the REFCON register shown in Register 7-1.

Note 1: If the VR module is to be used by the DAC, ADC, or VR output:, the VR module must be enabled using VREN (REFCON<3>).

2: When VREN = 1 and VROE = 1, the output driver for RB0/INT/AN4/VR will be driven tri-state and the analog driver for the VR output will be enabled. A read of RB0 will return a '0'.

Setting the VREN flag (REFCON<3>), enables the module. Following initial start-up, the module should be allowed to stabilize for best accuracy. See Section 17.0 for information concerning stabilization times and conditions.

To route the reference voltage to the external RB0/INT/AN4/VR pin, the VROE flag (REFCON<2>) must be set.

7.1 Effects of RESET

A device RESET clears the REFCON register, disabling the voltage reference.

7.2 Registers Associated with VR

A summary of the registers associated with VR is shown in Table 7-1.

REGISTER 7-1: VOLTAGE REFERENCE CONTROL REGISTER (REFCON: 9Bh)

U-0	U-0	U-0	U-0	R/W-0	R/W-0	U-0	U-0
—	—	—	—	VREN	VROE	—	—
bit 7							bit 0

bit 7-4 **Unimplemented:** Read as '0'

bit 3 **VREN:** Voltage Reference Enable bit (VR = 3.072V nominal)
1 = VR reference is enabled
0 = VR reference is disabled

bit 2 **VROE:** Voltage Reference Output Enable bit
If VREN = 1:
1 = Enabled, VR voltage reference is output on RB0
0 = Voltage reference is not available externally
If VREN = 0:
This bit is ignored

bit 1-0 **Unimplemented:** Read as '0'

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

TABLE 7-1: SUMMARY OF REGISTERS ASSOCIATED WITH VR

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other RESETS
09Bh	REFCON	—	—	—	—	VREN	VROE	—	—	---- 00--	---- 00--

8.0 PROGRAMMABLE LOW VOLTAGE DETECT MODULE (PLVD)

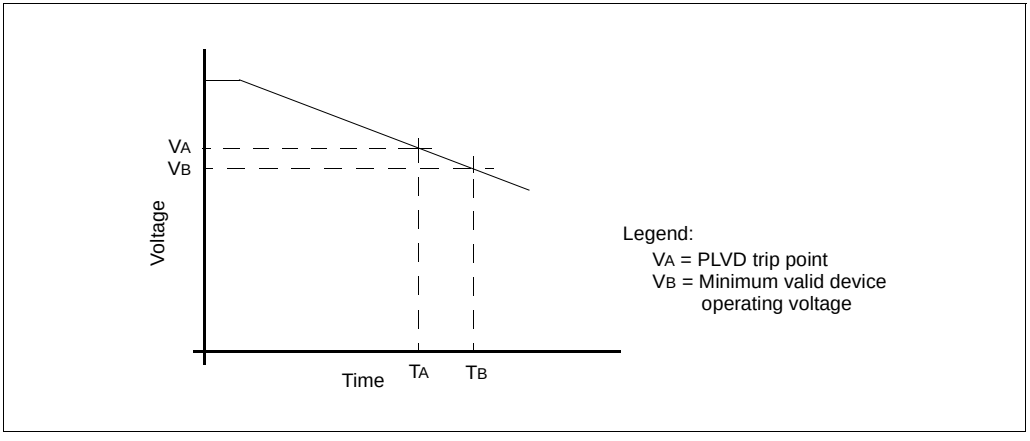
The PLVD module monitors the VDD power supply of the microcontroller and signals the microcontroller whenever VDD drops below its trip voltage. The signal acts as an 'early warning' of power-down, allowing the microcontroller to finish any critical 'housekeeping' tasks prior to completing power-down.

Figure 8-1 demonstrates a potential application of the PLVD module (typical battery operation). At time TA, the VDD supply voltage (VA) has fallen below the PLVD reference voltage. The PLVD voltage comparator then sets the LVDIF bit (PIR<7>), indicating a low voltage condition. The time between TA and TB is then available to the microcontroller for completing a 'graceful' power-down before VDD falls below VB.

Figure 8-2 is a simplified block diagram for the PLVD module, showing the VDD resistor ladder, control register, and voltage comparator.

Note:	For low power applications, current drain can be minimized by enabling the module only during regular polled testing. When not in use, the module is disabled by clearing the LVDEN bit (LVDCON<4>), which also powers down the resistor ladder between VDD and Vss.

FIGURE 8-1: TYPICAL LOW VOLTAGE DETECT APPLICATION



8.1 Control Register

The PLVD module is controlled via the LVDCON register shown in Register 8-1.

To enable the module for testing, the LVDEN bit (LVDCON<4>) must be set. This will enable the on-board voltage reference and connect the resistor ladder between VDD and Vss. Clearing LVDEN will disable the module and disconnect the resistor ladder from Vss.

The trip voltage is set by programming the LVDL<3:0> bit (LVDCON<3.0>). The voltages available are listed in Register 8-1. Note that voltages below 2.5V and above 4.75V are not available and should not be used.

The BGST bit (LVDCON<5>) is a status bit indicating that the internal reference voltage bandgap has stabilized. No test should be performed until this bit is set.

The low voltage output flag for the PLVD module is the LVDIF bit (PIR1<6>).

9.4.1 FASTER CONVERSION/LOWER RESOLUTION TRADE-OFF

Not all applications require a result having 8-bits of resolution. Some may instead, require a faster conversion time. The ADC module allows users to make a trade-off of conversion speed for resolution. Regardless of the resolution required, the acquisition time is the same. To speed up the conversion, the clock source of the ADC module may be switched during the conversion, so that the TAD time violates the minimum specified time (see the applicable Electrical Specification). Once the switch is made, all the following ADC result bits are invalid (see ADC Conversion Timing in the Electrical Specifications section). The clock source may only be switched between the three oscillator options (it cannot be switched from/to RC). The equation to determine the time before the oscillator must be switched for a desired resolution is as follows:

Conversion time = $2T_{AD} + N \bullet T_{AD} + (8 - N)(2T_{OSC})$

Where: N = number of bits of resolution required.

Since the TAD is based on the device oscillator, the user must employ some method (such as a timer, software loop, etc.) to determine when the ADC oscillator must be changed.

9.5 ADC Operation During SLEEP

The ADC module can operate during SLEEP mode. This requires that the ADC clock source be set to RC (ADCS1:ADCS0 = 11). When the RC clock source is selected, the ADC module waits one instruction cycle before starting the conversion. This allows the SLEEP instruction to be executed, which eliminates all digital switching noise from the conversion. When the conversion is completed the GO/DONE bit is cleared, and the result is loaded into the ADRES register. If the ADC interrupt is enabled, the device awakens from SLEEP. If the ADC interrupt is not enabled, the ADC module is turned off, although the ADON bit remains set.

When the ADC clock source is another clock option (not RC), a SLEEP instruction causes the present conversion to be aborted and the ADC module to be turned off. The ADON bit remains set.

Turning off the ADC places the ADC module in its lowest current consumption state.

Note:	For the ADC module to operate in SLEEP, the A/D clock source must be set to RC (ADCS1:ADCS0 = 11). To perform an ADC conversion in SLEEP, ensure the SLEEP instruction immediately follows the instruction that sets the GO/DONE bit.

9.6 ADC Accuracy/Error

The absolute accuracy (absolute error) specified for the ADC converter includes the sum of all contributions for:

- Offset error
- Gain error
- Quantization error
- Integral non-linearity error
- Differential non-linearity error
- Monotonicity

The **absolute error** is defined as the maximum deviation from an actual transition versus an ideal transition for any code. The absolute error of the ADC converter is specified as < ±1 LSb for $ADC_{REF} = V_{DD}$ (over the device's specified operating range). However, the accuracy of the ADC converter degrades as V_{DD} diverges from V_{REF}.

For a given range of analog inputs, the output digital code will be the same. This is due to the quantization of the analog input to a digital code. **Quantization error** is typically ± 1/2 LSb and is inherent in the analog to digital conversion process. The only way to reduce quantization error is to use an ADC with greater resolution of the ADC converter.

Offset error measures the first actual transition of a code versus the first ideal transition of a code. Offset error shifts the entire transfer function. Offset error can be calibrated out of a system, or introduced into a system, through the interaction of the total leakage current and source impedance at the analog input.

Gain error measures the maximum deviation of the last actual transition and the last ideal transition adjusted for offset error. This error appears as a change in slope of the transfer function. The difference in gain error to full scale error is that full scale does not take offset error into account. Gain error can be calibrated out in software.

Linearity error refers to the uniformity of the code changes. Linearity errors cannot be calibrated out of the system. **Integral non-linearity error** measures the actual code transition versus the ideal code transition, adjusted by the gain error for each code. **Differential non-linearity** measures the maximum actual code width versus the ideal code width. This measure is unadjusted.

If the linearity errors are very large, the ADC may become **non-monotonic**. This occurs when the digital values for one or more input voltages are less than the value for a lower input voltage.

FIGURE 9-4: FLOW CHART OF ADC OPERATION

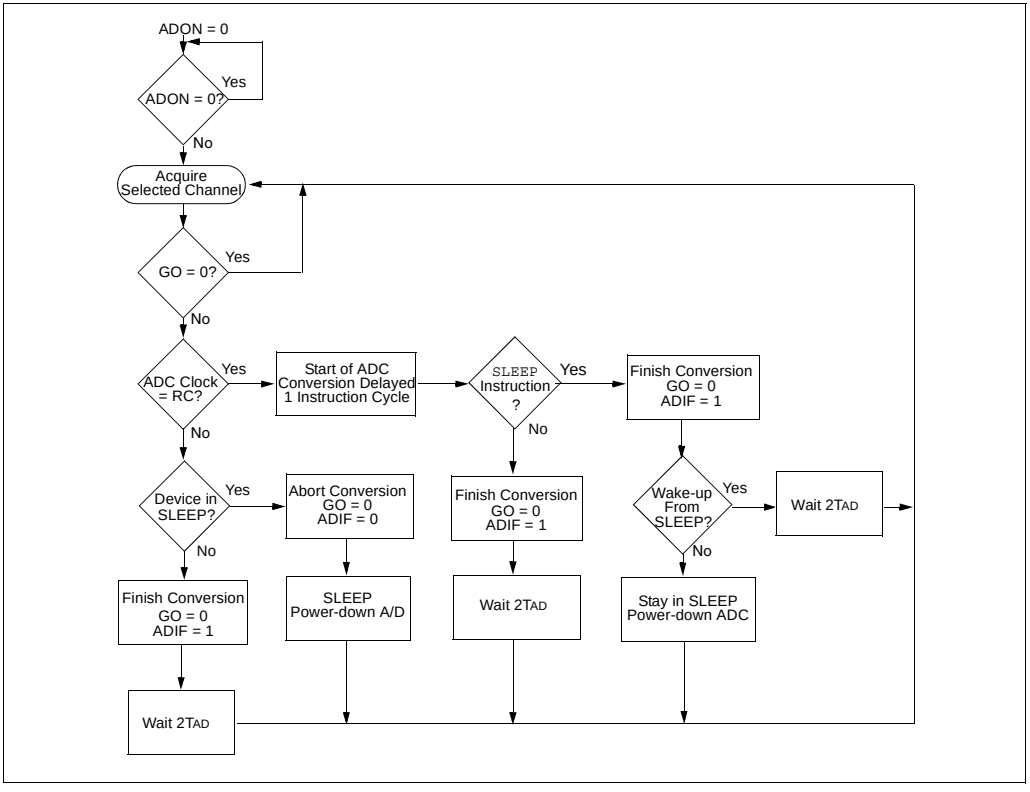


TABLE 9-2: REGISTERS/BITS ASSOCIATED WITH ADC, PIC16C781/782

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other RESETS
0Bh	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
8Ch	PIE1	LVDIE	ADIE	C2IE	C1IE	—	—	—	TMR1IE	0000 ---0	0000 ---0
0Ch	PIR1	LVDIF	ADIF	C2IF	C1IF	—	—	—	TMR1IF	0000 ---0	0000 ---0
1Eh	ADRES	ADC Result Register								xxxx xxxx	uuuu uuuu
1Fh	ADCON0	ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/$\overline{\text{DONE}}$	CHS3	ADON	0000 0000	0000 0000
9Fh	ADCON1	—	—	VCFG1	VCFG0	—	—	—	—	--00 ----	--00 ----
05h	PORTA	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	xxxx 0000	uuuu 0000
06h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx 0000	uuuu 0000
9Dh	ANSEL	Analog Channel Select								1111 1111	1111 1111

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used for ADC conversion.

13.3.2 EXAMPLE BUCK LC SWITCHING POWER SUPPLY

In this example, the PSMC controls the buck configuration switching power supply in Figure 13-6.

The PSMC is configured as a typical PWM, current mode, switching power supply controller. The inner current feedback loops consist of:

- PSMC
- 2 MOSFET drivers
- Power MOSFETs Q1 and Q2
- Inductors L1 and L2
- Current transformer
- Comparator C1/C2

The outer voltage feedback loop consists of:

- Diodes D1, D2, D3, and D4
- CMAIN
- OPAMP feedback filter
- DAC reference

The circuit uses two feedback loops, an inner current control loop, and an outer voltage loop. The inner loop is further divided into two channels, Q1/L1, and Q2/L2. The PSMC operates a PWM output, alternately driving Q1 for a cycle, then driving Q2 the next. During the active phase of either output pulse, the inner loop builds up a current flow in the output's inductor, proportional to the error voltage received from the OPAMP. The current flow in the inductor begins the charging of CMAIN. When the voltage (proportional to the current flow in the inductor) exceeds the error voltage:

- The comparator resets the PSMC output
- The MOSFET is turned off
- The flyback diode forward biases
- The inductor discharges into CMAIN for the remainder of the period.

The outer voltage loop monitors the output voltage across CMAIN via R1/R2. The reference voltage from the DAC is subtracted from the feedback voltage to generate the raw error voltage. The raw error voltage is then filtered by the OPAMP and routed to Comparator C1 in the inner current loop.

In using two alternating outputs, the outputs are limited to less than 50% duty cycle. As a result, the circuit avoids the problems associated with instability at duty cycles of >50%.

For more information concerning the design of switching power supplies, refer to:

Switching Power Supply Design, by Abraham I. Pressman, published by McGraw Hill (ISBN 0-07-052236-7).

Note:	Following RESET, both the PSMC1A and PSMC1B outputs are held tri-state until the PSMC is configured. Driver circuitry for all power MOSFET transistors must have a resistor bias to turn off the transistor in the event of tri-state conditions on either output to prevent undo stress on the MOSFET's and their associated circuitry.

EXAMPLE 13-3: PERIPHERAL CONFIGURATION EXAMPLE

```
;***********************************************
;*  This code block will configure the PSMC and
;*  all additional peripherals for a motor speed
;*  control.
;*
;*  Order of configuration
;*  1.  PORTA/B I/O and analog configured
;*  2.  DAC enabled, configured, and preset
;*  3.  Op Amp enabled and configured
;*  4.  Comparator C1 enabled and configured
;*  5.  PSMC configured
;*  6.  PSMC enabled
;*
;***********************************************
;*  This code block will configure all analog ports.

    BANKSEL     TRISA               ; Select Bank 1
    MOVLW       B'01000011'
    MOVWF       TRISA               ; Set RA0,1 & 6 as inputs
    MOVLW       B'00001100'
    MOVWF       TRISB               ; Set RB2 & 3 as inputs
    MOVLW       B'11000011'
    MOVWF       ANSEL               ; Set AN0,1,6,& 7 as analog

;***********************************************
;*  This code block will configure the DAC for VR as
;*  DACREF, and no output.

    BANKSEL     REFCON
    BSF         REFCON, VREN        ; Enable VR
    BANKSEL     DACON0              ; Select Bank 2

    CLRF        DAC                 ; Set DAC to safe value
    MOVLW       B'10000010'         ; Enable DAC, no output
    MOVWF       DACON0              ;  and set DACREF = VR

    MOVLW       OUTPUT_VALUE
    MOVWF       DAC                 ; Set DAC output level

;***********************************************
;*  This code block will configure the OPA module
;*  as an Op Amp, with a 2 MHz GBWP

    MOVLW       B'10000001'         ; Set Op Amp mode and
    MOVWF       OPACON              ;  2 MHz GBWP

;***********************************************
*   This code block will configure Comparator C1
*   for normal speed and output polarity,
*   input on AN6, and Reference from the VDAC

    MOVLW       B'10001110'         ; Set C1; no ext out, norm
    MOVWF       CM1CON0             ;  speed & pol, VDAC, AN6

;***********************************************
;*  This code block will configure the PSMC module
;*  for PWM, Fosc/16, Single input, Single output
;*  Non-inverting out, DC min = 0%, DC max = 94%

    MOVLW       B'11001100'
    MOVWF       PSMCCON0            ; Set DCmin 0, DCmax 94, Fosc/16
    MOVLW       B'00000010'
    MOVWF       PSMCCON1            ; Set PWM, Sngl in/out, noninvert
    BSF         PSMCCON1,SMCON      ; Enable PSMC
```

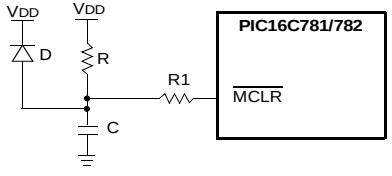
14.4 Power-on Reset (POR)

A Power-on Reset pulse is generated on-chip when a VDD rise is detected (in the range of 1.5V - 2.1V). To take advantage of the POR, simply enable the internal MCLR feature. This eliminates external RC components usually needed to create a Power-on Reset. A maximum rise time for VDD is specified. See Section 17.0 for details. For a slow rise time, see Figure 14-5.

Two delay timers (PWRT on OST) are provided, which hold the device in RESET after a POR (dependent upon device configuration), so that all operational parameters have been met prior to releasing the device to resume/begin normal operation.

When the device starts normal operation (exits the RESET condition), device operating parameters (i.e., voltage, frequency, temperature,...) must be met to ensure operation. If these conditions are not met, the device must be held in RESET until the operating conditions are met. Brown-out Reset may be used to meet the start-up conditions, or if necessary an external POR circuit may be implemented to delay end of RESET for as long as needed.

FIGURE 14-5: EXTERNAL POWER-ON RESET CIRCUIT (FOR SLOW VDD RAMP)



Note 1: External Power-on Reset circuit is required only if VDD power-up slope is too slow. The diode D helps discharge the capacitor quickly when VDD powers down.

2: R < 40 kΩ is recommended to make sure that voltage drop across R does not violate the device's electrical specification.

3: R1 = 100Ω to 1 kΩ will limit any current flowing into MCLR from external capacitor C in the event of MCLR pin breakdown due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS).

14.5 Power-up Timer (PWRT)

The Power-up Timer provides a fixed TPWRT time-out on power-up type RESETS only. For a POR, the PWRT is invoked when the POR pulse is generated. For a BOR, the PWRT is invoked when the device exits the RESET condition (VDD rises above BOR trip point). The Power-up Timer operates on an internal RC oscillator. The chip is kept in RESET as long as the PWRT is active. The PWRT's time delay is designed to allow VDD to rise to an acceptable level. A configuration bit (PWRT) is provided to enable/disable the PWRT for the POR only. For a BOR the PWRT is always available regardless of the configuration bit setting.

The power-up time delay varies from chip-to-chip due to VDD, temperature and process variation. See DC parameters for details.

14.6 Programmable Brown-out Reset (PBOR)

The Programmable Brown-out Reset module is used to generate a RESET when the supply voltage falls below a specified trip voltage. The trip voltage is configurable to any one of four voltages provided by the BORV<1:0> configuration word bits.

Configuration bit BODEN can disable (if clear/programmed), or enable (if set), the Brown-out Reset circuitry. If VDD falls below the specified trip point for longer than TBOR (see Parameter 35, Section 17.0, Table 17-6), the brown-out situation resets the chip. A RESET may not occur if VDD falls below the trip point for less than TBOR. The chip remains in Brown-out Reset until VDD rises above VBOR. The Power-up Timer is invoked at that point and keeps the chip in RESET an additional TPWRT. If VDD drops below VBOR while the Power-up Timer is running, the chip goes back into a Brown-out Reset and the Power-up Timer is re-initialized. Once VDD rises above VBOR, the Power-up Timer again begins a TPWRT time delay.

14.7 Time-out Sequence

On power-up, the time-out sequence is as follows: First, PWRT time-out is invoked by the POR pulse. When the PWRT delay expires, the Oscillator Start-up Timer is activated. The total time-out varies depending on oscillator configuration and the status of the PWRT. For example, in RC mode with the PWRT disabled, there is no time-out at all. Figure 14-6, and Figure 14-9 depict time-out sequences on power-up.

Since the time-outs occur from the POR pulse, if MCLR is kept low long enough, the time-outs expire. Then, bringing MCLR high begins execution immediately. This is useful for testing purposes or to synchronize more than one PIC microcontroller operating in parallel.

Table 14-5 shows the RESET conditions for some special function registers.

16.4 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK object linker combines relocatable objects created by the MPASM assembler and the MPLAB C17 and MPLAB C18 C compilers. It can also link relocatable objects from pre-compiled libraries, using directives from a linker script.

The MPLIB object librarian is a librarian for pre-compiled code to be used with the MPLINK object linker. When a routine from a library is called from another source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications. The MPLIB object librarian manages the creation and modification of library files.

The MPLINK object linker features include:

- Integration with MPASM assembler and MPLAB C17 and MPLAB C18 C compilers.
- Allows all memory areas to be defined as sections to provide link-time flexibility.

The MPLIB object librarian features include:

- Easier linking because single libraries can be included instead of many smaller files.
- Helps keep code maintainable by grouping related modules together.
- Allows libraries to be created and modules to be added, listed, replaced, deleted or extracted.

16.5 MPLAB SIM Software Simulator

The MPLAB SIM software simulator allows code development in a PC-hosted environment by simulating the PIC series microcontrollers on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a file, or user-defined key press, to any of the pins. The execution can be performed in single step, execute until break, or trace mode.

The MPLAB SIM simulator fully supports symbolic debugging using the MPLAB C17 and the MPLAB C18 C compilers and the MPASM assembler. The software simulator offers the flexibility to develop and debug code outside of the laboratory environment, making it an excellent multi-project software development tool.

16.6 MPLAB ICE High Performance Universal In-Circuit Emulator with MPLAB IDE

The MPLAB ICE universal in-circuit emulator is intended to provide the product development engineer with a complete microcontroller design tool set for PIC microcontrollers (MCUs). Software control of the MPLAB ICE in-circuit emulator is provided by the MPLAB Integrated Development Environment (IDE), which allows editing, building, downloading and source debugging from a single environment.

The MPLAB ICE 2000 is a full-featured emulator system with enhanced trace, trigger and data monitoring features. Interchangeable processor modules allow the system to be easily reconfigured for emulation of different processors. The universal architecture of the MPLAB ICE in-circuit emulator allows expansion to support new PIC microcontrollers.

The MPLAB ICE in-circuit emulator system has been designed as a real-time emulation system, with advanced features that are generally found on more expensive development tools. The PC platform and Microsoft® Windows environment were chosen to best make these features available to you, the end user.

16.7 ICEPIC In-Circuit Emulator

The ICEPIC low cost, in-circuit emulator is a solution for the Microchip Technology PIC16C5X, PIC16C6X, PIC16C7X and PIC16CXXX families of 8-bit One-Time-Programmable (OTP) microcontrollers. The modular system can support different subsets of PIC16C5X or PIC16CXXX products through the use of interchangeable personality modules, or daughter boards. The emulator is capable of emulating without target application circuitry being present.

TABLE 16-1: DEVELOPMENT TOOLS FROM MICROCHIP

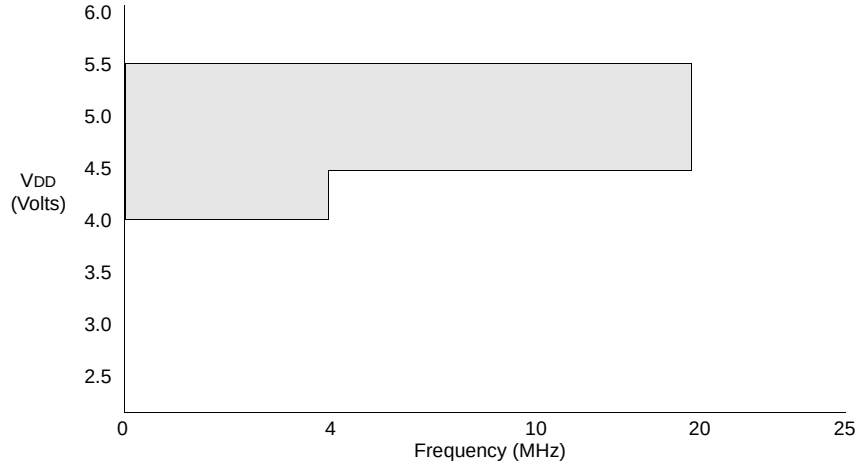
		PIC12CXXX	PIC14000	PIC16C5X	PIC16C6X	PIC16CXXX	PIC16F62X	PIC16C7X	PIC16C7XX	PIC16C8X	PIC16F8XX	PIC16C9XX	PIC17C4X	PIC17C7XX	PIC18CXX2	PIC18FXXX	24CXX/ 25CXX/ 93CXX	HCSXXX	MCRFXXX	MCP2510
Software Tools	MPLAB® Integrated Development Environment	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓				
	MPLAB® C17 C Compiler												✓	✓						
	MPLAB® C18 C Compiler														✓	✓				
	MPASM™ Assembler/ MPLINK™ Object Linker	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		
Emulators	MPLAB® ICE In-Circuit Emulator	✓	✓	✓	✓	✓	✓**	✓	✓	✓	✓	✓	✓	✓	✓	✓				
	ICEPIC™ In-Circuit Emulator	✓		✓	✓	✓		✓	✓	✓		✓								
Debugger	MPLAB® ICD In-Circuit Debugger				✓*			✓*			✓					✓				
Programmers	PICSTART® Plus Entry Level Development Programmer	✓	✓	✓	✓	✓	✓**	✓	✓	✓	✓	✓	✓	✓	✓	✓				
	PRO MATE® II Universal Device Programmer	✓	✓	✓	✓	✓	✓**	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		
Demo Boards and Eval Kits	PICDEM™ 1 Demonstration Board			✓		✓		✓†		✓			✓							
	PICDEM™ 2 Demonstration Board				✓†			✓†							✓	✓				
	PICDEM™ 3 Demonstration Board											✓								
	PICDEM™ 14A Demonstration Board		✓																	
	PICDEM™ 17 Demonstration Board													✓						
	KEELOQ® Evaluation Kit																	✓		
	KEELOQ® Transponder Kit																	✓		
	microID™ Programmer's Kit																		✓	
	125 kHz microID™ Developer's Kit																		✓	
	125 kHz Anticollision microID™ Developer's Kit																		✓	
	13.56 MHz Anticollision microID™ Developer's Kit																		✓	
	MCP2510 CAN Developer's Kit																			✓

* Contact the Microchip Technology Inc. web site at www.microchip.com for information on how to use the MPLAB® ICD In-Circuit Debugger (DV164001) with PIC16C62, 63, 64, 65, 72, 73, 74, 76, 77.

** Contact Microchip Technology Inc. for availability date.

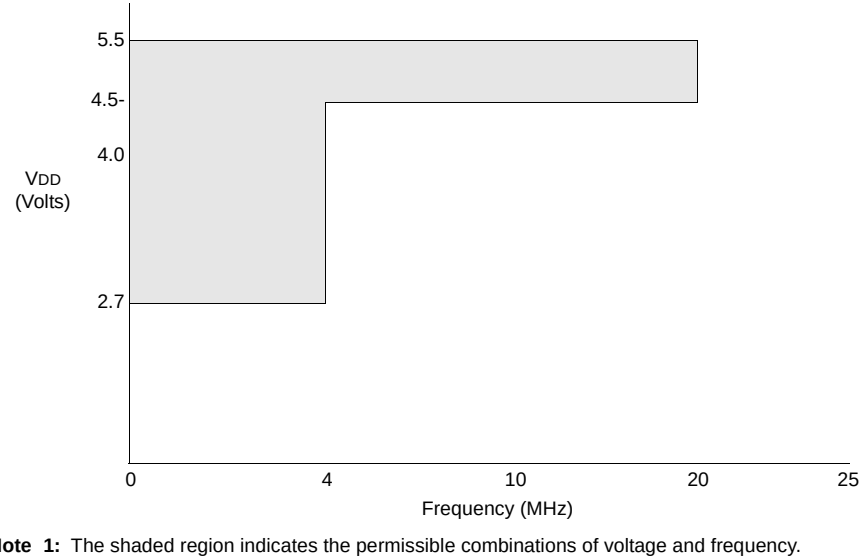
† Development tool is available on select devices.

FIGURE 17-1: PIC16C781/782 VOLTAGE-FREQUENCY GRAPH, -40°C ≤ TA ≤ +85°C



Note 1: The shaded region indicates the permissible combinations of voltage and frequency.

FIGURE 17-2: PIC16LC781/782 VOLTAGE-FREQUENCY GRAPH, -40°C ≤ TA ≤ +85°C



Note 1: The shaded region indicates the permissible combinations of voltage and frequency.

17.3 AC Characteristics: PIC16C781/782 (Industrial)

17.3.1 TIMING PARAMETER SYMBOLOGY

The timing parameter symbols have been created following one of the following formats:

1. TppS2ppS
2. TppS

T			
F	Frequency	T	Time

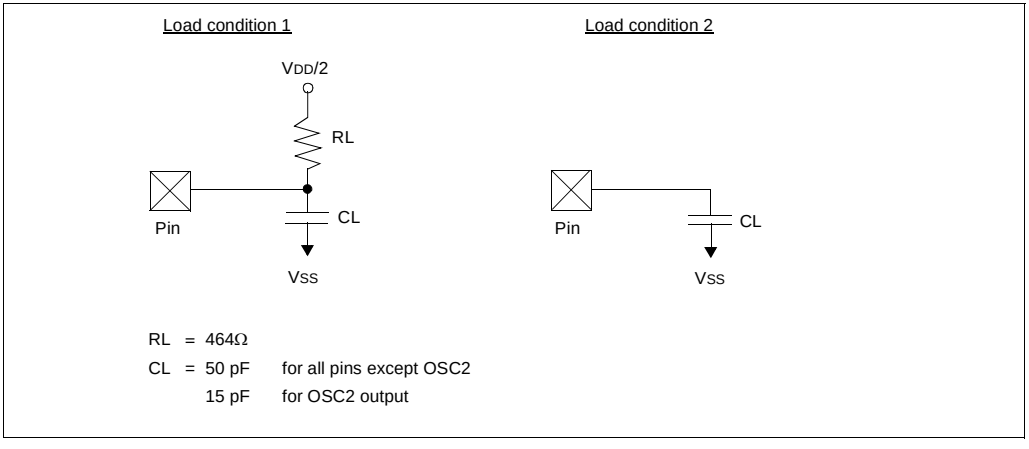
Lowercase letters (pp) and their meanings:

pp			
		osc	OSC1
ck	CLKOUT		
dt	Data in	t0	T0CKI
io	I/O port	t1	T1CKI
mc	$\overline{\text{MCLR}}$		

Uppercase letters and their meanings:

S			
F	Fall	P	Period
H	High	R	Rise
I	Invalid (Hi-impedance)	V	Valid
L	Low	Z	Hi-impedance
		High	High
		Low	Low

FIGURE 17-3: LOAD CONDITIONS



17.7 Analog Peripherals Characteristics

17.7.1 BANDGAP VOLTAGE

Bandgap voltage is used as the reference voltage in the PBOR, PLVD, Auto Calibration, and VR modules

FIGURE 17-10: BANDGAP START-UP TIME

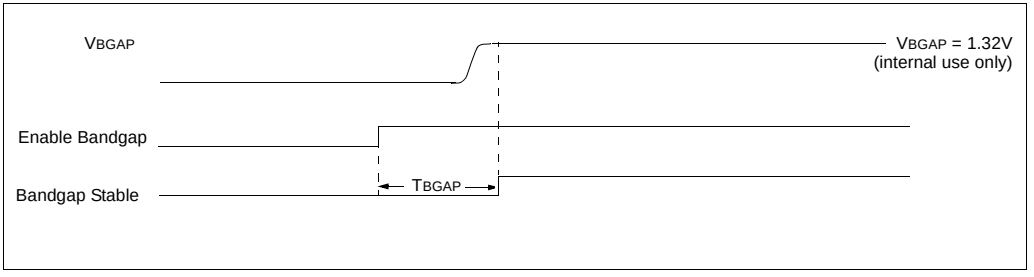


TABLE 17-14: BANDGAP START-UP TIME

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
36*	TBGAP	Bandgap start-up time	—	30	—	µs	Defined as the time between the instant that the bandgap is enabled and the moment that the bandgap reference voltage is stable.

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

17.7.2 VR MODULE

TABLE 17-15: DC CHARACTERISTICS: VR

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated): Operating temperature -40°C ≤ TA ≤ +85°C for industrial Operating voltage VDD as described in Section 17.1				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
D400	VR	Output Voltage	—	3.072	—	V	VDD ≥ 3.5V
D402*	TCVOUT	Output Voltage Temperature Coefficient	—	TBD	TBD	ppm/°C	
D404*	IVREFSO	External Load Source	—	—	5	mA	
D405*	IVREFSI	External Load Sink	—	—	-5	mA	
	CL*	External Capacitor Load	—	—	200	pF	
D406*	DVOUT/ DIOUT	Load Regulation	—	1	TBD	mV/mA	ISOURCE = 0 mA to 5 mA
			—	1	TBD		ISINK = 0 mA to 5 mA
D407*	DVOUT/ DVDD	Supply Regulation	—	—	1	mV/V	

* These parameters are characterized but not tested.

† Data in “Typ” column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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