**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | PIC |
| Core Size | 8-Bit |
| Speed | 20MHz |
| Connectivity | - |
| Peripherals | Brown-out Detect/Reset, POR, PWM, WDT |
| Number of I/O | 13 |
| Program Memory Size | 3.5KB (2K x 14) |
| Program Memory Type | OTP |
| EEPROM Size | - |
| RAM Size | 128 x 8 |
| Voltage - Supply (Vcc/Vdd) | 4V ~ 5.5V |
| Data Converters | A/D 8x8b; D/A 1x8b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 20-SSOP (0.209", 5.30mm Width) |
| Supplier Device Package | 20-SSOP |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic16c782-i-ss |

**TABLE 1-1: PIC16C781/782 PINOUT DESCRIPTION (CONTINUED)**

| Name | Function | Input Type | Output Type | Description |
|---|---|---|---|---|
| RB7/C2/PSMC1B/$\overline{T1G}$ | RB7 | TTL | CMOS | Bi-directional I/O |
| | C2 | — | CMOS | Comparator 2 Output |
| | PSMC1B | — | CMOS | PSMC Output 1B |
| | $\overline{T1G}$ | ST | — | Timer 1 Gate Input |
| AVDD | AVDD | Power | — | Positive Supply for Analog |
| AVSS | AVSS | Power | — | Ground Reference for Analog |
| VDD | VDD | Power | — | Positive Supply for Logic and I/O pins |
| VSS | VSS | Power | — | Ground Reference for Logic and I/O pins |

Legend: ST = Schmitt Trigger AN = Analog OD = open drain TTL = Logic Level
XTAL = Crystal CMOS = CMOS Output Power = Power Supply

## 2.0 MEMORY ORGANIZATION

There are two memory blocks in each of these PIC® microcontrollers. Each block (program and data memory) has its own bus, so that concurrent access can occur.

Additional information on device memory may be found in the PIC Mid-Range Reference Manual, (DS33023).

### 2.1 Program Memory Organization

The PIC16C781/782 devices have a 13-bit program counter capable of addressing an 8K x 14 program memory space. The PIC16C781 has 1K x 14 words of program memory. The PIC16C782 has 2K x 14 words of program memory. Accessing a location above the physically implemented address causes a wraparound.

The RESET vector is at 0000h and the interrupt vector is at 0004h.

**FIGURE 2-1: PIC16C781 PROGRAM MEMORY MAP AND STACK**

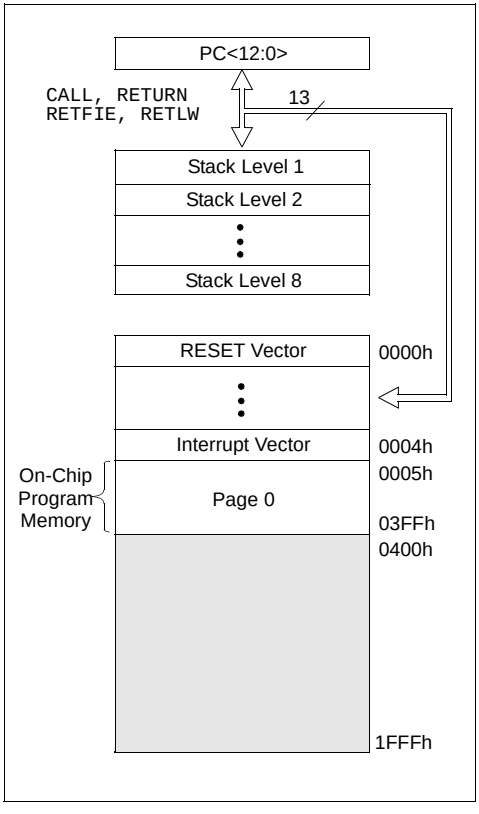
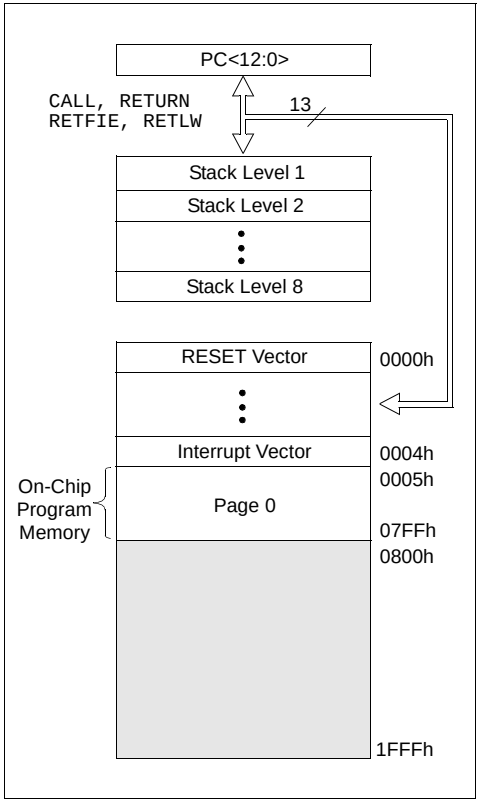



**FIGURE 2-2: PIC16C782 PROGRAM MEMORY MAP AND STACK**




### 2.2 Data Memory Organization

The data memory is partitioned into multiple banks, which contain the General Purpose Registers and the Special Function Registers. Bits RP0 and RP1 are bank select bits.

| RP1 | RP0 | (STATUS<6:5>) |
|---|---|---|

= 00 → Bank0

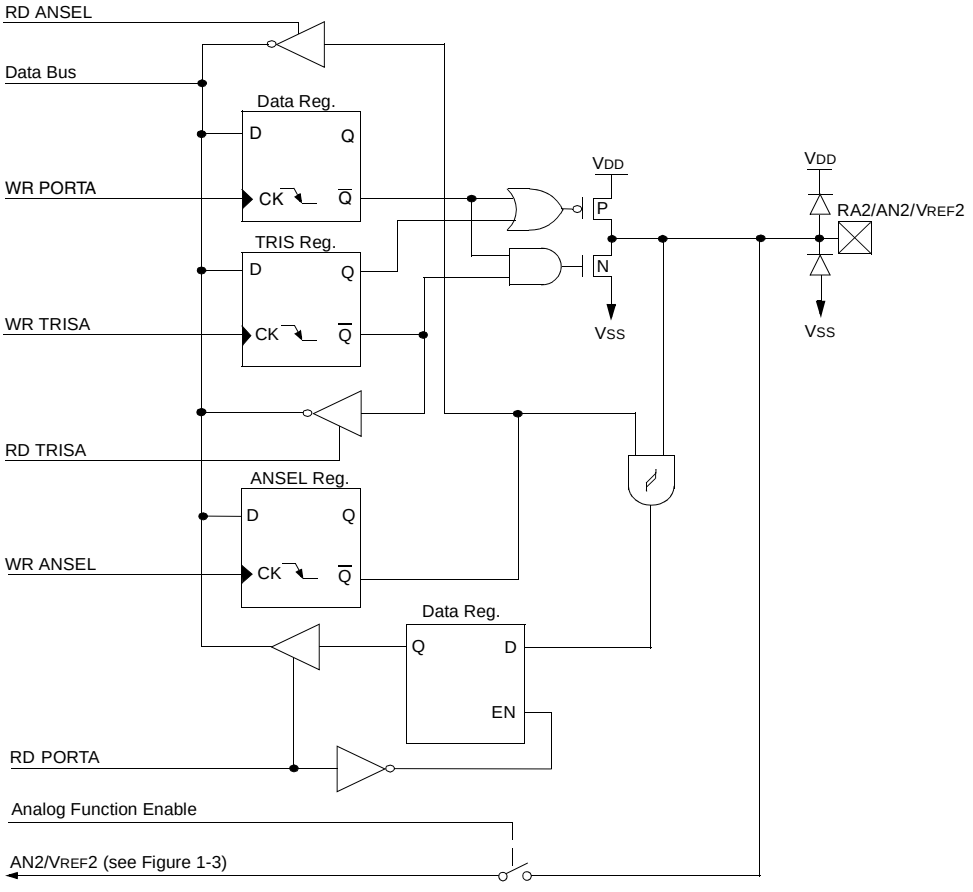
= 01 → Bank1

= 10 → Bank2

= 11 → Bank3

Each bank extends up to 7Fh (128 bytes). The lower locations of each bank are reserved for the Special Function Registers. Above the Special Function Registers are the General Purpose Registers, implemented as static RAM. All implemented banks contain Special Function Registers. Some frequently used Special Function Registers from one bank are mirrored in another bank for code reduction and quicker access.

**FIGURE 3-3: BLOCK DIAGRAM OF RA2/AN2/VREF2 PIN**




| ANSEL<2> | TRISA<2> | FUNCTION | PORTA<2> READ |
|---|---|---|---|
| 0 | 1 | Digital In | Pin |
| 0 | 0 | Digital Out | Pin |
| 1 | x | Analog In | 0 |

**NOTES:**

## 6.0 TIMER1 MODULE WITH GATE CONTROL

The Timer1 module timer/counter has the following features:

- 16-bit timer/counter
  (two 8-bit registers:TMR1H and TMR1L)
- Readable and writable (both registers)
- Internal or external clock select
- Interrupt on overflow from FFFFh to 0000h
- External enable input ($\overline{T1G}$ pin with TMR1GE bit = 1)
- Option for Timer1 to use LP oscillator if device is configured to use INTRC w/o CLKOUT

Timer1 Control register (T1CON) is shown in Register 6-1.

Figure 6-2 is a simplified block diagram of the Timer1 module.

### 6.1 Timer1 Operation

Timer1 can operate in one of three modes:

1. 16-bit timer with prescaler.
2. 16-bit synchronous counter.
3. 16-bit asynchronous counter.

In Timer mode, Timer1 is incremented on every instruction cycle. In Counter mode, Timer1 is incremented on the rising edge of the external clock input T1CKI (RA6/OSC2/CLKOUT/T1CKI). In addition, the Counter mode clock can be synchronized to the microcontroller clock or run asynchronously.

In Counter and Timer modes, the counter/timer clock can be gated by the $\overline{T1G}$ input.

If an external clock oscillator is needed (and the microcontroller is using INTRC w/o CLKOUT), Timer1 can use the LP oscillator as a clock source.

| **Note 1:** In Counter mode, the counter increments on the rising edge of the clock. |
|---|

**EXAMPLE 6-1: TIMER1 INITIALIZATION**

```
;* This code block will configure Timer1 for
;* Polling, Ext gate of int clk (Fosc/4), &
;* 1:1 prescaler.
;*
;* Wait for TMR1 overflow code included
;*
   BANKSEL  TMR1L           ; Select Bank 0
   CLRF     TMR1L           ; Clear TMR1 LSB
   CLRF     TMR1H           ; Clear TMR1 MSB
   MOVLW    B'01000000'     ; Gate, Ps 1:1
   MOVWF    T1CON           ; Int clk
   BSF      T1CON,TMR1ON    ; Enable timer

;*****************************************
;* Wait for TMR1 overflow

T1_OVFL_WAIT
   BANKSEL  PIR1            ; Select Bank 0
   T1_WAIT                  ;
   TBFSS    PIR1,TMR1IF     ; Overflow?
   GOTO     T1_WAIT         ; If 0, again

   BCF      PIR1,TMR1IF     ; Clear flag
```

## 6.2 Control Register T1CON

Control and configuration of Timer1 is by means of the T1CON register shown in Register 6-1.

Timer1 is enabled by setting the TMR1ON bit (T1CON<0>). Clearing TMR1ON stops the timer, but does not clear the Timer1 register.

The TMR1CS bit (T1CON<1>) determines the Timer mode. When TMR1CS is set, the timer is configured as a counter and receives its clock from RA6/OSC2/CLKOUT/T1CKI. When cleared, the timer is configured as a timer and its clock is derived from FOSC/4.

The $\overline{\text{T1SYNC}}$ bit (T1CON<2>) determines Timer1's synchronization. If cleared, the timer clock is synchronized to the system clock. If set, the timer is asynchronous.

The Timer1 clock gate function is enabled by setting the TMR1GE bit (T1CON<6>). When TMR1GE is set, the $\overline{\text{T1G}}$ input will control the clock input to the timer/counter. A low on the $\overline{\text{T1G}}$ input will cause Timer1 to increment at the clock rate, a high will hold the timer at its present value.

The T1OSCEN bit (T1CON<3>) enables the LP oscillator as a clock source for Timer1. This mode is a replacement for the regular external oscillator.

T1CKPS<1:0> determines the prescaler value for the timer. Available prescaler values are:

| T1CKPS<1:0> | | Prescaler Value |
|---|---|---|
| Bit 1 | Bit 0 | |
| 1 | 1 | 1:8 |
| 1 | 0 | 1:4 |
| 0 | 1 | 1:2 |
| 0 | 0 | 1:1 |

**Note:** To use the LP oscillator as the Timer1 oscillator:
1. TMR1CS must be set.
2. T1OSCEN must be set.
3. The Configuration Word must select INTRC w/o CLKOUT.

## 9.1 Control Registers

The ADC module has three registers. These registers are:

- ADC Result Register: ADRES
- ADC Control Register 0: ADCON0
- ADC Control Register 1: ADCON1

The ADCON0 register, shown in Register 9-1, controls the operations and input channel selection for the ADC module. The ADCON1 register, shown in Register 9-3, selects the voltage reference used by the ADC module. The ADRES register, shown in Register 9-2, holds the 8-bit result of the conversion.

Additional information on using the ADC module can be found in the PIC Mid-Range MCU Family Reference Manual (DS33023) and in Application Note AN546 (DS00546).

### 9.1.1 ADCON0 REGISTER

The ADCON0 register, shown in Register 9-1, controls the following:

- Clock source and prescaler
- Input channel
- Conversion start/stop
- Enabling of the ADC module

Setting the ADON bit, ADCON0<0>, enables the ADC module. Clearing ADON disables the module and terminates any conversion in process.

The ADCS<1:0> bits (ADCON0<7:6>) determine the clock source used by the ADC module.

The CHS<3:0> bits (ADCON0<5:3,1>) determine the input channel to the ADC module. CHS<3> specifically determines whether the source is internal or external.

Setting the GO/$\overline{\text{DONE}}$ bit (ADCON0<2>) initiates the conversion process. The ADC clears this bit at the completion of the conversion process.

**REGISTER 9-1: ADC CONTROL REGISTER 0 (ADCON0: 1Fh)**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/S-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| ADCS1 | ADCS0 | CHS2 | CHS1 | CHS0 | GO/$\overline{\text{DONE}}$ | CHS3 | ADON |
| bit 7 | | | | | | | bit 0 |

bit 7-6 **ADCS<1:0>:** ADC Conversion Clock Select bits
00 = FOSC/2
01 = FOSC/8
10 = FOSC/32
11 = ADRC (clock derived from a dedicated RC oscillator)

bit 5-3 **CHS<2:0>:** Analog Channel Select bits (select which channel to convert)

| If CHS3 = 0: | If CHS3 = 1: |
|---|---|
| 000 = channel 0 (AN0) | 000 = VR |
| 001 = channel 1 (AN1) | 001 = VDAC |
| 010 = channel 2 (AN2) | 010 = Reserved. Do not use. |
| 011 = channel 3 (AN3) | 011 = Reserved. Do not use. |
| 100 = channel 4 (AN4) | 100 = Reserved. Do not use. |
| 101 = channel 5 (AN5) | 101 = Reserved. Do not use. |
| 110 = channel 6 (AN6) | 110 = Reserved. Do not use. |
| 111 = channel 7 (AN7) | 111 = Reserved. Do not use. |

bit 2 **GO/$\overline{\text{DONE}}$:** ADC Conversion Status bit
1 = ADC conversion cycle in progress. Setting this bit starts an ADC conversion cycle.
0 = ADC conversion is not in progress (this bit is cleared by hardware when conversion is complete)

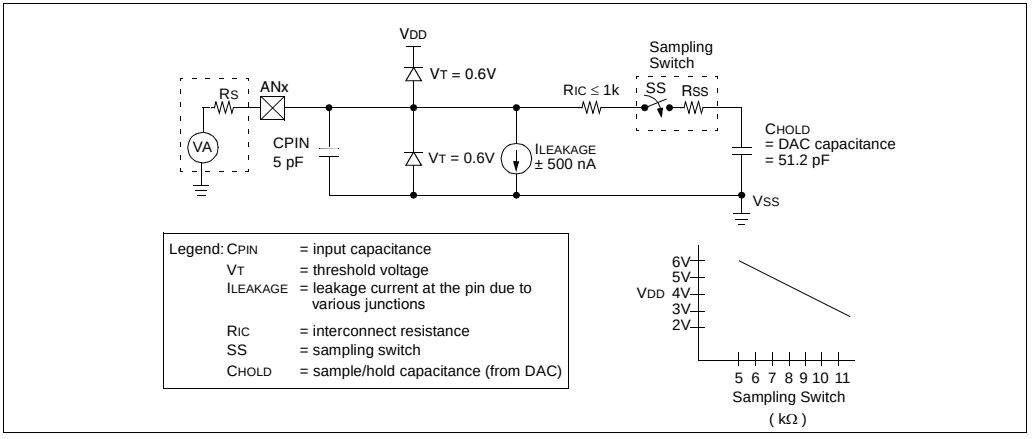
bit 1 **CHS3:** Analog Channel Select bit
1 = Internal channel selected for conversion
0 = External channel selected for conversion

bit 0 **ADON:** ADC On bit
1 = ADC enabled
0 = ADC disabled

| Legend: | | | |
|---|---|---|---|
| S = Settable bit | | | |
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| - n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

**FIGURE 9-2: ANALOG INPUT MODEL**




## 9.4 ADC Configuration and Conversion

Example 9-2 demonstrates an ADC conversion. The RA0/AN0 pin is configured as the analog input. The reference voltage selected is the device AVDD. The ADC interrupt is enabled, and the ADC conversion clock is ADRC.

Clearing the GO/$\overline{\text{DONE}}$ bit during a conversion aborts the current conversion. The ADRES register is NOT updated with the partially completed ADC conversion sample. That is, the ADRES register continues to contain the value of the last completed conversion (or the last value written to the ADRES register). After the ADC conversion is aborted, a 2TAD wait period is required before the next acquisition is started. After this 2TAD wait period, an acquisition is automatically started on the selected channel.

**EXAMPLE 9-2: ADC CONVERSION**

```
;*****************************************
;*  This code block will configure the ADC
;*  for polling, AVDD as reference, RC clock
;*  and RA0 input.
;*
;*  Conversion start & wait for complete
;*  polling code included.
;*
    BANKSEL    ADCON1      ; Select Bank 1
    CLRF       ADCON1      ; AVDD as VREF
    BSF        TRISA,0     ; Set RA0 as input
    BSF        ANSEL,0     ; Set RA0 as analog

    BANKSEL    ADCON0      ; Select Bank0
    MOVLW      B'11000001'
    MOVWF      ADCON0      ; RC, Ch 0, ADC on

;*****************************************
;*  Start & Wait for ADC complete, assumes
;*  minimum acquisition delay from
;*  configuration.

ADC_CNVRT
    BANKSEL    ADCON0      ; Select Bank 0
    BSF        ADCON0,GO   ; Start convert
ADC_CN_LOOP
    BTFSC      ADCON0,GO   ; Test for end
    GOTO       ADC_CN_LOOP ; If not, wait
    MOVF       ADRES,W     ; Get result
```

### 9.4.1 FASTER CONVERSION/LOWER RESOLUTION TRADE-OFF

Not all applications require a result having 8-bits of resolution. Some may instead, require a faster conversion time. The ADC module allows users to make a trade-off of conversion speed for resolution. Regardless of the resolution required, the acquisition time is the same. To speed up the conversion, the clock source of the ADC module may be switched during the conversion, so that the TAD time violates the minimum specified time (see the applicable Electrical Specification). Once the switch is made, all the following ADC result bits are invalid (see ADC Conversion Timing in the Electrical Specifications section). The clock source may only be switched between the three oscillator options (it cannot be switched from/to RC). The equation to determine the time before the oscillator must be switched for a desired resolution is as follows:

Conversion time = $2T_{AD} + N \bullet T_{AD} + (8 - N)(2T_{OSC})$

Where: N = number of bits of resolution required.

Since the TAD is based on the device oscillator, the user must employ some method (such as a timer, software loop, etc.) to determine when the ADC oscillator must be changed.

## 9.5 ADC Operation During SLEEP

The ADC module can operate during SLEEP mode. This requires that the ADC clock source be set to RC (ADCS1:ADCS0 = 11). When the RC clock source is selected, the ADC module waits one instruction cycle before starting the conversion. This allows the SLEEP instruction to be executed, which eliminates all digital switching noise from the conversion. When the conversion is completed the GO/DONE bit is cleared, and the result is loaded into the ADRES register. If the ADC interrupt is enabled, the device awakens from SLEEP. If the ADC interrupt is not enabled, the ADC module is turned off, although the ADON bit remains set.

When the ADC clock source is another clock option (not RC), a SLEEP instruction causes the present conversion to be aborted and the ADC module to be turned off. The ADON bit remains set.

Turning off the ADC places the ADC module in its lowest current consumption state.

| **Note:** | For the ADC module to operate in SLEEP, the A/D clock source must be set to RC (ADCS1:ADCS0 = 11). To perform an ADC conversion in SLEEP, ensure the SLEEP instruction immediately follows the instruction that sets the GO/DONE bit. |
|---|---|

## 9.6 ADC Accuracy/Error

The absolute accuracy (absolute error) specified for the ADC converter includes the sum of all contributions for:

- Offset error
- Gain error
- Quantization error
- Integral non-linearity error
- Differential non-linearity error
- Monotonicity

The **absolute error** is defined as the maximum deviation from an actual transition versus an ideal transition for any code. The absolute error of the ADC converter is specified as < ±1 LSb for $ADC_{REF} = V_{DD}$ (over the device's specified operating range). However, the accuracy of the ADC converter degrades as $V_{DD}$ diverges from $V_{REF}$.

For a given range of analog inputs, the output digital code will be the same. This is due to the quantization of the analog input to a digital code. **Quantization error** is typically ± 1/2 LSb and is inherent in the analog to digital conversion process. The only way to reduce quantization error is to use an ADC with greater resolution of the ADC converter.

**Offset error** measures the first actual transition of a code versus the first ideal transition of a code. Offset error shifts the entire transfer function. Offset error can be calibrated out of a system, or introduced into a system, through the interaction of the total leakage current and source impedance at the analog input.

**Gain error** measures the maximum deviation of the last actual transition and the last ideal transition adjusted for offset error. This error appears as a change in slope of the transfer function. The difference in gain error to full scale error is that full scale does not take offset error into account. Gain error can be calibrated out in software.

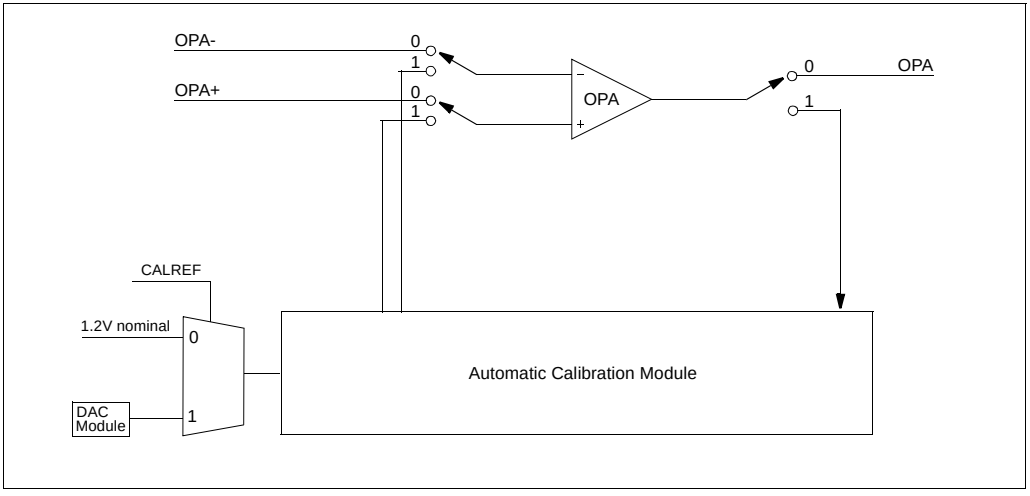
**Linearity error** refers to the uniformity of the code changes. Linearity errors cannot be calibrated out of the system. **Integral non-linearity error** measures the actual code transition versus the ideal code transition, adjusted by the gain error for each code. **Differential non-linearity** measures the maximum actual code width versus the ideal code width. This measure is unadjusted.

If the linearity errors are very large, the ADC may become **non-monotonic**. This occurs when the digital values for one or more input voltages are less than the value for a lower input voltage.

**NOTES:**

**FIGURE 11-2: AUTO CALIBRATION MODULE BLOCK DIAGRAM**




**REGISTER 11-2: CALIBRATION CONTROL REGISTER (CALCON: 110h)**

| R/S-0 | R-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| CAL | CALERR | CALREF | — | — | — | — | — |
| bit 7 | | | | | | | bit 0 |

bit 7 **CAL:** Start and Status bit
1 = Initiates a calibration
0 = Reserved (CAL is cleared by hardware)

bit 6 **CALERR:** Calibration Error Indicator bit
1 = Error occurred, OPAMP failed
0 = No error

bit 5 **CALREF:** Calibration Voltage Select bit
1 = $V_{DAC}$ set to desired common voltage reference
0 = 1.2V nominal source (internal voltage source)

**Note:** $V_{DAC}$ must not exceed OPAMP maximum common mode voltage.

bit 4-0 **Reserved:** Do not use

| Legend: | | | |
|---|---|---|---|
| S = Cleared by hardware | | | |
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| - n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

## 11.2 Configuration as OPAMP or Comparator

The following example demonstrates calibration of the OPA module as an Operational Amplifier.

**EXAMPLE 11-1: CALIBRATION FOR OPAMP MODE**

```
;*  This code block will configure the OPA
;*  module as an Op Amp, 2 MHz GBWP, and
;*  calibrated for a common mode voltage of
;*  1.2V. Routine returns w=0 if
;*  calibration good.

    BANKSEL     OPACON       ; Select Bank 2
    MOVLW       B'10000001'  ; Op Amp mode &
    MOVWF       OPACON       ; 2 MHz GBWP

    BCF         CALCON,CALREF; Set 1.2V
    BSF         CALCON,CAL   ; Start

CAL_LOOP
    BTFSC       CALCON,CAL   ; Test for end
    GOTO        CAL_LOOP     ; If not, wait
    MOVLW       ERROR_FLAG
    BTFSS       CALCON,CALERR; Test for error
    CLRW                     ; If no, return 0
    RETURN
```

The following example demonstrates how to configure and calibrate the OPA module as a Voltage Comparator.

**EXAMPLE 11-2: CALIBRATION FOR COMPARATOR MODE**

```
;*  This code block will configure the OPA
;*  module as a voltage comparator, slow
;*  speed, and calibrated for a common mode
;*  voltage of 2.5 V (assumes VDD=5V).
;*  Routine returns w=0 if calibration good.

    BANKSEL     OPACON       ; Select Bank 2
    MOVLW       B'10000000'
    MOVWF       OPACON       ; Op Amp mode,
                             ; slow
    BSF         CALCON,CALREF; Common mode=DAC

    MOVLW       H'0x80'
    MOVWF       DAC          ; DAC at VDD/2
    MOVLW       B'10000000'
    MOVWF       DACON0       ; enable DAC,
                             ; VDD ref
    BSF         CALCON,CAL   ; Start
CAL_LOOP
    BTFSC       CALCON,CAL   ; Test for end
    GOTO        CAL_LOOP     ; If not, wait

    MOVLW       ERROR_FLAG
    BTFSS       CALCON,CALERR; Test for error
    CLRW                     ; If no, return 0
    BSF         OPACON,CMPEN ; Comparator mode
    RETURN
```

## 11.3 Effects of RESET

A device RESET forces all registers to their RESET state. This disables the OPA module and clears any calibration.

## 11.4 OPA Module Performance

Common AC and DC performance specifications for the OPA module:

- Common Mode Voltage Range
- Leakage Current
- Input Offset Voltage
- Open Loop Gain
- Gain Bandwidth Product

**Common mode voltage range** is the specified voltage range for the OPA+ and OPA- inputs, for which the OPA module will perform to within its specifications. The OPA module is designed to operate with input voltages between 0 and $V_{DD}$-1.4V. Behavior for Common mode voltages greater than $V_{DD}$-1.4V, or below 0V, are not guaranteed.

**Leakage current** is a measure of the small source or sink currents on the OPA+ and OPA- inputs. To minimize the effect of leakage currents, the effective impedances connected to the OPA+ and OPA- inputs should be kept as small as possible and equal.

**Input offset voltage** is a measure of the voltage difference between the OPA+ and OPA- inputs in a closed loop circuit with the OPA in its linear region. The offset voltage will appear as a DC offset in the output equal to the input offset voltage, multiplied by the gain of the circuit. The input offset voltage is also affected by the Common mode voltage. The OPA has an automatic calibration module which can minimize the input offset voltage of the module.

**Open loop gain** is the ratio of the output voltage to the differential input voltage, (OPA+) - (OPA-). The gain is greatest at DC and falls off with frequency.

**Gain Bandwidth Product** or GBWP is the frequency at which the open loop gain falls off to 0 dB. The lower GBWP is optimized for systems requiring low frequency response and low power consumption.

#### 12.1.2.2 Control Register CM2CON1

Comparator C2 has one additional feature: its output can be synchronized to the Timer1 clock input. Setting C2SYNC (CM2CON1<0>) synchronizes the output of Comparator 2 to the falling edge of Timer 1's clock input (see Figure 12-1 and Register 12-3).

The CM2CON1 register also contains mirror copies of both comparator outputs, MC1OUT and MC2OUT (CM2CON1<7:6>). The ability to read both outputs simultaneously from a single register eliminates the timing skew of reading separate registers.

**REGISTER 12-3: COMPARATOR C2 CONTROL REGISTER1 (CM2CON1: 11Bh)**

| R-0 | R-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| MC1OUT | MC2OUT | — | — | — | — | — | C2SYNC |
| bit 7 | | | | | | | bit 0 |

bit 7 **MC1OUT:** Mirror Copy of C1OUT (CM1CON0<6>)

bit 6 **MC2OUT:** Mirror Copy of C2OUT (CM2CON0<6>)

bit 5-1 **Unimplemented:** Read as '0'

bit 0 **C2SYNC:** C2 Output Synchronous Mode bit

1 = C2 output is synchronous to falling edge of TMR1 clock

0 = C2 output is asynchronous

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| - n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

**EXAMPLE 12-3: WINDOW COMPARATOR**

```
;*  Example of Low Power Window Comparator C1
;*  This code block will configure Comparator
;*   C1 and C2 for slow speed, C1 non invert,
;*  C2 invert, input on AN4, and external
;*  References
;*
;*  Interrupt service routine included
;*
    BANKSEL     TRISA       ; Select Bank 1
    BSF         TRISA,2     ; RA2 input
    BSF         TRISA,3     ; RA3 input
    BSF         TRISB,0     ; Set RB0

    BSF         ANSEL,AN2   ; RA2 analog
    BSF         ANSEL,AN3   ; RA3 analog
    BSF         ANSEL,AN4   ; RB4 analog

    BANKSEL     CM1CON0     ; Select Bank 2
    MOVLW       B'10000000'; C1: no output
    MOVWF       CM1CON0     ; VREF1, AN4
    MOVLW       B'10010000'; C2: no output
    MOVWF       CM2CON0     ; invert,VREF1,AN4

    BANKSEL     PIE1        ; Select Bank 1
    BCF         INTCON,GIE  ; Disable Int
    BSF         PIE1,C1IE   ; Enabl C1&C2 Ints
    BSF         PIE1,C2IE
    BSF         INTCON,PEIE
    BSF         INTCON,GIE ; Enabl Global Ints
;*********************************************
;*  WINDOW COMPARATOR ISR with context save

WC_INT_SRV_R
    MOVWF       W_SAVE      ; Save W & STATUS
    SWAPF       STATUS,W
    MOVWF       STATUS_SAV

    BANKSEL     PIR1        ; Select Bank 0
    MOVLW       B'00110000'; Save Int
    ANDWF       PIR1,W
    MOVWF       WIN_INT

;*** CLEAR C1 INTERRUPT

    BTFSS       WIN_INT,C1IF; C1 Int ?
    GOTO        TST_C2_INT
    BANKSEL     CM1CON0     ; Select Bank 2
    MOVF        CM1CON0,F   ; Clear C2 mismatch
    BANKSEL     PIR1        ; Select Bank 0
    BCF         PIR1,C1IF   ; Clear C2 Int

;*** CLEAR C2 INTERRUPT

TXT_C2_INT
    BTFSS       WIN_INT,C2IF; C2 int?
    GOTO        USER_ISR
    BANKSEL     CM2CON0     ; Select Bank 2
    MOVF        CM2CON0,F   ; Clear C2 mismatch
    BANKSEL     PIR1        ; Select Bank 0
    BCF         PIR1,C1IF   ; Clear C2 int

USER_ISR
;*** USER INTERRUPT ROUTING
;*

    SWAPF       STATUS_SAVE,W; Restore W &
                            ; STATUS
    MOVWF       STATUS
    SWAPF       W_SAVE,F
    SWAPF       W_SAVE,W
    RETFIE                  ; Return
```

## 12.3 Effects of RESET

A RESET forces all registers to their RESET state. This disables both comparators.

**TABLE 12-2: REGISTERS ASSOCIATED WITH THE COMPARATOR MODULE**

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on: POR, BOR | Value on all other RESETS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 119h | CM1CON0 | C1ON | C1OUT | C1OE | C1POL | C1SP | C1R | C1CH1 | C1CH0 | 0000 0000 | 0000 0000 |
| 11Ah | CM2CON0 | C2ON | C2OUT | C2OE | C2POL | C2SP | C2R | C2CH1 | C2CH0 | 0000 0000 | 0000 0000 |
| 11Bh | CM2CON1 | MC1OUT | MC2OUT | — | — | — | — | — | C2SYNC | 00-- ---0 | 00-- ---0 |
| 85h | TRISA | PORTA Data Direction Register | | | | | | | | 1111 1111 | 1111 1111 |
| 86h | TRISB | PORTB Data Direction Register | | | | | | | | 1111 1111 | 1111 1111 |
| 05h | PORTA | RA7 | RA6 | RA5 | RA4 | RA3 | RA2 | RA1 | RA0 | xxxx 0000 | uuuu 0000 |
| 06h | PORTB | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 | xxxx 0000 | uuuu 0000 |
| 9Dh | ANSEL | AN7 | AN6 | AN5 | AN4 | AN3 | AN2 | AN1 | AN0 | 1111 1111 | 1111 1111 |
| 0Ch | PIR1 | LVDIF | ADIF | C2IF | C1IF | — | — | — | TMR1ON | 0000 ---0 | 0000 ---0 |
| 8Ch | PIE1 | LVDIE | ADIE | C2IE | C1IE | — | — | — | TMR1IE | 0000 ---0 | 0000 ---0 |

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used for comparator.

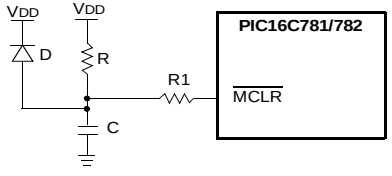
## 14.4 Power-on Reset (POR)

A Power-on Reset pulse is generated on-chip when a VDD rise is detected (in the range of 1.5V - 2.1V). To take advantage of the POR, simply enable the internal MCLR feature. This eliminates external RC components usually needed to create a Power-on Reset. A maximum rise time for VDD is specified. See Section 17.0 for details. For a slow rise time, see Figure 14-5.

Two delay timers (PWRT on OST) are provided, which hold the device in RESET after a POR (dependent upon device configuration), so that all operational parameters have been met prior to releasing the device to resume/begin normal operation.

When the device starts normal operation (exits the RESET condition), device operating parameters (i.e., voltage, frequency, temperature,...) must be met to ensure operation. If these conditions are not met, the device must be held in RESET until the operating conditions are met. Brown-out Reset may be used to meet the start-up conditions, or if necessary an external POR circuit may be implemented to delay end of RESET for as long as needed.

**FIGURE 14-5: EXTERNAL POWER-ON RESET CIRCUIT (FOR SLOW VDD RAMP)**




**Note 1:** External Power-on Reset circuit is required only if VDD power-up slope is too slow. The diode D helps discharge the capacitor quickly when VDD powers down.

**2:** R < 40 kΩ is recommended to make sure that voltage drop across R does not violate the device's electrical specification.

**3:** R1 = 100Ω to 1 kΩ will limit any current flowing into MCLR from external capacitor C in the event of MCLR pin breakdown due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS).

## 14.5 Power-up Timer (PWRT)

The Power-up Timer provides a fixed TPWRT time-out on power-up type RESETS only. For a POR, the PWRT is invoked when the POR pulse is generated. For a BOR, the PWRT is invoked when the device exits the RESET condition (VDD rises above BOR trip point). The Power-up Timer operates on an internal RC oscillator. The chip is kept in RESET as long as the PWRT is active. The PWRT's time delay is designed to allow VDD to rise to an acceptable level. A configuration bit (PWRT) is provided to enable/disable the PWRT for the POR only. For a BOR the PWRT is always available regardless of the configuration bit setting.

The power-up time delay varies from chip-to-chip due to VDD, temperature and process variation. See DC parameters for details.

## 14.6 Programmable Brown-out Reset (PBOR)

The Programmable Brown-out Reset module is used to generate a RESET when the supply voltage falls below a specified trip voltage. The trip voltage is configurable to any one of four voltages provided by the BORV<1:0> configuration word bits.

Configuration bit BODEN can disable (if clear/programmed), or enable (if set), the Brown-out Reset circuitry. If VDD falls below the specified trip point for longer than TBOR (see Parameter 35, Section 17.0, Table 17-6), the brown-out situation resets the chip. A RESET may not occur if VDD falls below the trip point for less than TBOR. The chip remains in Brown-out Reset until VDD rises above VBOR. The Power-up Timer is invoked at that point and keeps the chip in RESET an additional TPWRT. If VDD drops below VBOR while the Power-up Timer is running, the chip goes back into a Brown-out Reset and the Power-up Timer is re-initialized. Once VDD rises above VBOR, the Power-up Timer again begins a TPWRT time delay.

## 14.7 Time-out Sequence

On power-up, the time-out sequence is as follows: First, PWRT time-out is invoked by the POR pulse. When the PWRT delay expires, the Oscillator Start-up Timer is activated. The total time-out varies depending on oscillator configuration and the status of the PWRT. For example, in RC mode with the PWRT disabled, there is no time-out at all. Figure 14-6, and Figure 14-9 depict time-out sequences on power-up.

Since the time-outs occur from the POR pulse, if MCLR is kept low long enough, the time-outs expire. Then, bringing MCLR high begins execution immediately. This is useful for testing purposes or to synchronize more than one PIC microcontroller operating in parallel.

Table 14-5 shows the RESET conditions for some special function registers.

**REGISTER 14-2: POWER CONTROL REGISTER (PCON: 8Eh)**

| U-0 | U-0 | U-0 | R/W-q | R/W-1 | U-0 | R/W-q | R/W-x |
|---|---|---|---|---|---|---|---|
| — | — | — | WDTON | OSCF | — | $\overline{\text{POR}}$ | $\overline{\text{BOR}}$ |
| bit 7 | | | | | | | bit 0 |

bit 7-5 **Unimplemented:** Read as '0'

bit 4 **WDTON:** WDT Software Enable bit

If WDTE bit (Configuration Word <3>) = 1:
This bit is not writable, always reads '1'

If WDTE bit (Configuration Word <3>) = 0:
1 = WDT is enabled
0 = WDT is disabled and cleared

bit 3 **OSCF:** Oscillator Speed bit (pending on new internal oscillator decision)

INTRC mode:
1 = 4 MHz typical
0 = 37 kHz typical

All other oscillator modes:
Ignored

bit 2 **Unimplemented:** Read as '0'

bit 1 **$\overline{\text{POR}}$:** Power-on Reset Status bit

1 = No Power-on Reset occurred
0 = A Power-on Reset occurred (must be set in software after a Power-on Reset occurs)

bit 0 **$\overline{\text{BOR}}$:** Brown-out Reset Status bit

1 = No Brown-out Reset occurred
0 = A Brown-out Reset occurred (must be set in software after a Brown-out Reset occurs)

| Legend: | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| - n = Value at POR | '1' = Bit is set | '0' = Bit is cleared |
| x = Bit is unknown | 'q' = Value depends on condition | |

**TABLE 14-4: STATUS BITS AND THEIR SIGNIFICANCE**

| $\overline{\text{POR}}$ | $\overline{\text{BOR}}$ | $\overline{\text{TO}}$ | $\overline{\text{PD}}$ | Bit Significance |
|---|---|---|---|---|
| 0 | 1 | 1 | 1 | Power-on Reset |
| 0 | x | 0 | x | Illegal, $\overline{\text{TO}}$ is set on $\overline{\text{POR}}$ |
| 0 | x | x | 0 | Illegal, $\overline{\text{PD}}$ is set on $\overline{\text{POR}}$ |
| 1 | 0 | 1 | 1 | Brown-out Reset |
| 1 | 1 | 0 | 1 | WDT Reset |
| 1 | 1 | 0 | 0 | WDT Wake-up |
| 1 | 1 | u | u | $\overline{\text{MCLR}}$ Reset during normal operation |
| 1 | 1 | 1 | 0 | $\overline{\text{MCLR}}$ Reset during SLEEP or interrupt wake-up from SLEEP |

**TABLE 16-1: DEVELOPMENT TOOLS FROM MICROCHIP**

| | | PIC12CXXX | PIC14000 | PIC16C5X | PIC16C6X | PIC16CXXX | PIC16F62X | PIC16C7X | PIC16C7XX | PIC16C8X | PIC16F8XX | PIC16C9XX | PIC17C4X | PIC17C7XX | PIC18CXX2 | PIC18FXXX | 24CXX/ 25CXX/ 93CXX | HCSXXX | MCRFXXX | MCP2510 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Software Tools | MPLAB® Integrated Development Environment | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | | | |
| | MPLAB® C17 C Compiler | | | | | | | | | | | | ✓ | ✓ | | | | | | |
| | MPLAB® C18 C Compiler | | | | | | | | | | | | | | ✓ | ✓ | | | | |
| | MPASM™ Assembler/ MPLINK™ Object Linker | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | |
| Emulators | MPLAB® ICE In-Circuit Emulator | ✓ | ✓ | ✓ | ✓ | ✓ | ✓** | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | | | |
| | ICEPIC™ In-Circuit Emulator | ✓ | | ✓ | ✓ | ✓ | | ✓ | ✓ | ✓ | | ✓ | | | | | | | | |
| Debugger | MPLAB® ICD In-Circuit Debugger | | | | ✓* | | | ✓* | | | ✓ | | | | | ✓ | | | | |
| Programmers | PICSTART® Plus Entry Level Development Programmer | ✓ | ✓ | ✓ | ✓ | ✓ | ✓** | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | | | |
| | PRO MATE® II Universal Device Programmer | ✓ | ✓ | ✓ | ✓ | ✓ | ✓** | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | |
| Demo Boards and Eval Kits | PICDEM™ 1 Demonstration Board | | | ✓ | | ✓ | | ✓† | | ✓ | | | ✓ | | | | | | | |
| | PICDEM™ 2 Demonstration Board | | | | ✓† | | | ✓† | | | | | | | ✓ | ✓ | | | | |
| | PICDEM™ 3 Demonstration Board | | | | | | | | | | | ✓ | | | | | | | | |
| | PICDEM™ 14A Demonstration Board | | ✓ | | | | | | | | | | | | | | | | | |
| | PICDEM™ 17 Demonstration Board | | | | | | | | | | | | | ✓ | | | | | | |
| | KEELOQ® Evaluation Kit | | | | | | | | | | | | | | | | | ✓ | | |
| | KEELOQ® Transponder Kit | | | | | | | | | | | | | | | | | ✓ | | |
| | microID™ Programmer's Kit | | | | | | | | | | | | | | | | | | ✓ | |
| | 125 kHz microID™ Developer's Kit | | | | | | | | | | | | | | | | | | ✓ | |
| | 125 kHz Anticollision microID™ Developer's Kit | | | | | | | | | | | | | | | | | | ✓ | |
| | 13.56 MHz Anticollision microID™ Developer's Kit | | | | | | | | | | | | | | | | | | ✓ | |
| | MCP2510 CAN Developer's Kit | | | | | | | | | | | | | | | | | | | ✓ |

* Contact the Microchip Technology Inc. web site at www.microchip.com for information on how to use the MPLAB® ICD In-Circuit Debugger (DV164001) with PIC16C62, 63, 64, 65, 72, 73, 74, 76, 77.

** Contact Microchip Technology Inc. for availability date.

† Development tool is available on select devices.

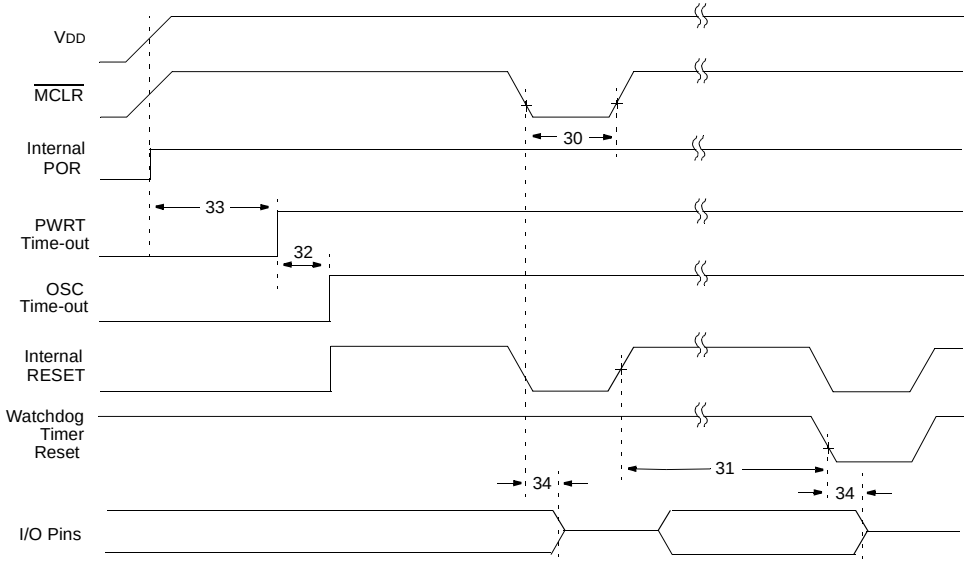
**TABLE 17-5: INTERNAL RC OSCILLATOR CALIBRATED FREQUENCIES PIC16C781/782, DSTEMP**

| AC Characteristics | | Standard Operating Conditions (unless otherwise specified)<br>Operating Temperature –40×C ≤ TA ≤ +85°C (industrial)<br>Operating Voltage VDD range is described in Section 17-1. | | | | | |
|---|---|---|---|---|---|---|---|
| **Parameter No.** | **Sym** | **Characteristic** | **Min** | **Typ(1)** | **Max** | **Units** | **Conditions** |
| | | Internal Calibrated RC Frequency | 3.65 | 4.00 | 4.28 | MHz | VDD = 5.0V |
| | | Internal Calibrated RC Frequency | 3.55* | 4.00 | 4.31* | MHz | VDD = 2.5V |

* These parameters are characterized but not tested.

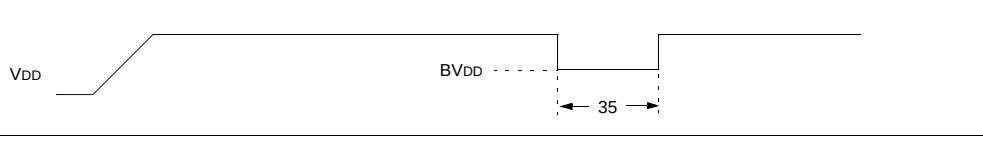
**Note 1:** Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**FIGURE 17-6: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING**




**Note 1:** Refer to Figure 17-3 for load conditions.

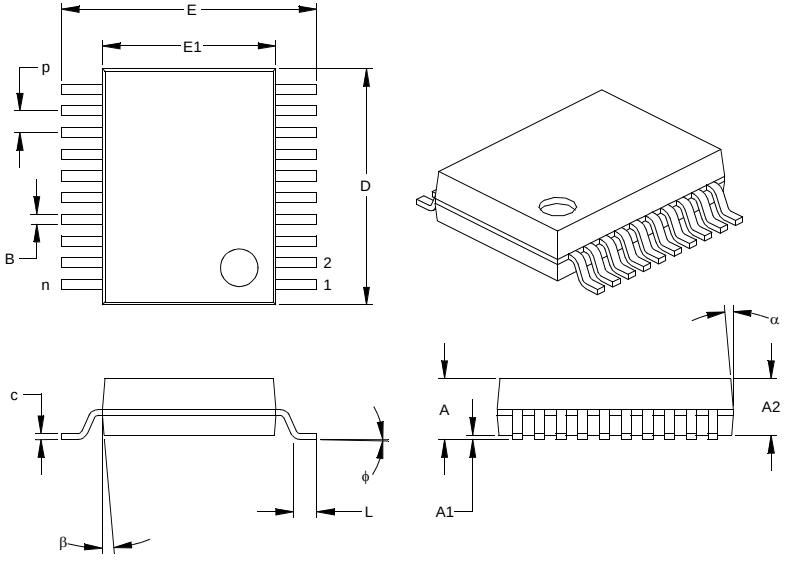
**FIGURE 17-7: BROWN-OUT RESET TIMING**



### 20-Lead Plastic Shrink Small Outline (SS) – 209 mil, 5.30 mm (SSOP)

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | INCHES* | | | MILLIMETERS | | |
|---|---|---|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX | MIN | NOM | MAX |
| Number of Pins | n | | 20 | | | 20 | |
| Pitch | p | | .026 | | | 0.65 | |
| Overall Height | A | .068 | .073 | .078 | 1.73 | 1.85 | 1.98 |
| Molded Package Thickness | A2 | .064 | .068 | .072 | 1.63 | 1.73 | 1.83 |
| Standoff § | A1 | .002 | .006 | .010 | 0.05 | 0.15 | 0.25 |
| Overall Width | E | .299 | .309 | .322 | 7.59 | 7.85 | 8.18 |
| Molded Package Width | E1 | .201 | .207 | .212 | 5.11 | 5.25 | 5.38 |
| Overall Length | D | .278 | .284 | .289 | 7.06 | 7.20 | 7.34 |
| Foot Length | L | .022 | .030 | .037 | 0.56 | 0.75 | 0.94 |
| Lead Thickness | c | .004 | .007 | .010 | 0.10 | 0.18 | 0.25 |
| Foot Angle | ϕ | 0 | 4 | 8 | 0.00 | 101.60 | 203.20 |
| Lead Width | B | .010 | .013 | .015 | 0.25 | 0.32 | 0.38 |
| Mold Draft Angle Top | α | 0 | 5 | 10 | 0 | 5 | 10 |
| Mold Draft Angle Bottom | β | 0 | 5 | 10 | 0 | 5 | 10 |

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.
JEDEC Equivalent: MO-150
Drawing No. C04-072