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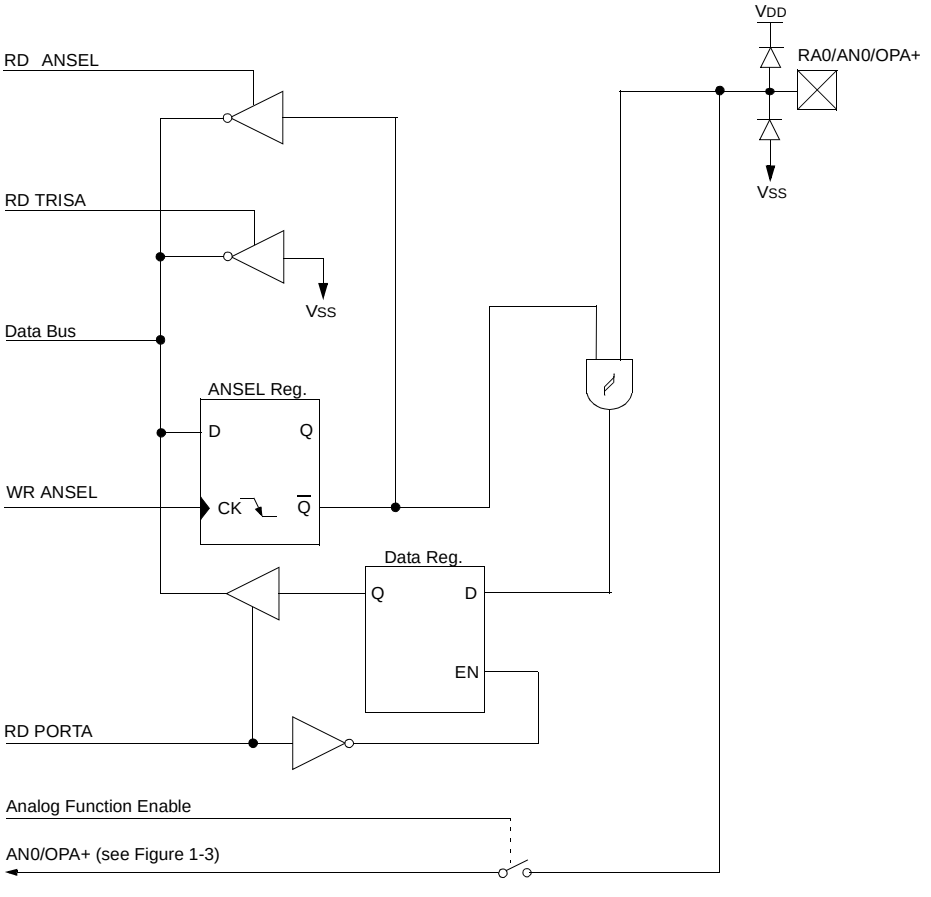
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	13
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 8x8b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	20-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c782t-i-so

FIGURE 3-1: BLOCK DIAGRAM OF RA0/AN0/OPA+ PIN



ANSEL<0>	TRISA<0>	FUNCTION	PORTA<0> READ
0	x	Digital In	Pin
1	x	Analog In	0

NOTES:

Example 8-1 shows the configuration of the PLVD module and a sample polling routine to monitor for low voltage conditions.

EXAMPLE 8-1: PLVD EXAMPLE

```
;*************************************************
;*  This code block will configure the PLVD for polling
;*  and set the trip point for 4.2 to 4.4 volts
;*  Includes polling routine
;*

    BANKSEL     LVDCON              ; Select Bank 1
    BCF         PIE1,LVDIE          ; Disable PLVD interrupt
    MOVLW       B'00011101'
    MOVWF       LVDCON              ; Enable PLVD, 4.2-4.4V trip

WRM_UP
    BTFSS       LVDCON,BGST         ;
    GOTO        WRM_UP              ;
    BANKSEL     PIR1                ; Select Bank 0
    BCF         PIR1,LVDIF          ; Clear PLVD interrupt flag

;*************************************************
;* Test for PLVD trip

    BANKSEL     PIR1                ; Select Bank 0
    BTFSC       PIR1,LVDIF          ; Test for PLVD trip
    GOTO        LO_V_DET            ; If tripped save 4 pwrfail
```

8.3 Operation During SLEEP

When enabled, the PLVD circuitry continues to operate during SLEEP. If the device voltage crosses the trip point, the LVDIF bit is set and the device awakens from SLEEP. Device execution continues from the interrupt vector address, if interrupts have been globally enabled.

8.4 Effects of a RESET

A device RESET forces all registers to their RESET state. This forces the PLVD module to be disabled.

8.5 Low Voltage Detect Registers

The registers associated with Programmable Low Voltage Detect are shown in Table 8-1.

TABLE 8-1: SUMMARY OF REGISTERS ASSOCIATED WITH LOW VOLTAGE DETECT

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other RESETS
09Ch	LVDCON	—	—	BGST	LVDEN	LV3	LV2	LV1	LV0	--00 0101	--00 0101
08Ch	PIE1	LVDIE	ADIE	C2IE	C2IE	—	—	—	TMR1IE	0000 ---0	0000 ---0
08Ch	PIR1	LVDIF	ADIF	C2IF	C2IF	—	—	—	TMR1IF	0000 ---0	0000 ---0

9.1.2 ADCON1 REGISTER

The ADCON1 register, shown in Register 9-3, controls the reference voltage selection for the ADC module.

Bits VCFG<1:0> select the reference voltage (ADCREF).

9.1.3 ADRES REGISTER

The ADRES register, shown in Register 9-2, contains the 8-bit result of the conversion. At the completion of the ADC conversion:

- 8-bit result is loaded into ADRES.
- GO/$\overline{\text{DONE}}$ bit (ADOCN0<2>) is cleared.
- ADC interrupt flag bit ADIF (INTCON<6> and PIR1<6>) are set.
- If the ADC interrupt is enabled, an interrupt is also generated.

REGISTER 9-2: ADC RESULT REGISTER (ADRES: 1Eh)

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
bit 7							bit 0

bit 7-0 **AD<7:0>:** ADC Conversion Results bits

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
- n = Value at POR	’1’ = Bit is set	’0’ = Bit is cleared	x = Bit is unknown

REGISTER 9-3: ADC CONTROL REGISTER 1 (ADCON1: 9Fh)

U-0	U-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0
—	—	VCFG1	VCFG0	—	—	—	—
bit 7							bit 0

bit 7-6 **Unimplemented:** Read as ’0’

bit 5-4 **VCFG<1:0>:** Voltage Reference Configuration bits

00 = AVDD
01 = VREF1
10 = VR
11 = VDAC

bit 3-0 **Unimplemented:** Read as ’0’

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
- n = Value at POR	’1’ = Bit is set	’0’ = Bit is cleared	x = Bit is unknown

10.3 DAC Configuration

Example 10-1 shows a sample configuration for the DAC module. The port pin is configured, AVDD is selected for the voltage reference, and the DAC output is enabled.

EXAMPLE 10-1: DAC CONFIGURATION

```
;*  This code block will configure the DAC
;*  for AVDD Voltage Ref, and RB1/AN5/VDAC as
;*  output.

    BANKSEL TRISB          ; Select bank 1
    BSF     TRISB,1        ; Set RB1 input
    BSF     ANSEL,1        ; Set RB1 as analog

    BANKSEL DACON0         ; Select Bank 2
    CLRF    DAC            ; DAC to 00
    MOVLW   B'11000000'    ; Enable DAC output
    MOVWF   DACON0         ; Set REF = VDD

    MOVLW   DAC_VALUE
    MOVWF   DAC            ; Set DAC output
```

10.4 Effects of RESET

A device RESET forces all registers to their RESET state. This forces the following conditions:

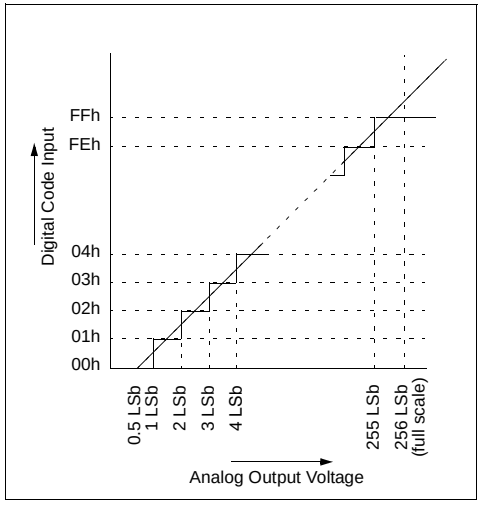
- DAC module is off
- Reference input to AVDD
- Output disabled
- DAC register is cleared

10.5 DAC Module Accuracy/Error

The accuracy/error specified for the DAC includes:

- Integral non-linearity error
- Differential non-linearity error
- Gain error
- Offset error
- Monotonicity

FIGURE 10-2: DAC TRANSFER FUNCTION



Offset error measures the first actual transition of a code versus the first ideal transition of a code. Offset error shifts the entire transfer function. Offset error can be calibrated out of a system or introduced into a system through the interaction of the output drive capability with the load impedance.

Gain error measures the maximum deviation of the last actual transition and the last ideal transition adjusted for offset error. This error appears as a change in slope of the transfer function. The difference in gain error to full scale error is that full scale does not take offset error into account. Gain error can be calibrated out by adjusting the reference voltage.

Linearity error refers to the uniformity of the voltage change with code change. Linearity errors cannot be calibrated out of the system. **Integral non-linearity error** measures the actual voltage output versus the ideal voltage output adjusted by the gain error for each code.

Differential non-linearity error measures the maximum actual voltage step versus the ideal voltage step. This measure is unadjusted.

TABLE 10-1: REGISTERS/BITS ASSOCIATED WITH DAC

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on All Other RESETS
11Fh	DACON0	DAON	DAOE	—	—	—	—	DARS1	DARS0	00-- --00	00-- --00
11Eh	DAC	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0	0000 0000	0000 0000
86h	TRISB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	1111 1111	1111 1111
9Dh	ANSEL	AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0	1111 1111	1111 1111

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used for DAC conversion.

FIGURE 12-1: COMPARATOR C1 SIMPLIFIED BLOCK DIAGRAM

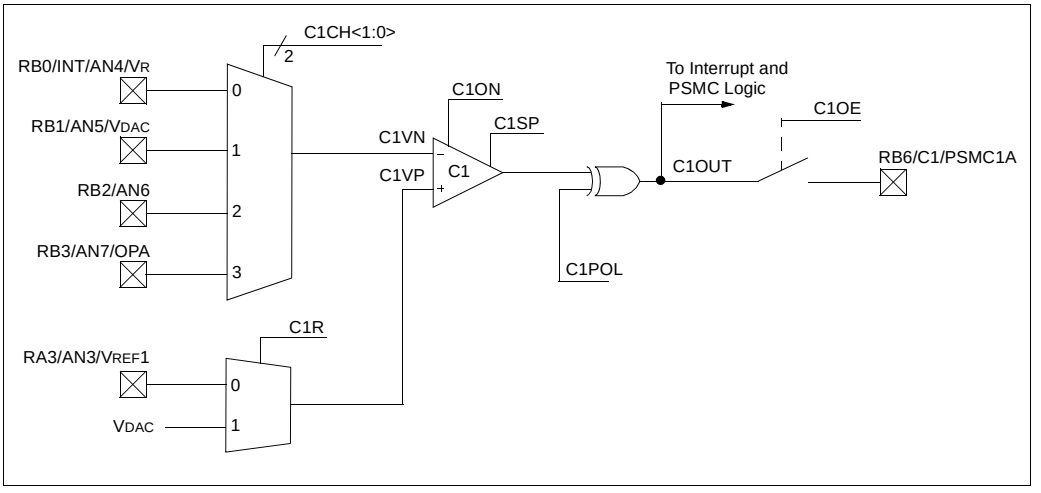
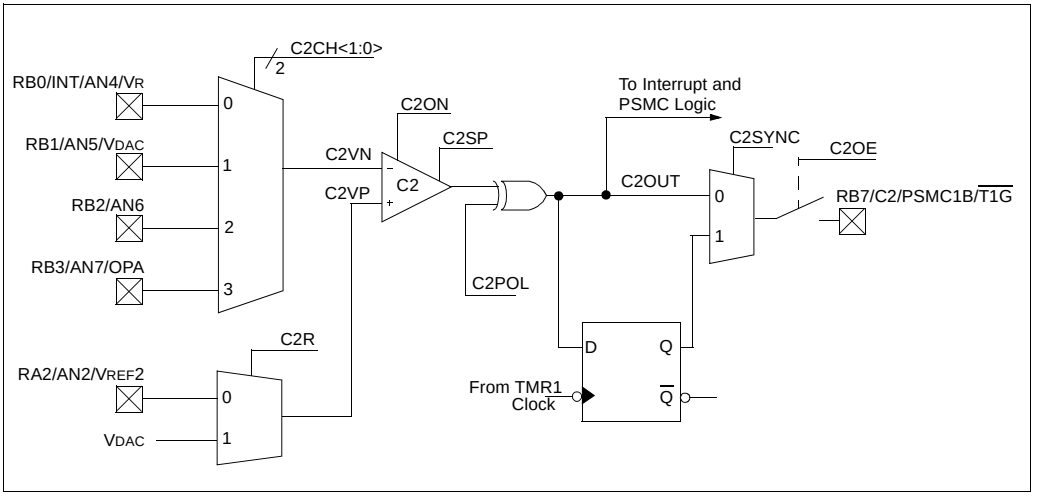


FIGURE 12-2: COMPARATOR C2 SIMPLIFIED BLOCK DIAGRAM



13.1.1 PULSE SKIP MODULATION (PSM)

In PSM (Pulse Skip Modulation), the PSMC operates as a fixed duty cycle pulse generator, with its output gated by the analog feedback (see Figure 13-3). Immediately prior to the initiation of a pulse, the analog feedback is sampled. If the comparator output = H, a pulse is initiated and held active for the programmed duty cycle. If the comparator output = L, no pulse is initiated and the PSMC waits for the start of the next pulse (see Table 13-3 and Table 13-4). In this mode, both the frequency and duty cycle of the output pulse are programmable. The analog feedback gates the presence or absence of the pulse on a pulse-by-pulse basis.

FIGURE 13-3: PSMC MODULE IN SINGLE OUTPUT PSM MODE (SIMPLIFIED BLOCK DIAGRAM)

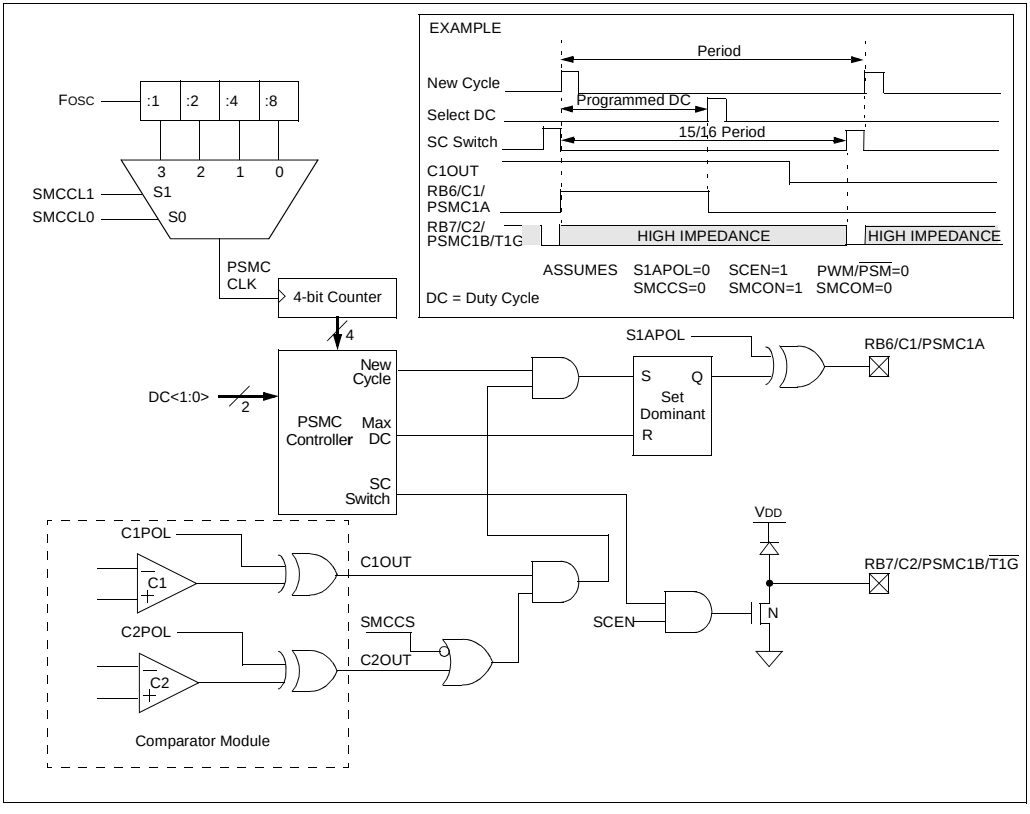


TABLE 13-3: PSMC1A OPERATION IN PSM MODE USING C1 COMPARATOR ONLY

Time	C1OUT	PSMC1A Output Signal
Beginning of PSM cycle	H	0 → 1
	L	0
During Pulse	x	No Change
		1
End of Pulse	x	1 → 0

Legend: x = Don't Care 0 = Inactive 1 = Active H = High L = Low

13.2 Control Registers

The PSMC is controlled by means of two special function registers: PSMCCON0 and PSMCCON1.

The PSMCCON0 register (Register 13-1) contains control bits for:

- Frequency of the output pulse
- Minimum and maximum duty cycle in PWM mode
- Fixed duty cycle in PSM mode

The PSMCCON1 register (Register 13-2) contains the control bits for:

- Enabling the PSMC module
- Setting the PSMC mode
- Configuring inputs and outputs

Note:	Following RESET, both the PSMC1A and PSMC1B outputs are held tri-state until the PSMC is configured. Driver circuitry for all power MOSFET transistors must have a resistor bias to turn off the transistor in the event of tri-state conditions, on either PSMC1A or PSMC1B, to prevent excessive stress on the MOSFET's and their associated circuitry.

13.2.1 PSMCCON0 REGISTER

The SMCCL<1:0> bits in the PSMCCON0 register, are used to set the pulse frequency of the PSMC.

Note:	Changing SMCCL<1:0> bits with the PSMC enabled (SMCON=1) can result in unpredictable output. Always disable PSMC before changing SMCCL<1:0>.

In the PWM mode, the MINDC <1:0> bits (PSMCCON0 <5:4>) specify the minimum duty cycle.

In the PWM mode, the MAXDC <1:0> bits (PSMCCON0 <3:2>) specify the maximum duty cycle limit.

In the PSM mode, the DC<1:0> bits (PSMCCON0<1:0>) specify the fixed duty cycle.

13.2.2 PSMCCON1 REGISTER

To enable the PSMC operation, the SMCON bit in the PSMCCON1 register must be set (see Register 13-2).

The PWM/$\overline{\text{PSM}}$ bit (PSMCCON1<1>) configures the output mode of the PSMC. When the PWM/$\overline{\text{PSM}}$ bit is set, the PSMC is configured for a PWM output. When the PWM/$\overline{\text{PSM}}$ bit is cleared, a fixed duty cycle pulse is output.

The SMCCS bit (PSMCCON1<0>) sets the input mode. When the SMCCS bit is set, the PSMC is configured for two inputs: C1 and C2. When cleared, only Comparator C1 is used.

SMCOM bit (PSMCCON1<1>) determines the number of outputs from the PSMC. When SMCOM is set, both PSMC1A and PSMC1B are active. When SMCOM is cleared, only the PSMC1A output is active and the PSMC1B output is available for another function.

S1APOL and S1BPOL control the polarity of the PSMC outputs. Setting the polarity bit configures the corresponding output for an active low state. Clearing the bit results in an active high output.

The SCEN bit (PSMCCON1<2>) enables the slope compensation output. When SCEN is set (and SMCOM is cleared) the PSMC1B output is configured to generate a slope compensation signal.

Note:	PSMC outputs must have their corresponding direction bits cleared in TRISB; TRISB<6>: for PSMC1A, and TRISB<7> for PSMC1B.

TABLE 13-5: PSMC OUTPUT MODES

FUNCTION	PSMC		PORTB	
	SMCOM	SCEN	TRISB<6>	TRISB<7>
Single Output	0	0	0	*
Single Output + Slope Compensation	0	1	0	0
Dual Output	1	x	0	0

Legend: x = Don't Care
*As needed for other functions (such as C2, RB7, $\overline{\text{T1G}}$).

EXAMPLE 13-2: EXAMPLE PSMC CONFIGURATION FOR A BUCK MODE SWITCHING POWER SUPPLY

```
;*  PSMC Initialization
;*  This code block will configure the PSMC
;*  and all additional peripherals for a buck
;*  mode switching power supply.
;*
;*  Order of configuration
;*  1.  PORTA/B I/O and analog configured
;*  2.  DAC enabled, configured, and preset
;*  3.  Op Amp enabled and configured
;*  4.  Comparator C1 enabled and configured
;*  5.  PSMC configured
;*  6.  PSMC enabled
;*****************************************
;*  This code block will configure all analog ports.
;
    BANKSEL     TRISA               ; Select Bank 1
    MOVLW       B'00001011'
    MOVWF       TRISA               ; Set RA0,1,& 3 as inputs
    MOVLW       B'11001110
    MOVWF       TRISB               ; Set RB1,2,3,6 & 7 as inputs
    MOVLW       B'11101011'
    MOVWF       ANSEL               ; Set AN0,1,3,5,6 & 7 as analog

;*****************************************************
;*  This code block will configure the DAC for VDD as
;*  DACREF, and RB1/AN5/VDAC as an output.

    BANKSEL         DACON0              ; Select Bank 2

    CLRF            DAC                 ; Set DAC to safe value
    MOVLW           B'11000000'         ; Enable DAC, output
    MOVWF           DACON0              ;   and set DACREF = VDD

    MOVLW           OUTPUT_VALUE
    MOVWF           DAC                 ; Set dAC output level

;*****************************************************
;*  This code block will configure the OPA module
;*  as an Op Amp, with a 3 MHZ GBWP

    MOVLW           B'10000001'         ; Set Op Amp mode and
    MOVWF           OPACON              ;  2 MHz GBWP

;*****************************************************
;*  This code block will configure Comparator C1
;*  for normal speed and output polarity,
;*  input on AN6, and Reference from the VREF1

    MOVLW           B'10001010'         ; Set C1; no ext out, norm
    MOVWF           CM1CON0             ;  speed & pol, VREF1, AN6

;*****************************************************
;*  This code block will configure the PSMC module
;*  for PWM, Fosc/128, Single input, Single output
;*  Non-inverting out, DC min = 0%, DC max = 50%

    MOVLW           B'0000000'
    MOVWF           PSMCCON0            ; Set DCmin 0, DCmax 50, Fosc/128
    MOVLW           B'00000110'
    MOVWF           PSMCCON1            ; Set PWM, 1 in, 2 out, noninvert
    BSF             PSMCCON1,SMCON      ; Enable PSMC
```

NOTES:

14.0 SPECIAL FEATURES OF THE CPU

These devices have a host of features intended to maximize system reliability, minimize cost through elimination of external components, provide power saving operating modes and offer code protection. These features include:

- Oscillator selection
- RESET
  - Power-on Reset (POR)
  - Power-up Timer (PWRT)
  - Oscillator Start-up Timer (OST)
  - Programmable Brown-out Reset (PBOR)
- Interrupts
- Watchdog Timer (WDT)
- Programmable Low Voltage Detection (PLVD)
- SLEEP
- Code protection
- ID locations
- In-Circuit Serial Programming™ (ICSP™)

Several oscillator options are available to allow the part to fit the application. The INTRC oscillator options save system cost while the LP crystal option saves power. A set of configuration bits is used to select various options.

The CPU also features a Watchdog Timer (WDT), which can be enabled either through a configuration bit during programming, or by the software. For added reliability, the WDT runs off its own internal RC oscillator instead of the main CPU clock.

In addition to the WDT, the CPU incorporates both an Oscillator Start-up Timer and a Power-up Timer. The Oscillator Start-up Timer (OST) is intended to hold the chip in RESET until the crystal oscillator has stabilized. The Power-up Timer (PWRT) holds the CPU in a fixed RESET delay of 72ms (nominal) on Power-up Resets (POR and PBOR), while the power supply stabilizes. With these two timers on-chip, most applications need no external RESET circuitry.

SLEEP mode is designed to offer a very low current power-down mode. The user can awaken from SLEEP through:

- External RESET
- Watchdog Timer Wake-up
- Interrupt

Additional information on special features is available in the PIC Mid-Range Reference Manual, (DS33023).

14.1 Configuration Bits

The configuration bits can be programmed (read as '0'), or left unprogrammed (read as '1'), to select various device configurations. These bits are mapped in program memory location 2007h.

Note:	Address 2007h is beyond the user program memory space, which can be accessed only during programming.

Some of the core features provided may not be necessary for each application in which a device may be used. The configuration word bits allow these features to be configured/enabled/disabled as necessary. These features include:

- Code Protection
- PBOR Trip Point
- Power-up Timer
- Watchdog Timer
- Device Oscillator Mode

As can be seen in Table 14-1, some additional configuration word bits have been provided for Brown-out Reset trip point selection.

TABLE 15-2: PIC16CXXX INSTRUCTION SET

Mnemonic, Operands		Description	Cycles	14-Bit Opcode MSb LSb	Status Affected	Notes
BYTE-ORIENTED FILE REGISTER OPERATIONS						
ADDWF	f, d	Add W and f	1	00 0111 dfff ffff	C,DC,Z	1,2
ANDWF	f, d	AND W with f	1	00 0101 dfff ffff	Z	1,2
CLRF	f	Clear f	1	00 0001 lfff ffff	Z	2
CLRW	-	Clear W	1	00 0001 0000 0011	Z	
COMF	f, d	Complement f	1	00 1001 dfff ffff	Z	1,2
DECF	f, d	Decrement f	1	00 0011 dfff ffff	Z	1,2
DECFSZ	f, d	Decrement f, Skip if 0	1(2)	00 1011 dfff ffff		1,2,3
INCF	f, d	Increment f	1	00 1010 dfff ffff	Z	1,2
INCFSZ	f, d	Increment f, Skip if 0	1(2)	00 1111 dfff ffff		1,2,3
IORWF	f, d	Inclusive OR W with f	1	00 0100 dfff ffff	Z	1,2
MOVF	f, d	Move f	1	00 1000 dfff ffff	Z	1,2
MOVWF	f	Move W to f	1	00 0000 lfff ffff		
NOP	-	No Operation	1	00 0000 0xx0 0000		
RLF	f, d	Rotate Left f through Carry	1	00 1101 dfff ffff	C	1,2
RRF	f, d	Rotate Right f through Carry	1	00 1100 dfff ffff	C	1,2
SUBWF	f, d	Subtract W from f	1	00 0010 dfff ffff	C,DC,Z	1,2
SWAPF	f, d	Swap nibbles in f	1	00 1110 dfff ffff		1,2
XORWF	f, d	Exclusive OR W with f	1	00 0110 dfff ffff	Z	1,2
BIT-ORIENTED FILE REGISTER OPERATIONS						
BCF	f, b	Bit Clear f	1	01 00bb bfff ffff		1,2
BSF	f, b	Bit Set f	1	01 01bb bfff ffff		1,2
BTFSC	f, b	Bit Test f, Skip if Clear	1 (2)	01 10bb bfff ffff		3
BTFSS	f, b	Bit Test f, Skip if Set	1 (2)	01 11bb bfff ffff		3
LITERAL AND CONTROL OPERATIONS						
ADDLW	k	Add literal and W	1	11 111x kkkk kkkk	C,DC,Z	
ANDLW	k	AND literal with W	1	11 1001 kkkk kkkk	Z	
CALL	k	Call subroutine	2	10 0kkk kkkk kkkk		
CLRWDT	-	Clear Watchdog Timer	1	00 0000 0110 0100	$\overline{TO}$,$\overline{PD}$	
GOTO	k	Go to address	2	10 1kkk kkkk kkkk		
IORLW	k	Inclusive OR literal with W	1	11 1000 kkkk kkkk	Z	
MOVLW	k	Move literal to W	1	11 00xx kkkk kkkk		
RETFIE	-	Return from interrupt	2	00 0000 0000 1001		
RETLW	k	Return with literal in W	2	11 01xx kkkk kkkk		
RETURN	-	Return from Subroutine	2	00 0000 0000 1000		
SLEEP	-	Go into standby mode	1	00 0000 0110 0011	$\overline{TO}$,$\overline{PD}$	
SUBLW	k	Subtract W from literal	1	11 110x kkkk kkkk	C,DC,Z	
XORLW	k	Exclusive OR literal with W	1	11 1010 kkkk kkkk	Z	

Note 1: When an I/O register is modified as a function of itself (e.g., `MOVF PORTB, 1`), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.

2: If this instruction is executed on the TMR0 register (and, where applicable, d = 1), the prescaler will be cleared if assigned to the Timer0 Module.

3: If the Program Counter (PC) is modified or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a `NOP`.

XORWF	Exclusive OR W with f
Syntax:	[*label*] XORWF f,d
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	(W) .XOR. (f) $\rightarrow$ (destination)
Status Affected:	Z
Description:	Exclusive OR the contents of the W register with register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.

17.2 DC Characteristics: Input/Output Pins

TABLE 17-2: DC CHARACTERISTICS: PIC16C781/782, DSTEMP (INDUSTRIAL)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial and Operating voltage VDD range as described in DC spec Section 17-1				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
		Input Low Voltage					
	VIL	I/O ports:					
D030		with TTL buffer	VSS	—	0.15VDD	V	For entire VDD range
D030A			VSS	—	0.8V	V	4.5V ≤ VDD ≤ 5.5V
D031		with Schmitt Trigger buffer	VSS	—	0.2VDD	V	For entire VDD range
D032		$\overline{MCLR}$	VSS	—	0.2VDD	V	
D033		OSC1 (in XT, HS, LP and EC)	VSS	—	0.3 VD	V	
		Input High Voltage					
	VIH	I/O ports:		—			
D040		with TTL buffer	2.0	—	VDD	V	4.5V ≤ VDD ≤ 5.5V
D040A			(0.25VDD + 0.8V)	—	VDD	V	For entire VDD range
D041		with Schmitt Trigger buffer	0.8VDD	—	VDD	V	For entire VDD range
D042		$\overline{MCLR}$	0.8VDD	—	VDD	V	
D042A		OSC1 (XT, HS, LP and EC)	0.7VDD	—	VDD	V	
D070	IPURB	**PORTB Weak Pull-up Current Per Pin**	50	250	400	µA	VDD = 5V, VPIN = VSS
		Input Leakage Current(1,2)					
D060	IIL	I/O ports (with digital functions)	—	—	±1	µA	Vss ≤ VPIN ≤ VDD, Pin at hi-impedance
D060A	IIL	I/O ports (with analog functions)	—	—	±100	nA	Vss ≤ VPIN ≤ VDD, Pin at hi-impedance
D061		RA5/$\overline{MCLR}$/VPP	—	—	±5	µA	Vss ≤ VPIN ≤ VDD
D063		OSC1	—	—	±5	µA	Vss ≤ VPIN ≤ VDD, XT, HS, LP and EC osc configuration
		Output Low Voltage					
D080	VOL	I/O ports (Includes CLKOUT)	—	—	0.6	V	IOL = 8.5 mA, VDD = 4.5V
		Output High Voltage					
D090	VOH	I/O ports(2) (Includes CLKOUT)	VDD - 0.7	—	—	V	IOH = -3.0 mA, VDD = 4.5V
D150*	VOD	**Open Drain High Voltage**	—	—	10.5	V	RA4 pin
		Capacitive Loading Specs on Output Pins*					
D100	Cosc2	OSC2 pin	—	—	15	pF	In XT, HS and LP modes when external clock is used to drive OSC1.
D101	CIO	All I/O pins and OSC2 (in RC mode)	—	—	50	pF	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

2: Negative current is defined as current sourced by the pin.

17.7 Analog Peripherals Characteristics

17.7.1 BANDGAP VOLTAGE

Bandgap voltage is used as the reference voltage in the PBOR, PLVD, Auto Calibration, and VR modules

FIGURE 17-10: BANDGAP START-UP TIME

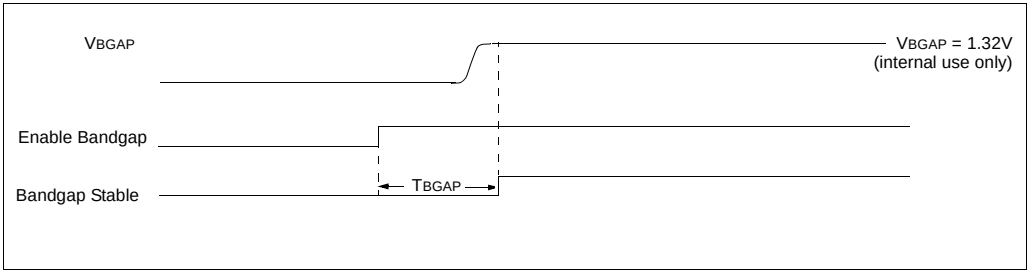


TABLE 17-14: BANDGAP START-UP TIME

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
36*	TBGAP	Bandgap start-up time	—	30	—	µs	Defined as the time between the instant that the bandgap is enabled and the moment that the bandgap reference voltage is stable.

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

17.7.2 VR MODULE

TABLE 17-15: DC CHARACTERISTICS: VR

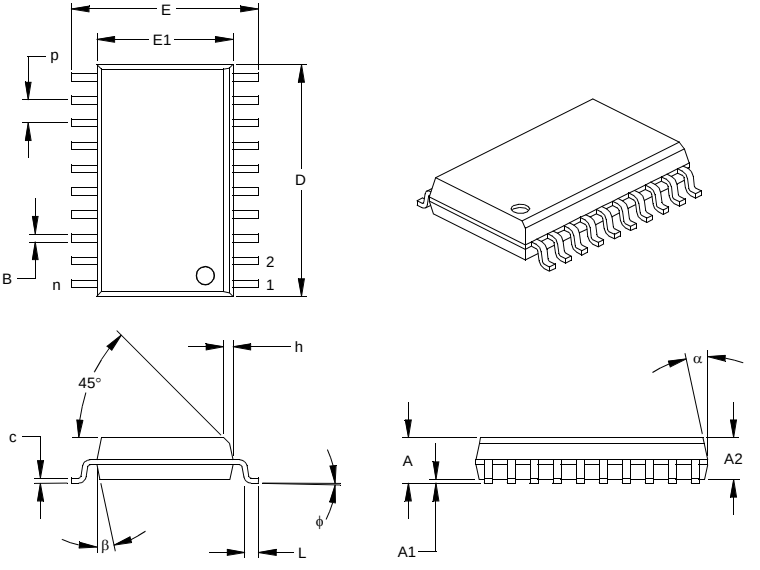
DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated): Operating temperature -40°C ≤ TA ≤ +85°C for industrial Operating voltage VDD as described in Section 17.1				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
D400	VR	Output Voltage	—	3.072	—	V	VDD ≥ 3.5V
D402*	TCVOUT	Output Voltage Temperature Coefficient	—	TBD	TBD	ppm/°C	
D404*	IVREFSO	External Load Source	—	—	5	mA	
D405*	IVREFSI	External Load Sink	—	—	-5	mA	
	CL*	External Capacitor Load	—	—	200	pF	
D406*	DVOUT/ DIOUT	Load Regulation	—	1	TBD	mV/mA	ISOURCE = 0 mA to 5 mA
			—	1	TBD		ISINK = 0 mA to 5 mA
D407*	DVOUT/ DVDD	Supply Regulation	—	—	1	mV/V	

* These parameters are characterized but not tested.

† Data in “Typ” column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

20-Lead Plastic Small Outline (SO) – Wide, 300 mil (SOIC)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		20			20	
Pitch	p		.050			1.27	
Overall Height	A	.093	.099	.104	2.36	2.50	2.64
Molded Package Thickness	A2	.088	.091	.094	2.24	2.31	2.39
Standoff §	A1	.004	.008	.012	0.10	0.20	0.30
Overall Width	E	.394	.407	.420	10.01	10.34	10.67
Molded Package Width	E1	.291	.295	.299	7.39	7.49	7.59
Overall Length	D	.496	.504	.512	12.60	12.80	13.00
Chamfer Distance	h	.010	.020	.029	0.25	0.50	0.74
Foot Length	L	.016	.033	.050	0.41	0.84	1.27
Foot Angle	ϕ	0	4	8	0	4	8
Lead Thickness	c	.009	.011	.013	0.23	0.28	0.33
Lead Width	B	.014	.017	.020	0.36	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.
JEDEC Equivalent: MS-013
Drawing No. C04-094

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NOTES: