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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	13
Program Memory Size	1.75KB (1K x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 8x8b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	20-DIP (0.300", 7.62mm)
Supplier Device Package	20-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lc781-i-p

Peripheral Features (Continued):

- Dual Analog Comparator module with:
  - Individual enable and interrupt bits
  - Programmable speed and output polarity
  - Fully configurable inputs and outputs
  - Reference from DAC, or VREF1/VREF2
  - Low input offset voltage.
- VR voltage reference module:
  - 3.072V +/- 0.7% @25°C, AVDD = 5V
  - Configurable output to ADC reference, DAC reference, and VR pin
  - 5 mA sink/source
- Programmable Switch Mode Controller module:
  - PWM and PSM modes
  - Programmable switching frequency
  - Configurable for either single or dual feedback inputs
  - Configurable single or dual outputs
  - Slope compensation output available in single output mode

Key Features PIC® Mid-Range Reference Manual (DS33023)	PIC16C781	PIC16C782
Operating Frequency	DC - 20 MHz	DC - 20 MHZ
RESETS (and Delays)	POR, BOR, $\overline{\text{MCLR}}$, WDT (PWRT, OST)	POR, BOR, $\overline{\text{MCLR}}$, WDT (PWRT, OST)
Program Memory (14 bit words)	1K	2K
Data Memory (bytes)	128	128
Interrupts	8	8
I/O Ports	13 + 3 Input only	13 + 3 Input only
Timers	2	2
Programmable Switch Mode Controller	1	1
8-bit Analog-to-Digital Module	1	1
ADC channels	8 External, 2 Internal	8 External, 2 Internal
8-bit Digital-to-Analog Module	1	1
Comparators	2	2
Comparator Channels	4 (AN<7:4>)	4 (AN<7:4>)
Operational Amplifier	1	1
Voltage Reference	1	1
Brown-out Reset	Yes	Yes
Programmable Low Voltage Detect	Yes	Yes
Instruction Set	35 Instructions	35 Instructions

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TABLE 2-1: PIC16C781/782 SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Details on Page:
Bank 2											
100h(2)	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								0000 0000	23
101h	TMR0	Timer0 Module's Register								xxxx xxxx	51
102h(2)	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	23
103h(2)	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	17
104h(2)	FSR	Indirect Data Memory Address Pointer								xxxx xxxx	23
105h	—	Unimplemented								—	—
106h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx 0000	35
107h	—	Unimplemented								—	—
108h	—	Unimplemented								—	—
109h	—	Unimplemented								—	—
10Ah(1,2)	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter					---0 0000	23
10Bh(2)	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	19
10Ch	PMDATL	PMD7	PMD6	PMD5	PMD4	PMD3	PMD2	PMD1	PMD0	0000 0000	48
10Dh	PMADRL	PMA7	PMA6	PMA5	PMA4	PMA3	PMA2	PMA1	PMA0	xxxx xxxx	48
10Eh	PMDATH	—	—	PMD13	PMD12	PMD11	PMD10	PMD9	PMD8	--00 0000	47
10Fh	PMADRH	—	—	—	Reserved	Reserved	PMA10	PMA9	PMA8	---x xxxx	48
110h	CALCON	CAL	CALERR	CALREF	—	—	—	—	—	000- ----	85
111h	PSMCCON0	SMCCL1	SMCCL0	MINDC1	MINDC0	MAXDC1	MAXDC0	DC1	DC0	0000 0000	104
112h	PSMCCON1	SMCON	S1APOL	S1BPOL	—	SCEN	SMCOM	PWM/$\overline{PSM}$	SMCCS	000- 0000	104
113h	—	Unimplemented								—	—
114h	—	Unimplemented								—	—
115h	—	Unimplemented								—	—
116h	—	Unimplemented								—	—
117h	—	Unimplemented								—	—
118h	—	Unimplemented								—	—
119h	CM1CON0	C1ON	C1OUT	C1OE	C1POL	C1SP	C1R	C1CH1	C1CH0	0000 0000	91
11Ah	CM2CON0	C2ON	C2OUT	C2OE	C2POL	C2SP	C2R	C2CH1	C2CH0	0000 0000	93
11Bh	CM2CON1	MC1OUT	MC2OUT	—	—	—	—	—	C2SYNC	00-- ---0	94
11Ch	OPACON	OPAON	CMPEN	—	—	—	—	—	GBWP	00-- ---0	84
11Dh	—	Unimplemented								—	—
11Eh	DAC	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0	0000 0000	79
11Fh	DACON0	DAON	DAOE	—	—	—	—	DARS1	DARS0	00-- --00	79

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0'.
Shaded locations are unimplemented, read as '0'.

Note 1: The upper byte of the program counter is not directly accessible. PCLATH is a holding register for the PC<12:8> whose contents are transferred to the upper byte of the program counter. See Section 2.9 for more detail.

2: These registers can be addressed from any bank.

2.4 OPTION_REG Register

The OPTION_REG register is a readable and writable register which contains various control bits to configure:

- TMR0 prescaler/WDT postscaler (single assignable register known also as the prescaler)
- External INT interrupt
- TMR0
- Weak pull-ups on PORTB

Note: To achieve a 1:1 prescaler assignment for the TMR0 register, assign the prescaler to the Watchdog Timer.

REGISTER 2-2: OPTION REGISTER (OPTION_REG: 81h, 181h)

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
$\overline{\text{RBPU}}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0
bit7							bit0

bit 7 **$\overline{\text{RBPU}}$:** PORTB Pull-up Enable bit(1)
1 = PORTB weak pull-ups are disabled
0 = PORTB weak pull-ups are enabled by the WPUB register

bit 6 **INTEDG:** Interrupt Edge Select bit
1 = Interrupt on rising edge of RB0/INT pin
0 = Interrupt on falling edge of RB0/INT pin

bit 5 **T0CS:** TMR0 Clock Source Select bit
1 = Transition on RA4/T0CKI pin
0 = Internal instruction cycle clock (FOSC/4)

bit 4 **T0SE:** TMR0 Source Edge Select bit
1 = Increment on high-to-low transition on RA4/T0CKI pin
0 = Increment on low-to-high transition on RA4/T0CKI pin

bit 3 **PSA:** Prescaler Assignment bit
1 = Prescaler is assigned to the WDT
0 = Prescaler is assigned to the Timer0 module

bit 2-0 **PS<2:0>:** Prescaler Rate Select bits

Bit Value	TMR0 Rate	WDT Rate
000	1 : 2	1 : 1
001	1 : 4	1 : 2
010	1 : 8	1 : 4
011	1 : 16	1 : 8
100	1 : 32	1 : 16
101	1 : 64	1 : 32
110	1 : 128	1 : 64
111	1 : 256	1 : 128

Note 1: Individual weak pull-ups on RB pins can be enabled/disabled from the weak pull-up PORTB register (WPUB).

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

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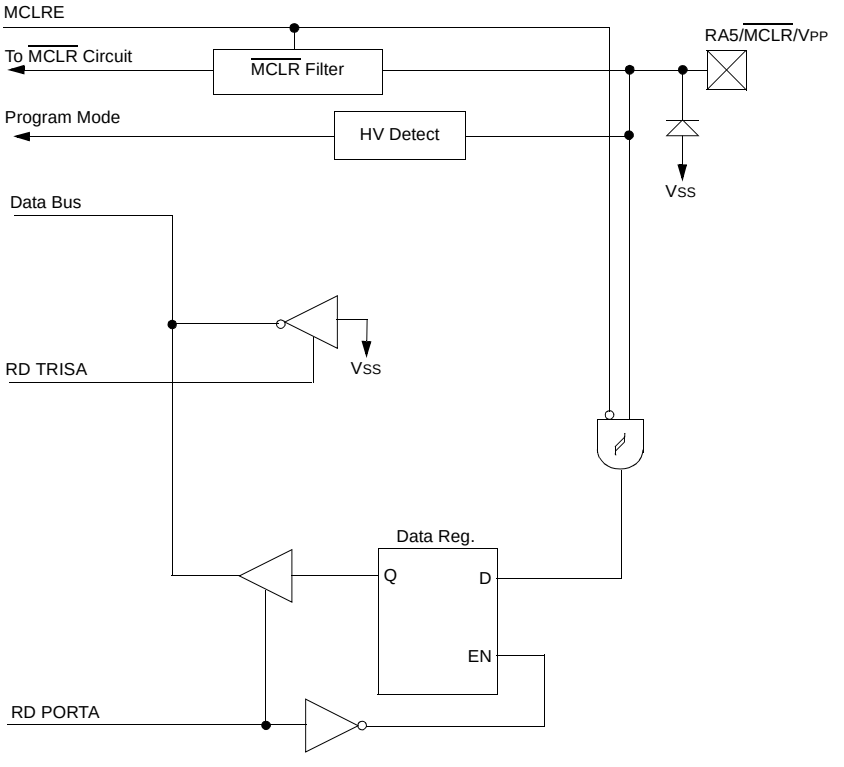
FIGURE 3-6: BLOCK DIAGRAM OF RA5/$\overline{\text{MCLR}}$/VPP PIN



MCLRE(1)	TRISA<5>	FUNCTION	PORTA<5> READ
Internal	x	Digital In	Pin
External	x	$\overline{\text{MCLR}}$	0

Note 1: See Configuration Word <5>, Register 14-1.

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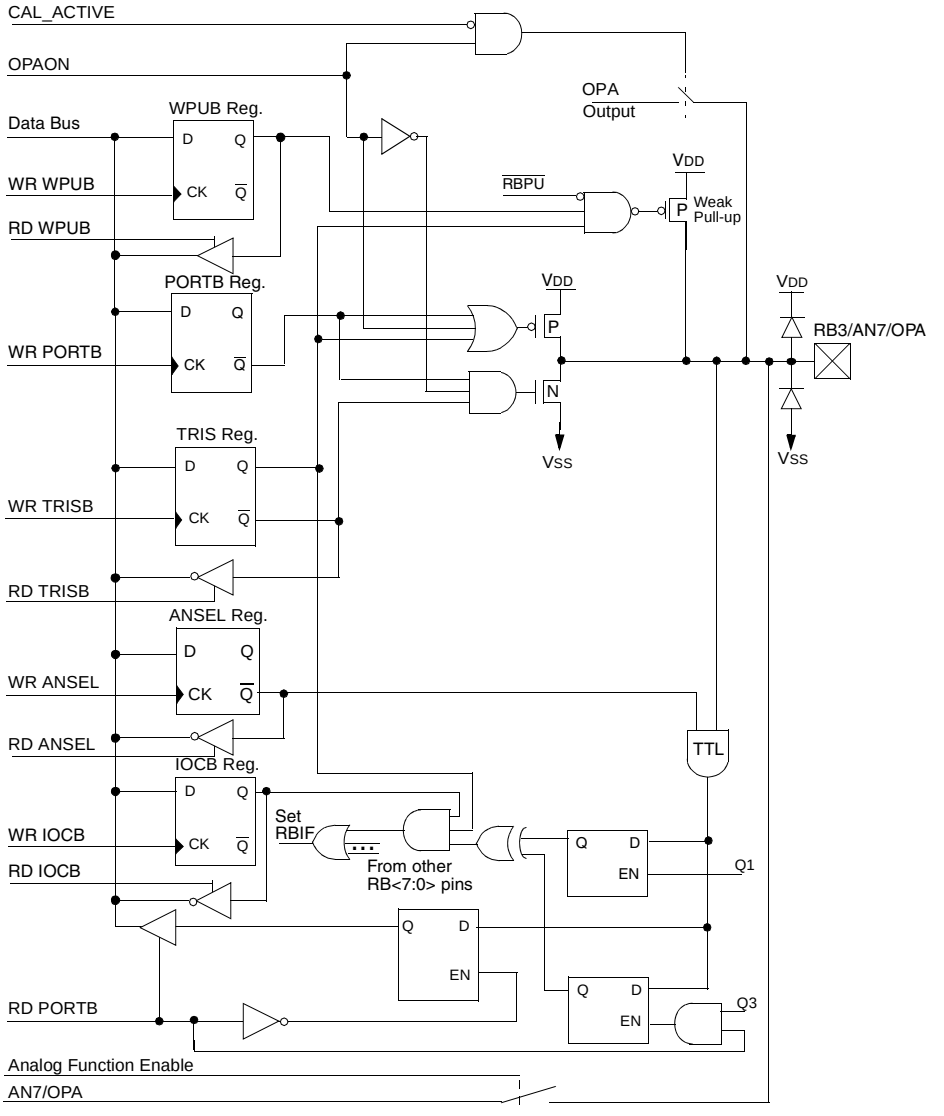
FIGURE 3-12: BLOCK DIAGRAM OF RB3/AN7/OPA PIN



OPA MODULE		ANSEL<7>	ADC/C1/C2 INPUT	FUNCTION	PORTB<3> READ
OPAON	CAL_ACTIVE				
0	x	0	Digital	Digital I/O	Pin
0	x	1	Analog	Analog In	0
1	0	1	Analog	OPA Output	0
1	1	1	Analog HI-Z	Calibration	0

Analog HI-Z = No internal drive on pin (analog input) during calibration.

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5.0 TIMER0 MODULE

The Timer0 module timer/counter has the following features:

- 8-bit timer/counter
- Readable and writable
- Internal or external clock select
- Edge select for external clock
- 8-bit software programmable prescaler
- Interrupt on overflow from FFh to 00h

Figure 5-1 is a simplified block diagram of the Timer0 module.

Additional information on timer modules is available in the PIC Mid-Range Reference Manual, (DS33023).

5.1 Timer0 Operation

Timer0 can operate as either a timer or a counter.

Programming Timer0 is via the OPTION register (see Register 2-2).

Timer0 mode is selected by clearing/setting the bit T0CS (OPTION_REG<5>). In Timer mode (T0CS = 0), the Timer0 module increments every instruction cycle (without prescaler). If the TMR0 register is written, the increment is inhibited for the following two instruction cycles. The user can work around this by writing an adjusted value to the TMR0 register.

Counter mode is selected by setting bit T0CS (OPTION_REG<5>). In Counter mode, Timer0 increments either on every rising, or falling edge of pin RA4/T0CKI. The incrementing edge is determined by the Timer0 Source Edge Select bit T0SE (OPTION_REG<4>). Clearing bit T0SE selects the rising edge, setting selects the falling edge. Restrictions on the external clock input are discussed below.

When an external clock input is used for Timer0, it must meet certain requirements. The requirements ensure the external clock can be synchronized with the internal system clock. Also, there is a delay in the actual incrementing of Timer0 after synchronization.

Additional information on external clock requirements is available in the PIC Mid-Range Reference Manual, (DS33023).

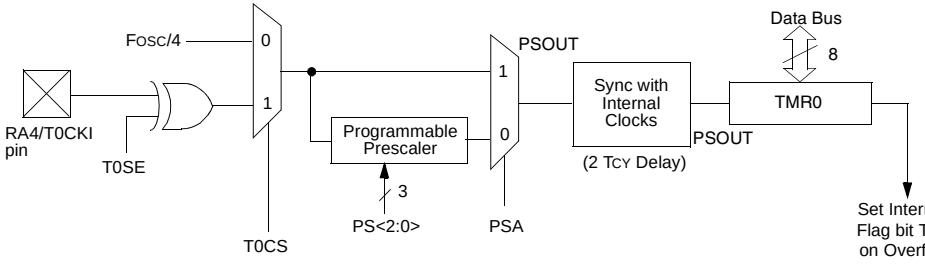
EXAMPLE 5-1: INITIALIZING TIMER0

```
;* This code block will configure Timer0
;* for Polling, internal clock & 1:16
;*  prescaler
;*
;* Wait for TMR0 overflow code included
    BANKSEL     TMR0            ; Select Bank 0
    CLRF        TMR0            ; Clear Timer0
                                ; Register

    BANKSEL     OPTION_REG      ; Select Bank 1

    MOVLW       B'11000011'     ; INT on L2H
    MOVWF       OPTION_REG      ; Internal clk,
                                ; pscaler 1:16
*****************************************
;*  Wait for TMR0 overflow
;*
T0_OVFL_WAIT
    TBFSS       INTCON,T0IF     ; Check for TMR0
                                ; overflow
    GOTO        T0_OVFL_WAIT    ; If clear, test
                                ; again
    BCF         INTCON,T0IF     ; Clear interrupt
```

FIGURE 5-1: TIMER0 BLOCK DIAGRAM



Note 1: T0CS, T0SE, PSA, PS<2:0> (OPTION_REG<5:0>).
2: The prescaler is shared with Watchdog Timer (refer to Figure 5-2 for detailed block diagram).

5.2 Prescaler

An 8-bit counter is available as a prescaler for the Timer0 module, or as a postscaler for the Watchdog Timer, respectively (Figure 5-2). For simplicity, this counter is referred to as “prescaler” throughout this data sheet.

Note:	There is only one prescaler available which is mutually exclusively shared between the Timer0 module and the Watchdog Timer. Thus, a prescaler assignment for the Timer0 module means that there is no prescaler for the Watchdog Timer, and vice-versa.

The prescaler is not readable or writable.

The PSA and PS<2:0> bits (OPTION_REG<3:0>) determine the prescaler assignment and prescale ratio.

Clearing bit PSA assigns the prescaler to the Timer0 module. When the prescaler is assigned to the Timer0 module, prescale values of 1:2, 1:4, ..., 1:256 are selectable.

Setting bit PSA assigns the prescaler to the Watchdog Timer (WDT). When the prescaler is assigned to the WDT, prescale values of 1:1, 1:2, ..., 1:128 are selectable.

When assigned to the Timer0 module, all instructions writing to the TMR0 register (e.g., `CLRF TMR0, MOVWF TMR0, BSF TMR0, x....etc`.) will clear the prescaler. When assigned to WDT, a `CLRWDT` instruction clears the prescaler along with the WDT.

Note:	Writing to TMR0 when the prescaler is assigned to Timer0 clears the prescaler count, but does not change the prescaler assignment.

5.2.1 SWITCHING PRESCALER ASSIGNMENT

The prescaler assignment is fully under software control, i.e., it can be changed “on-the-fly” during program execution.

Note:	To avoid an unintended device RESET, a specific instruction sequence (shown in the PIC Mid-Range Reference Manual, DS33023) must be executed when changing the prescaler assignment from Timer0 to the WDT. This sequence must be followed even if the WDT is disabled.

5.3 Timer0 Interrupt

The TMR0 interrupt is generated when the TMR0 register overflows from FFh to 00h. This overflow sets bit T0IF (INTCON<2>). The interrupt can be masked by clearing bit T0IE (INTCON<5>). Bit T0IF must be cleared in software by the Timer0 module Interrupt Service Routine before re-enabling this interrupt. The TMR0 interrupt cannot awaken the processor from SLEEP, since the timer is shut-off during SLEEP.

5.4 Effects of RESET

A device RESET will program Timer0 for an external clock input on RA4/T0CKI, Hi-Low edge, and no prescaler. The TMR0 register is not cleared.

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NOTES:

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11.2 Configuration as OPAMP or Comparator

The following example demonstrates calibration of the OPA module as an Operational Amplifier.

EXAMPLE 11-1: CALIBRATION FOR OPAMP MODE

```
;*  This code block will configure the OPA
;*  module as an Op Amp, 2 MHz GBWP, and
;*  calibrated for a common mode voltage of
;*  1.2V. Routine returns w=0 if
;*  calibration good.

    BANKSEL     OPACON       ; Select Bank 2
    MOVLW       B'10000001'  ; Op Amp mode &
    MOVWF       OPACON       ; 2 MHz GBWP

    BCF         CALCON,CALREF; Set 1.2V
    BSF         CALCON,CAL   ; Start

CAL_LOOP
    BTFSC       CALCON,CAL   ; Test for end
    GOTO        CAL_LOOP     ; If not, wait
    MOVLW       ERROR_FLAG
    BTFSS       CALCON,CALERR; Test for error
    CLRW                     ; If no, return 0
    RETURN
```

The following example demonstrates how to configure and calibrate the OPA module as a Voltage Comparator.

EXAMPLE 11-2: CALIBRATION FOR COMPARATOR MODE

```
;*  This code block will configure the OPA
;*  module as a voltage comparator, slow
;*  speed, and calibrated for a common mode
;*  voltage of 2.5 V (assumes VDD=5V).
;*  Routine returns w=0 if calibration good.

    BANKSEL     OPACON       ; Select Bank 2
    MOVLW       B'10000000'
    MOVWF       OPACON       ; Op Amp mode,
                             ; slow
    BSF         CALCON,CALREF; Common mode=DAC

    MOVLW       H'0x80'
    MOVWF       DAC          ; DAC at VDD/2
    MOVLW       B'10000000'
    MOVWF       DACON0       ; enable DAC,
                             ; VDD ref
    BSF         CALCON,CAL   ; Start
CAL_LOOP
    BTFSC       CALCON,CAL   ; Test for end
    GOTO        CAL_LOOP     ; If not, wait

    MOVLW       ERROR_FLAG
    BTFSS       CALCON,CALERR; Test for error
    CLRW                     ; If no, return 0
    BSF         OPACON,CMPEN ; Comparator mode
    RETURN
```

11.3 Effects of RESET

A device RESET forces all registers to their RESET state. This disables the OPA module and clears any calibration.

11.4 OPA Module Performance

Common AC and DC performance specifications for the OPA module:

- Common Mode Voltage Range
- Leakage Current
- Input Offset Voltage
- Open Loop Gain
- Gain Bandwidth Product

Common mode voltage range is the specified voltage range for the OPA+ and OPA- inputs, for which the OPA module will perform to within its specifications. The OPA module is designed to operate with input voltages between 0 and V_{DD}-1.4V. Behavior for Common mode voltages greater than V_{DD}-1.4V, or below 0V, are not guaranteed.

Leakage current is a measure of the small source or sink currents on the OPA+ and OPA- inputs. To minimize the effect of leakage currents, the effective impedances connected to the OPA+ and OPA- inputs should be kept as small as possible and equal.

Input offset voltage is a measure of the voltage difference between the OPA+ and OPA- inputs in a closed loop circuit with the OPA in its linear region. The offset voltage will appear as a DC offset in the output equal to the input offset voltage, multiplied by the gain of the circuit. The input offset voltage is also affected by the Common mode voltage. The OPA has an automatic calibration module which can minimize the input offset voltage of the module.

Open loop gain is the ratio of the output voltage to the differential input voltage, (OPA+) - (OPA-). The gain is greatest at DC and falls off with frequency.

Gain Bandwidth Product or GBWP is the frequency at which the open loop gain falls off to 0 dB. The lower GBWP is optimized for systems requiring low frequency response and low power consumption.

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FIGURE 13-2: PSMC MODULE IN DUAL ALTERNATING OUTPUT PWM MODE (SIMPLIFIED BLOCK DIAGRAM)

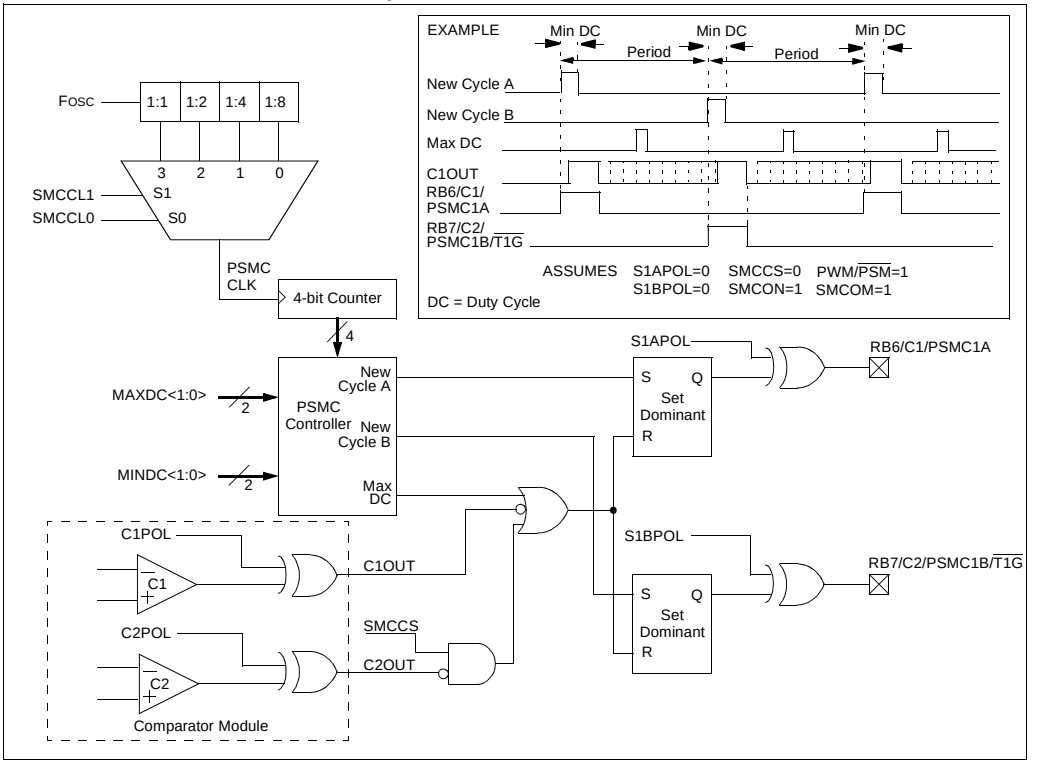

TABLE 13-1: PSMC1A OUTPUT SEQUENCE IN PWM MODE USING C1 COMPARATOR ONLY

Time	MINDC<1:0>	C1OUT	PSMC1A Output Signal
Beginning of PWM cycle	00	H	0 → 1
		L	0
	non-zero	x	0 → 1
During Min Duty Cycle	non-zero	x	1
After Min Duty Cycle, Before Max Duty Cycle	x	H → L	q→ 0
		L → H	0
Max Duty Cycle	x	x	q→ 0

Legend: x = Don't Care q = Prior State 0 = Inactive 1 = Active H = High L = Low

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13.1.1 PULSE SKIP MODULATION (PSM)

In PSM (Pulse Skip Modulation), the PSMC operates as a fixed duty cycle pulse generator, with its output gated by the analog feedback (see Figure 13-3). Immediately prior to the initiation of a pulse, the analog feedback is sampled. If the comparator output = H, a pulse is initiated and held active for the programmed duty cycle. If the comparator output = L, no pulse is initiated and the PSMC waits for the start of the next pulse (see Table 13-3 and Table 13-4). In this mode, both the frequency and duty cycle of the output pulse are programmable. The analog feedback gates the presence or absence of the pulse on a pulse-by-pulse basis.

FIGURE 13-3: PSMC MODULE IN SINGLE OUTPUT PSM MODE (SIMPLIFIED BLOCK DIAGRAM)

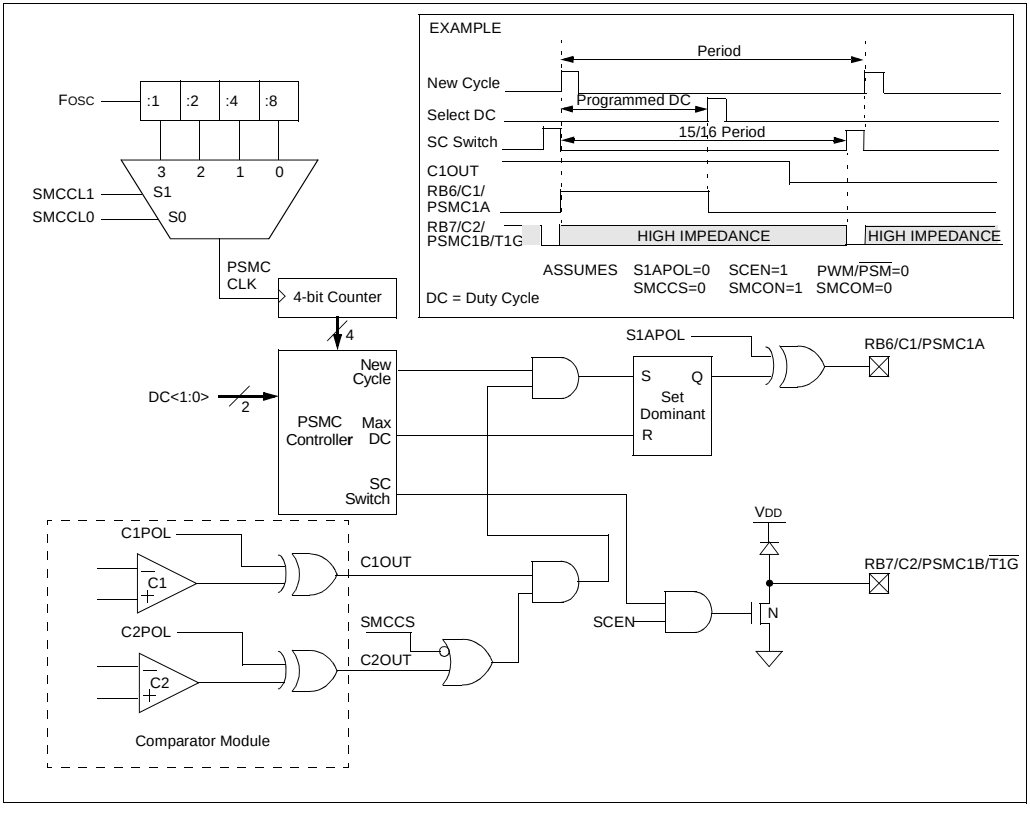

TABLE 13-3: PSMC1A OPERATION IN PSM MODE USING C1 COMPARATOR ONLY

Time	C1OUT	PSMC1A Output Signal
Beginning of PSM cycle	H	0 → 1
	L	0
During Pulse	x	No Change
		1
End of Pulse	x	1 → 0

Legend: x = Don't Care 0 = Inactive 1 = Active H = High L = Low

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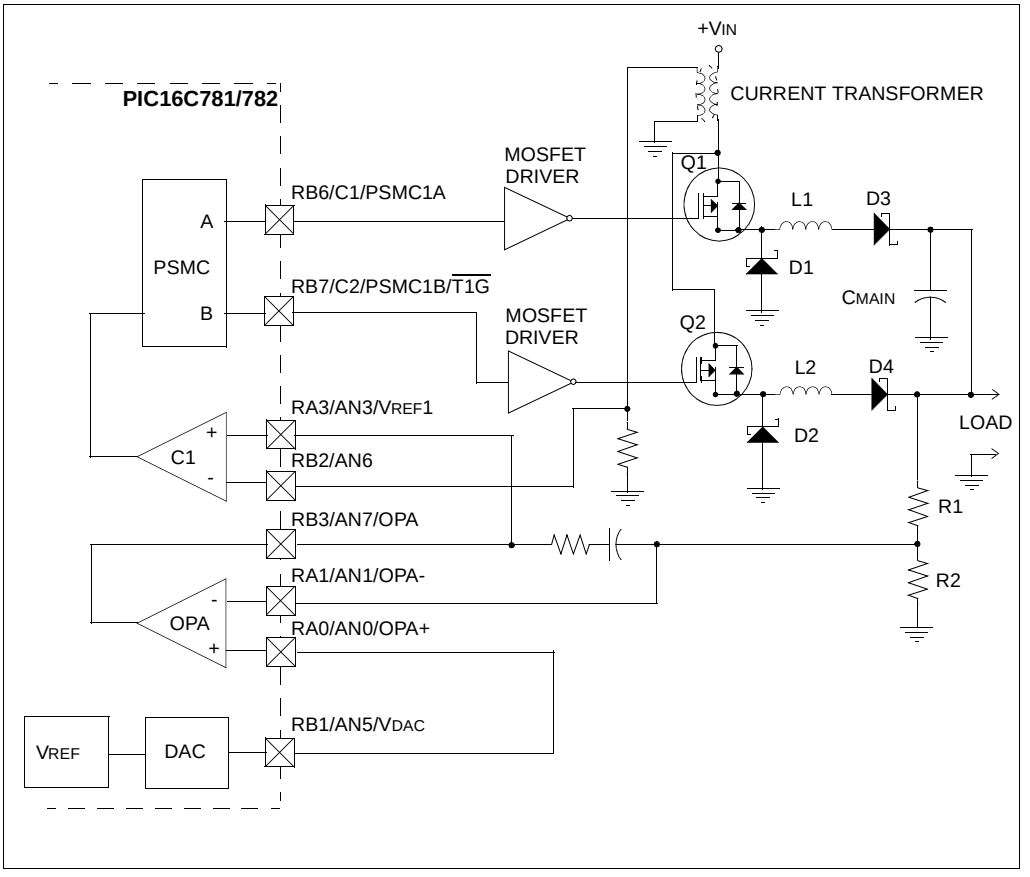
FIGURE 13-6: EXAMPLE BUCK CONFIGURATION LC POWER SUPPLY



13.3.3 EXAMPLE MOTOR SPEED CONTROL

In Figure 13-7, the PSMC acts as a speed control for a brushless DC motor. The direction of the current in the motor winding is set by feedback from a Hall effect position sensor on the motor. The sensor switches the phase in the motor in response to the rotation of the rotor so that the magnetic field rotates just ahead of the rotor, pulling it in the desired direction. The speed at which the rotor spins is a function of the mechanical load on the rotor and the current in the field winding.

Speed control is accomplished by monitoring the speed via the Hall effect sensor and regulating the current in the winding appropriately. The winding current is regulated by the PSMC to be proportional to the value supplied by the DAC module. The feedback loop is closed by software making periodic measurement of the rotor speed using the Hall Effect sensor/Timer1 and adjusting the output value of the DAC appropriately.

The algorithm (used to determine the values output by the DAC module) depends on:

- mechanical system connected to the motor
- motor characteristics
- characteristics of the high current drive

An analysis of the mechanics of the system and the design of an appropriate control algorithm is beyond the scope of this Data Sheet. Therefore, the designer should consult a text dealing with the design of motor speed controls and feedback control system, in general, for the necessary design guidance.

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13.4 Effects of SLEEP and RESET

A device RESET forces all registers to their RESET state. This disables the PSMC and resets its outputs to digital inputs. It is good design practice to include a fail-safe resistor bias in all power transistor drive circuitry. The fail-safe circuit should disable the power device when the PSMC output drive transistor is held tri-state. This protects the power device and its associated circuitry from the stress of prolonged operation without feedback.

Placing the PIC16C781/782 into SLEEP mode will stop the main oscillator for the microcontroller. The PSMC derives its timing from the main oscillator. Therefore, operation of the PSMC will halt when the microcontroller enters SLEEP mode. To prevent damage, the outputs of the PSMC are gated so that they are driven to their inactive state whenever the device enters SLEEP mode. When the microcontroller wakes up, the PSMC resumes operation per its previously programmed configuration.

TABLE 13-6: REGISTERS ASSOCIATED WITH THE PSMC

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other RESETS
86h,186h	TRISB	PORTB Data Direction Register								1111 1111	1111 1111
11Ah	CM2CON0	C2ON	C2OUT	C2OE	C2POL	C2SP	C2R	C2CH1	C2CH0	0000 0000	0000 0000
119h	CM1CON0	C1ON	C1OUT	C1OE	C1POL	C1SP	C1R	C1CH1	C1CH0	0000 0000	0000 0000
111h	PSMCCON0	SMCCL1	SMCCL0	MINDC1	MINDC0	MAXDC1	MAXDC0	DC1	DC0	0000 0000	0000 0000
112h	PSMCCON1	SMCON	S1APOL	S1BPOL	—	SCEN	SMCOM	PWM/$\overline{\text{PSM}}$	SMCCS	000- 0000	000- 0000

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used for PSMC.

14.0 SPECIAL FEATURES OF THE CPU

These devices have a host of features intended to maximize system reliability, minimize cost through elimination of external components, provide power saving operating modes and offer code protection. These features include:

- Oscillator selection
- RESET
  - Power-on Reset (POR)
  - Power-up Timer (PWRT)
  - Oscillator Start-up Timer (OST)
  - Programmable Brown-out Reset (PBOR)
- Interrupts
- Watchdog Timer (WDT)
- Programmable Low Voltage Detection (PLVD)
- SLEEP
- Code protection
- ID locations
- In-Circuit Serial Programming™ (ICSP™)

Several oscillator options are available to allow the part to fit the application. The INTRC oscillator options save system cost while the LP crystal option saves power. A set of configuration bits is used to select various options.

The CPU also features a Watchdog Timer (WDT), which can be enabled either through a configuration bit during programming, or by the software. For added reliability, the WDT runs off its own internal RC oscillator instead of the main CPU clock.

In addition to the WDT, the CPU incorporates both an Oscillator Start-up Timer and a Power-up Timer. The Oscillator Start-up Timer (OST) is intended to hold the chip in RESET until the crystal oscillator has stabilized. The Power-up Timer (PWRT) holds the CPU in a fixed RESET delay of 72ms (nominal) on Power-up Resets (POR and PBOR), while the power supply stabilizes. With these two timers on-chip, most applications need no external RESET circuitry.

SLEEP mode is designed to offer a very low current power-down mode. The user can awaken from SLEEP through:

- External RESET
- Watchdog Timer Wake-up
- Interrupt

Additional information on special features is available in the PIC Mid-Range Reference Manual, (DS33023).

14.1 Configuration Bits

The configuration bits can be programmed (read as '0'), or left unprogrammed (read as '1'), to select various device configurations. These bits are mapped in program memory location 2007h.

Note:	Address 2007h is beyond the user program memory space, which can be accessed only during programming.

Some of the core features provided may not be necessary for each application in which a device may be used. The configuration word bits allow these features to be configured/enabled/disabled as necessary. These features include:

- Code Protection
- PBOR Trip Point
- Power-up Timer
- Watchdog Timer
- Device Oscillator Mode

As can be seen in Table 14-1, some additional configuration word bits have been provided for Brown-out Reset trip point selection.

14.3 RESET

The PIC16C781/782 devices have several different RESETS. These RESETS are grouped into two classifications: power-up and non power-up. The power-up type RESETS are the Power-on and Brown-out Resets, which assume the device VDD was below its normal operating range for the device's configuration. The non power-up type RESETS assume normal operating limits were maintained before/during and after the RESET.

- Power-on Reset (POR)
- Programmable Brown-out Reset (PBOR)
- Non Power-up ($\overline{MCLR}$) Reset during normal operation
- $\overline{MCLR}$ Reset during SLEEP
- WDT Reset (during normal operation)

Some registers are not affected in any RESET condition. Their status is unknown on a Power-up Reset and unchanged in any other RESET. Most other registers are placed into an initialized state upon RESET. However, they are not affected by a WDT Reset during SLEEP, because this is considered a WDT Wake-up, which is viewed as the resumption of normal operation.

Several status bits have been provided to indicate which RESET occurred (see Table 14-4). See Table 14-5 for a full description of RESET states of special registers.

A simplified block diagram of the On-Chip Reset Circuit is shown in Figure 14-4.

These devices have a $\overline{MCLR}$ noise filter in the $\overline{MCLR}$ Reset path. The filter detects and ignores small pulses.

It should be noted that a WDT Reset does not drive $\overline{MCLR}$ pin low.

FIGURE 14-4: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT

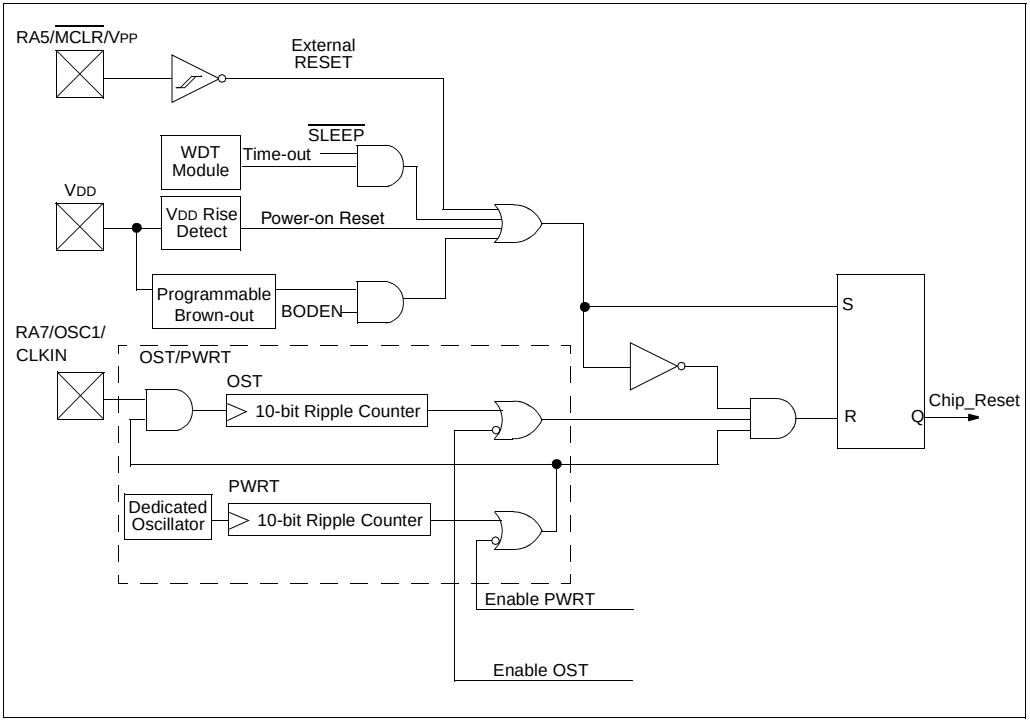

TABLE 14-6: INITIALIZATION CONDITION FOR ALL REGISTERS

Register	Power-On Reset or Brown-Out Reset	$\overline{\text{MCLR}}$ Reset or WDT Reset	Wake-up via WDT or Interrupt
W (not a mapped register)	xxxx xxxx	uuuu uuuu	uuuu uuuu
INDF	0000 0000	uuuu uuuu	uuuu uuuu
TMR0	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCL	0000 0000	0000 0000	PC + 1(1)
STATUS	0001 1xxx	000q quuu(2)	uuuq quuu(2)
FSR	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTA	xxxx 0000	uuuu 0000	uuuu uuuu
PORTB	xxxx xx00	uuuu uu00	uuuu uu00
PCLATH	---0 0000	---0 0000	---u uuuu
INTCON	0000 000x	0000 000u	uuuu uuqq
PIR1	0000 ---0	0000 ---0	0000 ---u
CALCON	000- ----	000- ----	uuu- ----
TMR1L	xxxx xxxx	uuuu uuuu	uuuu uuuu
TMR1H	xxxx xxxx	uuuu uuuu	uuuu uuuu
T1CON	-000 0000	-uuu uuuu	-uuu uuuu
PSMCCON0	0000 0000	0000 0000	uuuu uuuu
PSMCCON1	000- 0000	000- 0000	uuu- uuuu
CM1CON0	0000 0000	0000 0000	uuuu uuuu
CM2CON0	0000 0000	0000 0000	uuuu uuuu
CM2CON1	00-- ---0	00-- ---0	uu-- ---u
OPACON	00-- ---0	00-- ---0	uu-- ---u
ADRES	xxxx xxxx	uuuu uuuu	uuuu uuuu
ADCON0	0000 0000	0000 0000	uuuu uuuu
OPTION_REG	1111 1111	1111 1111	uuuu uuuu
TRISA	1111 1111	1111 1111	uuuu uuuu
TRISB	1111 1111	1111 1111	uuuu uuuu
PIE1	0000 ---0	0000 ---0	uuuu ---u
PCON	---0 1-qq	---0 1-uu	---u u-uu
DAC	0000 0000	0000 0000	uuuu uuuu
DACON0	00-- --00	00-- --00	uu-- --uu
WPUB	1111 1111	1111 1111	uuuu uuuu
IOCB	1111 0000	1111 0000	uuuu uuuu
REFCON	---- 00--	---- 00--	---- uu--
LVDCON	--00 0101	--00 0101	--uu uuuu
ANSEL	1111 1111	1111 1111	uuuu uuuu
ADCON1	--00 ----	--00 ----	--uu ----
PMDATL	xxxx xxxx	uuuu uuuu	uuuu uuuu
PMADRL	xxxx xxxx	uuuu uuuu	uuuu uuuu
PMDATH	--xx xxxx	--uu uuuu	--uu uuuu
PMADRH	---- xxxx	---- uuuu	---- uuuu
PMCON1	1--- ---0	1--- ---0	1--- ---0

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as '0', q = value depends on condition

Note 1: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

2: See Table 14-5 for RESET value for specific condition.

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15.1 Instruction Descriptions

ADDLW	Add Literal and W
Syntax:	[*label*] ADDLW k
Operands:	$0 \le k \le 255$
Operation:	(W) + k → (W)
Status Affected:	C, DC, Z
Description:	The contents of the W register are added to the eight bit literal 'k' and the result is placed in the W register.

ADDWF	Add W and f
Syntax:	[*label*] ADDWF f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	(W) + (f) → (destination)
Status Affected:	C, DC, Z
Description:	Add the contents of the W register with register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.

ANDLW	AND Literal with W
Syntax:	[*label*] ANDLW k
Operands:	$0 \le k \le 255$
Operation:	(W) .AND. (k) → (W)
Status Affected:	Z
Description:	The contents of W register are AND'ed with the eight bit literal 'k'. The result is placed in the W register.

ANDWF	AND W with f
Syntax:	[*label*] ANDWF f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	(W) .AND. (f) → (destination)
Status Affected:	Z
Description:	AND the W register with register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.

BCF	Bit Clear f
Syntax:	[*label*] BCF f,b
Operands:	$0 \le f \le 127$ $0 \le b \le 7$
Operation:	0 → (f<b>)
Status Affected:	None
Description:	Bit 'b' in register 'f' is cleared.

BSF	Bit Set f
Syntax:	[*label*] BSF f,b
Operands:	$0 \le f \le 127$ $0 \le b \le 7$
Operation:	1 → (f<b>)
Status Affected:	None
Description:	Bit 'b' in register 'f' is set.

BTFSS	Bit Test f, Skip if Set
Syntax:	[*label*] BTFSS f,b
Operands:	$0 \le f \le 127$ $0 \le b < 7$
Operation:	skip if (f<b>) = 1
Status Affected:	None
Description:	If bit 'b' in register 'f' is '0', the next instruction is executed. If bit 'b' is '1', then the next instruction is discarded and a NOP is executed instead, making this a 2TCY instruction.

NOTES:

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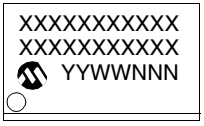
19.0 PACKAGING INFORMATION

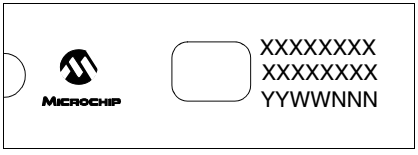
19.1 Package Marking Information

20-Lead SSOP

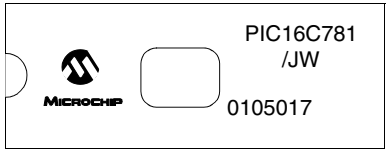


Example

20-Lead CERDIP Windowed

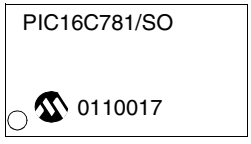


Example

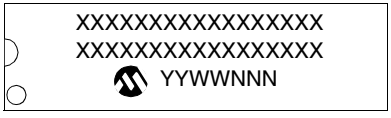


20-Lead SOIC

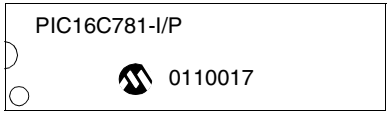
Example



20-Lead PDIP



Example



Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

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