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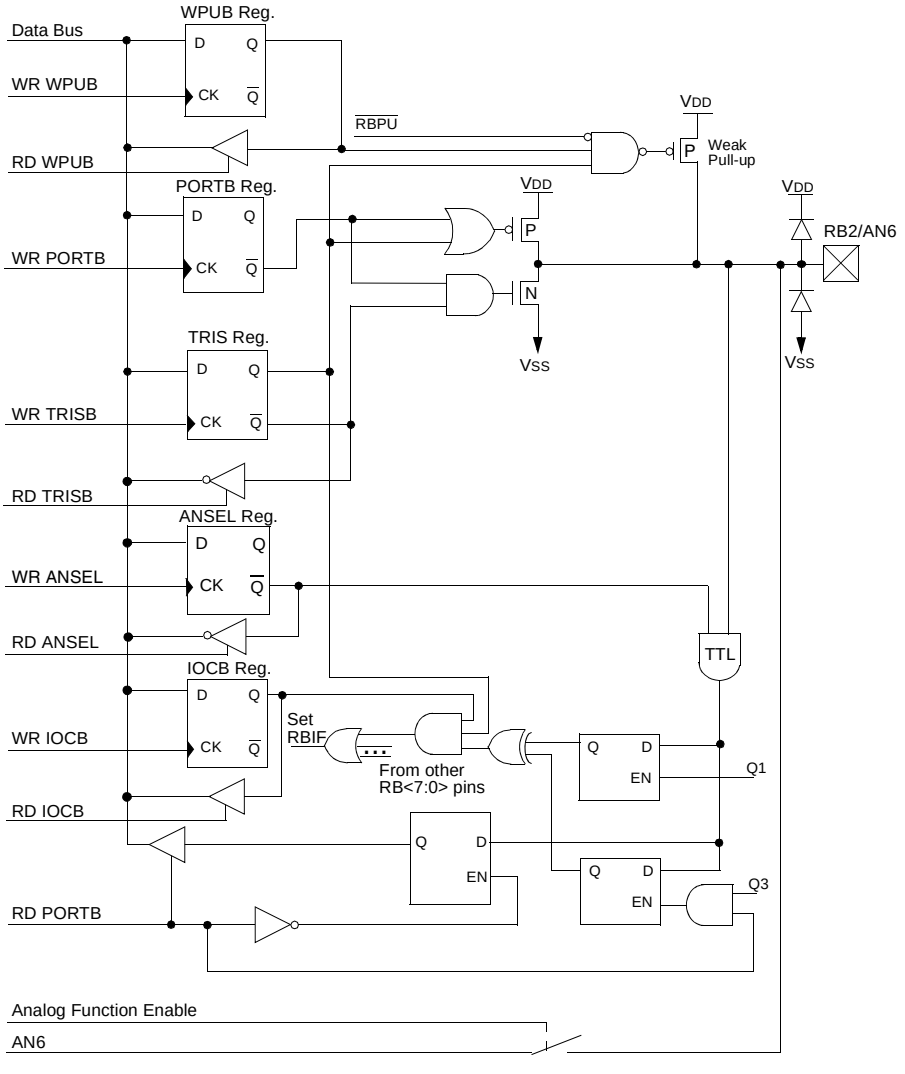
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	13
Program Memory Size	1.75KB (1K x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 8x8b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	20-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lc781-i-so

FIGURE 3-11: BLOCK DIAGRAM OF RB2/AN6 PIN



ANSEL<6>	TRISB<2>	FUNCTION	PORTB<2> READ
0	1	Digital In	Pin
0	0	Digital Out	Pin
1	x	Analog In	0

4.4 Program Memory Read With Code Protect Set

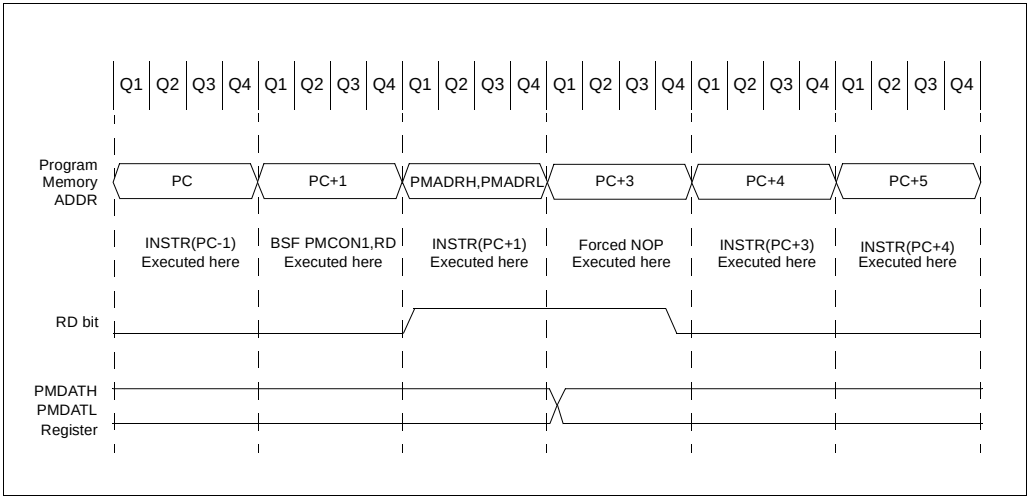
When the device is code protected, the CPU can still perform the program memory read function.

TABLE 4-1: SUMMARY OF REGISTERS ASSOCIATED WITH PMR

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other RESETS
10Ch	PMDATL	PMD7	PMD6	PMD5	PMD4	PMD3	PMD2	PMD1	PMD0	0000 0000	0000 0000
10Dh	PMADRL	PMA7	PMA6	PMA5	PMA4	PMA3	PMA2	PMA1	PMA0	xxxx xxxx	uuuu uuuu
10Eh	PMDATH	—	—	PMD13	PMD12	PMD11	PMD10	PMD9	PMD8	--00 0000	--00 0000
10Fh	PMADRH	—	—	—	Reserved	Reserved	PMA10	PMA9	PMA8	---x xxxx	---u uuuu
18Ch	PMCON1	Reserved	—	—	—	—	—	—	RD	1--- ---0	1--- ---0

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by PMR.

FIGURE 4-1: PROGRAM MEMORY READ CYCLE EXECUTION



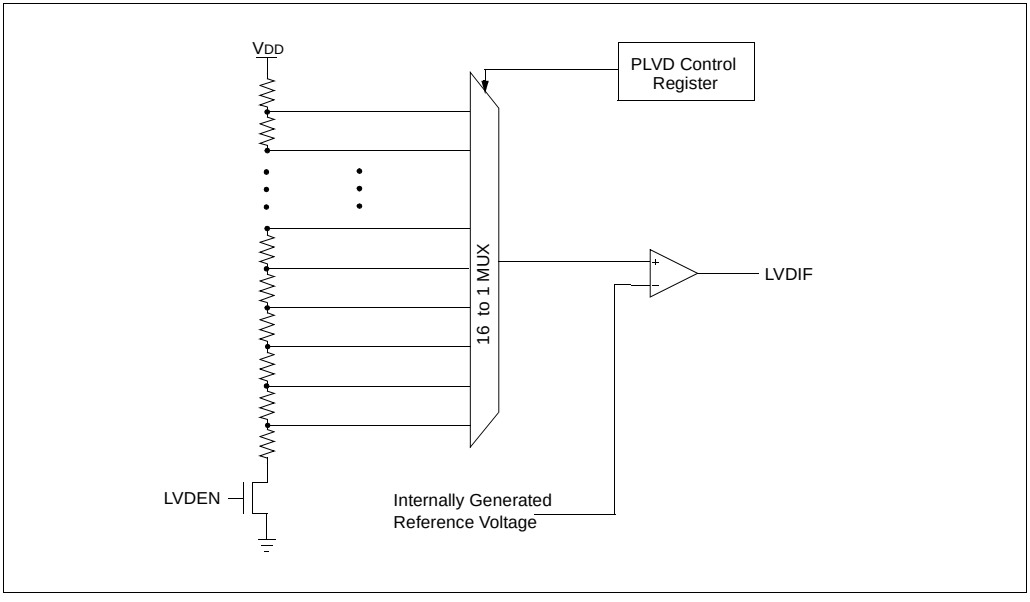
8.2 Operation

The PLVD indicates a low voltage condition by setting the LVDIF bit in the PIR1 register. Once set by the PLVD module, the LVDIF bit will remain set until cleared by software. For proper indication of a low voltage condition, the user should clear this bit prior to testing.

To test for a low voltage condition, the PLVD module compares the divided output of VDD against an internal bandgap reference. The PLVD module automatically enables this reference whenever it is enabled and provides a stability bit, BGST, to indicate when it has stabilized. The bandgap reference is also enabled by other modules within the PIC16C781/782 as part of their operation. Other modules using the bandgap include the following:

- VR module
- BOR module
- OPA calibration module

FIGURE 8-2: LOW VOLTAGE DETECT BLOCK DIAGRAM



REGISTER 8-1: PROGRAMMABLE LOW VOLTAGE DETECT REGISTER (LVDCON: 9Ch)

U-0	U-0	R-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-1
—	—	BGST	LVDEN	LV3	LV2	LV1	LV0
bit 7							bit 0

bit 7-6 **Unimplemented:** Read as '0'

bit 5 **BGST:** Internal Reference Voltage Stable Flag bit
1 = Reference is stable
0 = Reference is not stable

bit 4 **LVDEN:** Low Voltage Detect Power Enable bit
1 = Enables PLVD, powers up LVD circuit
0 = Disables PLVD, powers down LVD circuit.

bit 3-0 **LV<3:0>:** Low Voltage Detection Limit bits
1111 = Reserved
1110 = 4.5V typical
1101 = 4.2V typical
1100 = 4.0V typical
1011 = 3.8V typical
1010 = 3.6V typical
1001 = 3.5V typical
1000 = 3.3V typical
0111 = 3.0V typical
0110 = 2.8V typical
0101 = 2.7V typical
0100 = 2.5V typical
0011 = Below valid operating voltage
0010 = Below valid operating voltage
0001 = Below valid operating voltage
0000 = Below valid operating voltage

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
- n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

9.2 Configuring the ADC Module

9.2.1 CONFIGURING ANALOG PORT PINS

The ANSEL and TRISB registers control the operation of the ADC port pins. The port pins to be used as analog inputs must have their corresponding TRISB bits set (= 1). The proper ANSEL bits must also be set (analog input) to disable the digital input buffer.

Note 1: The ADC operation is independent of the state of the TRISB or ANSEL bits. These bits must be configured by the firmware prior to initiation of an ADC conversion.

2: When reading the PORTA or PORTB registers, all pins configured as analog input channels will read as a '0'.

3: Analog levels on any pin that is defined as a digital input, including AN<7:0>, may cause the input buffer to consume excess supply current.

9.2.2 CONFIGURING THE REFERENCE VOLTAGES

The VCFG<5:4> bits in the ADCON1 register configure the ADC module reference voltage input, ADCREF. The reference input can come from any of the following:

- Internal voltage reference (VR)
- External comparator C1 reference (VREF1)
- DAC output (VDAC)
- Analog positive supply (AVDD)

If an external reference is chosen for the ADCREF input, the port pin that multiplexes with the incoming external reference must also be configured as an analog input.

9.2.3 SELECTING THE ADC CONVERSION CLOCK

The ADC conversion cycle requires 9.5TAD. The source of the ADC conversion clock is software selectable. The four possible options for ADC clock are:

- FOSC/2
- FOSC/8
- FOSC/32
- ADRC (clock derived from a dedicated internal RC oscillator)

For correct ADC conversion, the ADC conversion clock (TAD) must be selected to ensure a minimum TAD time of 1.6 μsec. Table 9-1 shows the resultant TAD times derived from the device operating frequencies and the ADC clock source selected.

TABLE 9-1: TAD vs. DEVICE OPERATING FREQUENCIES: PIC16C781/782

ADC Clock Source (TAD)		Device Frequency			
Operation	**ADCS1:ADCS0**	**20 MHz**	**5 MHz**	**1.25 MHz**	**333.33kHz**
2 TOSC	00	100 ns(2)	400 ns(2)	1.6 s	6 μs
8 TOSC	01	400 ns	1.6 μs	6.4 μs	24 μs(3)
32 TOSC	10	1.6 μs	6.4 μs	25.6 μs(3)	96 μs(3)
RC	11	2 - 6 μs(1,4)	2 - 6 μs(1,4)	2 - 6 μs(1,4)	2 - 6 μs(1)

Legend: Shaded cells are outside of recommended range.

Note 1: The RC source has a typical TAD time of 4 μs.

2: These values violate the minimum required TAD time.

3: For faster conversion times, the selection of another clock source is recommended.

4: When device frequency is greater than 1 MHz, the RC ADC conversion clock source is recommended for SLEEP operation only.

REGISTER 11-1: OPAMP CONTROL REGISTER (OPACON: 11Ch)

R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0	R/W-0
OPAON	CMPEN	—	—	—	—	—	GBWP
bit 7							bit 0

bit 7 **OPAON:** OPAMP Enable bit
1 = OPAMP is enabled
0 = OPAMP is disabled

bit 6 **CMPEN:** Comparator Mode Enable bit
1 = Comparator mode
0 = OPAMP mode

bit 5-1 **Unimplemented:** Read as '0'

bit 0 **GBWP:** Gain Bandwidth Product Select bits
1 = 2 MHz typ. (fast mode)
0 = 70 kHz typ. (slow mode)

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

11.1.2 CALCON REGISTER

The Automatic Calibration Module (ACM) is an internal state machine which performs an input offset voltage calibration (trim) on the OPA module (see Figure 11-2). Calibration is initiated by setting the CAL bit (CALCON<7>). Upon completion of the calibration sequence, the ACM will clear the CAL bit.

If a problem arises in the calibration process, the CALERR flag (CALCON<6>) will be set to indicate the failure to calibrate.

Setting CALREF (CALCON<5>) forces calibration at a common mode voltage specified by the output of the DAC module. The DAC module must be enabled prior to calibration. Clearing CALREF will perform the calibration with a common mode voltage of 1.2V. The output pin floats during calibration.

Note 1: Auto Calibration must be performed while the module is configured as an OPAMP (CMPEN = 0). Performing Auto Calibration function in the Comparator mode may yield unpredictable results.

2: If the internal 1.2V reference is used for the common mode voltage during Auto Calibration, CALREF = 0 (CALCON<5>), a delay for reference stabilization must be observed before start of calibration.

3: The OPA module shares pins with the ADC module. Performing ADC conversions on the OPA+ or OPA- pins may affect OPAMP stability.

4: When using the DAC as a reference for calibration, CALREF = 1 (CALCON<5>), the V_{DAC} voltage must be within the specified common mode voltage for the OPAMP.

FIGURE 12-1: COMPARATOR C1 SIMPLIFIED BLOCK DIAGRAM

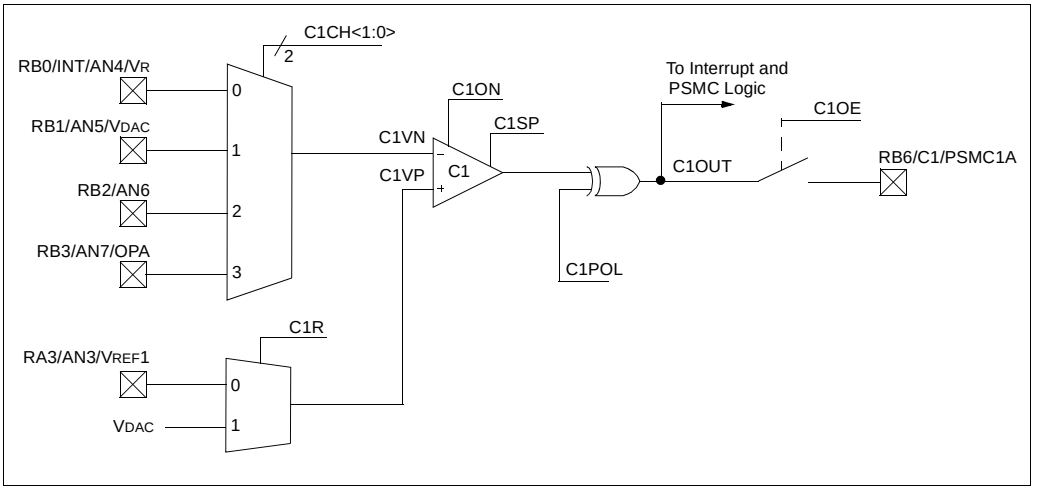


FIGURE 12-2: COMPARATOR C2 SIMPLIFIED BLOCK DIAGRAM

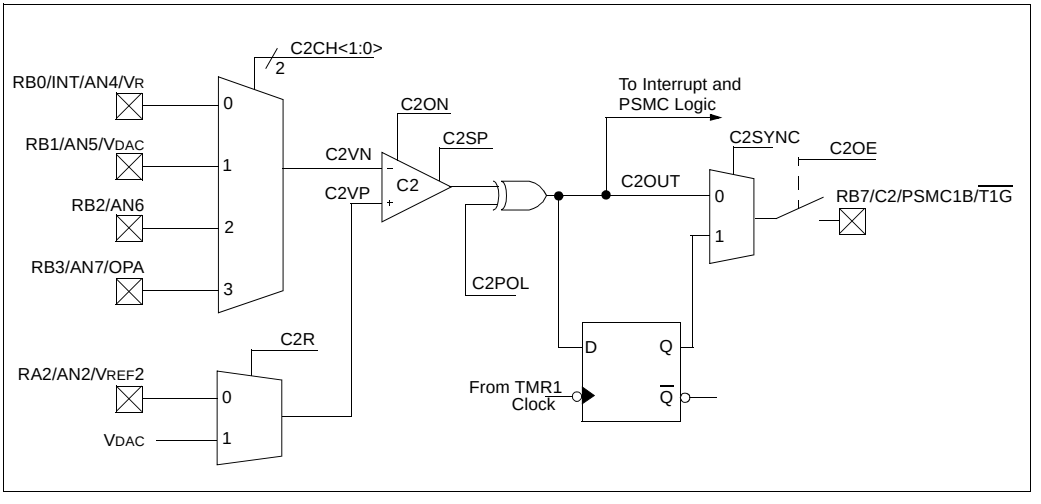
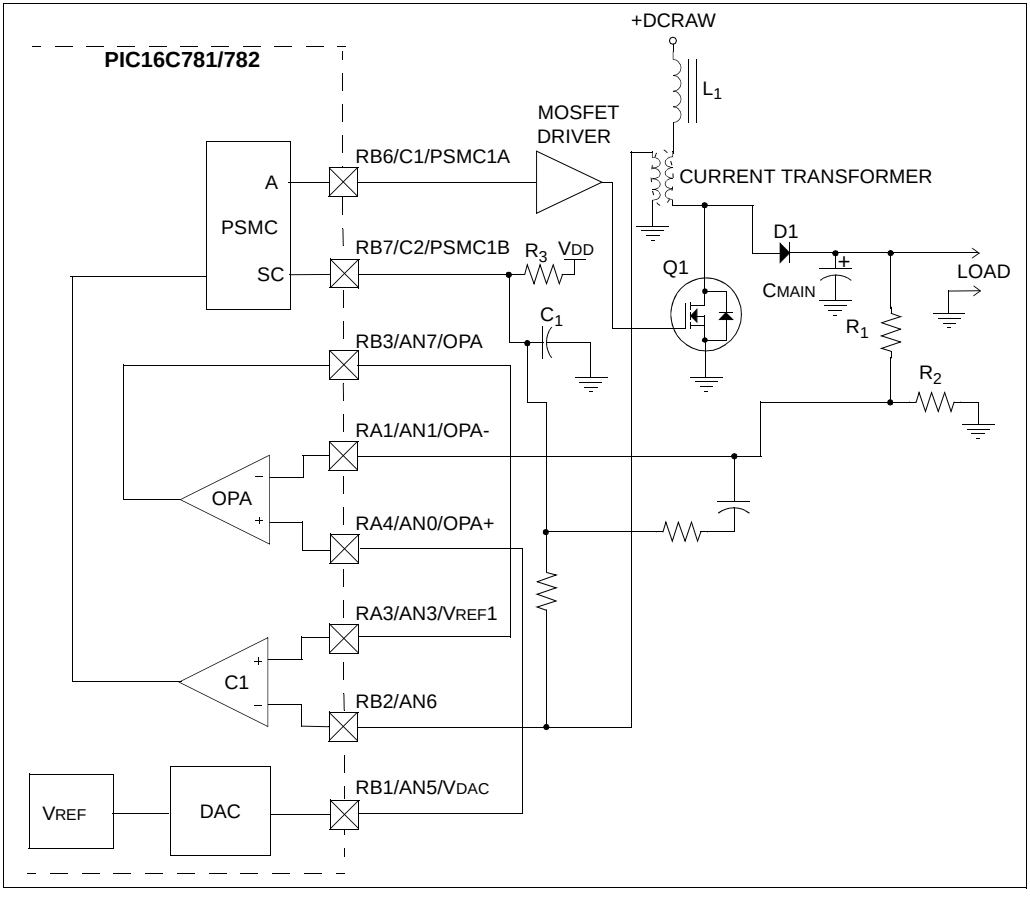


FIGURE 13-5: EXAMPLE BOOST CONFIGURATION LC SWITCHING POWER SUPPLY



Note:	The OPAMP, Comparator and DAC must be configured, prior to enabling the PSMC to prevent unpredictable operation which may stress the power MOSFET transistors.

EXAMPLE 13-2: EXAMPLE PSMC CONFIGURATION FOR A BUCK MODE SWITCHING POWER SUPPLY

```
;*  PSMC Initialization
;*  This code block will configure the PSMC
;*  and all additional peripherals for a buck
;*  mode switching power supply.
;*
;*  Order of configuration
;*  1.  PORTA/B I/O and analog configured
;*  2.  DAC enabled, configured, and preset
;*  3.  Op Amp enabled and configured
;*  4.  Comparator C1 enabled and configured
;*  5.  PSMC configured
;*  6.  PSMC enabled
;*****************************************
;*  This code block will configure all analog ports.
;
    BANKSEL     TRISA               ; Select Bank 1
    MOVLW       B'00001011'
    MOVWF       TRISA               ; Set RA0,1,& 3 as inputs
    MOVLW       B'11001110
    MOVWF       TRISB               ; Set RB1,2,3,6 & 7 as inputs
    MOVLW       B'11101011'
    MOVWF       ANSEL               ; Set AN0,1,3,5,6 & 7 as analog

;*****************************************************
;*  This code block will configure the DAC for VDD as
;*  DACREF, and RB1/AN5/VDAC as an output.

    BANKSEL         DACON0              ; Select Bank 2

    CLRF            DAC                 ; Set DAC to safe value
    MOVLW           B'11000000'         ; Enable DAC, output
    MOVWF           DACON0              ;   and set DACREF = VDD

    MOVLW           OUTPUT_VALUE
    MOVWF           DAC                 ; Set dAC output level

;*****************************************************
;*  This code block will configure the OPA module
;*  as an Op Amp, with a 3 MHZ GBWP

    MOVLW           B'10000001'         ; Set Op Amp mode and
    MOVWF           OPACON              ;  2 MHz GBWP

;*****************************************************
;*  This code block will configure Comparator C1
;*  for normal speed and output polarity,
;*  input on AN6, and Reference from the VREF1

    MOVLW           B'10001010'         ; Set C1; no ext out, norm
    MOVWF           CM1CON0             ;  speed & pol, VREF1, AN6

;*****************************************************
;*  This code block will configure the PSMC module
;*  for PWM, Fosc/128, Single input, Single output
;*  Non-inverting out, DC min = 0%, DC max = 50%

    MOVLW           B'0000000'
    MOVWF           PSMCCON0            ; Set DCmin 0, DCmax 50, Fosc/128
    MOVLW           B'00000110'
    MOVWF           PSMCCON1            ; Set PWM, 1 in, 2 out, noninvert
    BSF             PSMCCON1,SMCON      ; Enable PSMC
```

14.0 SPECIAL FEATURES OF THE CPU

These devices have a host of features intended to maximize system reliability, minimize cost through elimination of external components, provide power saving operating modes and offer code protection. These features include:

- Oscillator selection
- RESET
  - Power-on Reset (POR)
  - Power-up Timer (PWRT)
  - Oscillator Start-up Timer (OST)
  - Programmable Brown-out Reset (PBOR)
- Interrupts
- Watchdog Timer (WDT)
- Programmable Low Voltage Detection (PLVD)
- SLEEP
- Code protection
- ID locations
- In-Circuit Serial Programming™ (ICSP™)

Several oscillator options are available to allow the part to fit the application. The INTRC oscillator options save system cost while the LP crystal option saves power. A set of configuration bits is used to select various options.

The CPU also features a Watchdog Timer (WDT), which can be enabled either through a configuration bit during programming, or by the software. For added reliability, the WDT runs off its own internal RC oscillator instead of the main CPU clock.

In addition to the WDT, the CPU incorporates both an Oscillator Start-up Timer and a Power-up Timer. The Oscillator Start-up Timer (OST) is intended to hold the chip in RESET until the crystal oscillator has stabilized. The Power-up Timer (PWRT) holds the CPU in a fixed RESET delay of 72ms (nominal) on Power-up Resets (POR and PBOR), while the power supply stabilizes. With these two timers on-chip, most applications need no external RESET circuitry.

SLEEP mode is designed to offer a very low current power-down mode. The user can awaken from SLEEP through:

- External RESET
- Watchdog Timer Wake-up
- Interrupt

Additional information on special features is available in the PIC Mid-Range Reference Manual, (DS33023).

14.1 Configuration Bits

The configuration bits can be programmed (read as '0'), or left unprogrammed (read as '1'), to select various device configurations. These bits are mapped in program memory location 2007h.

Note:	Address 2007h is beyond the user program memory space, which can be accessed only during programming.

Some of the core features provided may not be necessary for each application in which a device may be used. The configuration word bits allow these features to be configured/enabled/disabled as necessary. These features include:

- Code Protection
- PBOR Trip Point
- Power-up Timer
- Watchdog Timer
- Device Oscillator Mode

As can be seen in Table 14-1, some additional configuration word bits have been provided for Brown-out Reset trip point selection.

14.9 Interrupts

The devices have up to eight sources of interrupt. The interrupt control register (INTCON) records individual interrupt requests in flag bits. It also has individual and global interrupt enable bits.

Note:	Individual interrupt flag bits are set, regardless of the status of their corresponding mask bit or the GIE bit.

A global interrupt enable bit, GIE (INTCON<7>), enables (if set) all unmasked interrupts or disables (if cleared) all interrupts. When bit GIE is enabled and an interrupt's flag bit and mask bit are set, the interrupt will vector immediately. Individual interrupts can be disabled through their corresponding enable bits in various registers. Individual interrupt bits are set, regardless of the status of the GIE bit. The GIE bit is cleared on RESET.

The "return from interrupt" instruction, RETFIE, exits the interrupt routine as well as sets the GIE bit, which re-enables interrupts.

The RB0/INT/AN4/VR pin interrupt, the RB port Interrupt-on-Change (IOCB) and the TMR0 overflow interrupt flags are contained in the INTCON register.

The peripheral interrupt flags are contained in the special function register PIR1. The corresponding interrupt enable bits are contained in special function register PIE1, and the peripheral interrupt enable bit is contained in special function register INTCON.

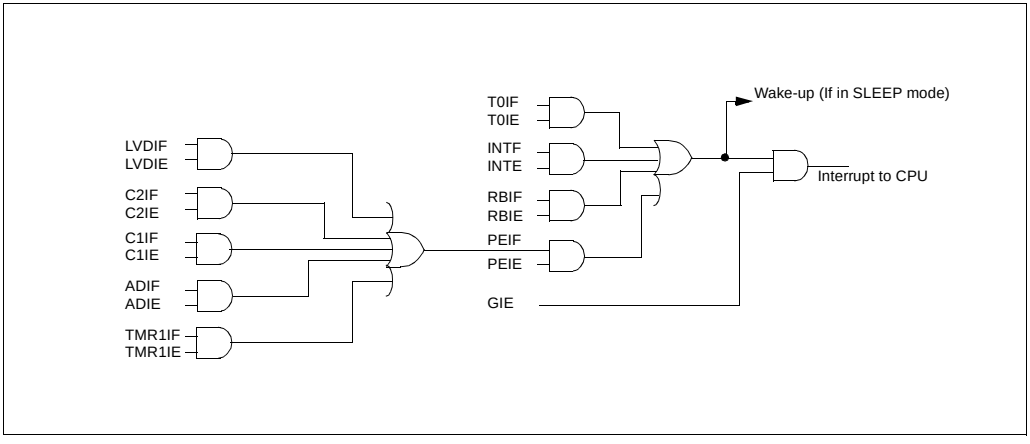
When an interrupt is serviced, the GIE bit is cleared to disable any further interrupt. The return address is pushed onto the stack and the PC is loaded with 0004h. Once in the Interrupt Service Routine the source(s) of the interrupt can be determined by polling the interrupt flag bits. The interrupt flag bit(s) must be cleared in software before re-enabling interrupts to avoid recursive interrupts.

For external interrupt events, such as the INT pin or PORTB change interrupt, the interrupt latency is three or four instruction cycles. The exact latency depends on when the interrupt event occurs. The latency is the same for one or two-cycle instructions. Individual interrupt flag bits are set, regardless of the status of their corresponding mask bit or the GIE bit.

14.9.1 INT INTERRUPT

External interrupt on RB0/INT/AN4/VR pin is edge triggered: either rising, if bit INTEDG (OPTION_REG<6>) is set, or falling, if the INTEDG bit is clear. When a valid edge appears on the RB0/INT pin, flag bit INTF (INTCON<1>) is set. This interrupt can be disabled by clearing enable bit INTE (INTCON<4>). Flag bit INTF must be cleared in software in the Interrupt Service Routine before re-enabling this interrupt. The INT interrupt can awaken the processor from SLEEP, if bit INTE was set prior to going into SLEEP. The status of global interrupt enable bit GIE decides whether or not the processor branches to the interrupt vector following a wake-up sequence. See Section 14.12 for details on SLEEP mode.

FIGURE 14-10: INTERRUPT LOGIC



RRF **Rotate Right f through Carry**

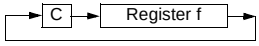
Syntax: [*label*] RRF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: See description below

Status Affected: C

Description: The contents of register 'f' are rotated one bit to the right through the Carry Flag. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed back in register 'f'.



SLEEP

Syntax: [*label*] SLEEP

Operands: None

Operation: 00h → WDT,
0 → WDT prescaler,
1 → $\overline{TO}$,
0 → $\overline{PD}$

Status Affected: $\overline{TO}$, $\overline{PD}$

Description: The power-down status bit, $\overline{PD}$ is cleared. Time-out status bit, $\overline{TO}$ is set. Watchdog Timer and its prescaler are cleared.
The processor is put into SLEEP mode with the oscillator stopped.

SUBLW **Subtract W from Literal**

Syntax: [*label*] SUBLW k

Operands: $0 \le k \le 255$

Operation: k - (W) → (W)

Status Affected: C, DC, Z

Description: The W register is subtracted (2's complement method) from the eight-bit literal 'k'. The result is placed in the W register.

SUBWF **Subtract W from f**

Syntax: [*label*] SUBWF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: (f) - (W) → (destination)

Status Affected: C, DC, Z

Description: Subtract (2's complement method) W register from register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.

SWAPF **Swap Nibbles in f**

Syntax: [*label*] SWAPF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: (f<3:0>) → (destination<7:4>),
(f<7:4>) → (destination<3:0>)

Status Affected: None

Description: The upper and lower nibbles of register 'f' are exchanged. If 'd' is 0, the result is placed in W register. If 'd' is 1, the result is placed in register 'f'.

XORLW **Exclusive OR Literal with W**

Syntax: [*label*]

Operands: $0 \le k \le 255$

Operation: (W) .XOR. k → (W)

Status Affected: Z

Description: The contents of the W register are XOR'ed with the eight-bit literal 'k'. The result is placed in the W register.

XORWF	Exclusive OR W with f
Syntax:	[*label*] XORWF f,d
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	(W) .XOR. (f) $\rightarrow$ (destination)
Status Affected:	Z
Description:	Exclusive OR the contents of the W register with register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.

16.4 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK object linker combines relocatable objects created by the MPASM assembler and the MPLAB C17 and MPLAB C18 C compilers. It can also link relocatable objects from pre-compiled libraries, using directives from a linker script.

The MPLIB object librarian is a librarian for pre-compiled code to be used with the MPLINK object linker. When a routine from a library is called from another source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications. The MPLIB object librarian manages the creation and modification of library files.

The MPLINK object linker features include:

- Integration with MPASM assembler and MPLAB C17 and MPLAB C18 C compilers.
- Allows all memory areas to be defined as sections to provide link-time flexibility.

The MPLIB object librarian features include:

- Easier linking because single libraries can be included instead of many smaller files.
- Helps keep code maintainable by grouping related modules together.
- Allows libraries to be created and modules to be added, listed, replaced, deleted or extracted.

16.5 MPLAB SIM Software Simulator

The MPLAB SIM software simulator allows code development in a PC-hosted environment by simulating the PIC series microcontrollers on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a file, or user-defined key press, to any of the pins. The execution can be performed in single step, execute until break, or trace mode.

The MPLAB SIM simulator fully supports symbolic debugging using the MPLAB C17 and the MPLAB C18 C compilers and the MPASM assembler. The software simulator offers the flexibility to develop and debug code outside of the laboratory environment, making it an excellent multi-project software development tool.

16.6 MPLAB ICE High Performance Universal In-Circuit Emulator with MPLAB IDE

The MPLAB ICE universal in-circuit emulator is intended to provide the product development engineer with a complete microcontroller design tool set for PIC microcontrollers (MCUs). Software control of the MPLAB ICE in-circuit emulator is provided by the MPLAB Integrated Development Environment (IDE), which allows editing, building, downloading and source debugging from a single environment.

The MPLAB ICE 2000 is a full-featured emulator system with enhanced trace, trigger and data monitoring features. Interchangeable processor modules allow the system to be easily reconfigured for emulation of different processors. The universal architecture of the MPLAB ICE in-circuit emulator allows expansion to support new PIC microcontrollers.

The MPLAB ICE in-circuit emulator system has been designed as a real-time emulation system, with advanced features that are generally found on more expensive development tools. The PC platform and Microsoft® Windows environment were chosen to best make these features available to you, the end user.

16.7 ICEPIC In-Circuit Emulator

The ICEPIC low cost, in-circuit emulator is a solution for the Microchip Technology PIC16C5X, PIC16C6X, PIC16C7X and PIC16CXXX families of 8-bit One-Time-Programmable (OTP) microcontrollers. The modular system can support different subsets of PIC16C5X or PIC16CXXX products through the use of interchangeable personality modules, or daughter boards. The emulator is capable of emulating without target application circuitry being present.

16.8 MPLAB ICD In-Circuit Debugger

Microchip's In-Circuit Debugger, MPLAB ICD, is a powerful, low cost, run-time development tool. This tool is based on the FLASH PIC MCUs and can be used to develop for this and other PIC microcontrollers. The MPLAB ICD utilizes the in-circuit debugging capability built into the FLASH devices. This feature, along with Microchip's In-Circuit Serial Programming™ protocol, offers cost-effective in-circuit FLASH debugging from the graphical user interface of the MPLAB Integrated Development Environment. This enables a designer to develop and debug source code by watching variables, single-stepping and setting break points. Running at full speed enables testing hardware in real-time.

16.9 PRO MATE II Universal Device Programmer

The PRO MATE II universal device programmer is a full-featured programmer, capable of operating in stand-alone mode, as well as PC-hosted mode. The PRO MATE II device programmer is CE compliant.

The PRO MATE II device programmer has programmable V_{DD} and V_{PP} supplies, which allow it to verify programmed memory at V_{DD} min and V_{DD} max for maximum reliability. It has an LCD display for instructions and error messages, keys to enter commands and a modular detachable socket assembly to support various package types. In stand-alone mode, the PRO MATE II device programmer can read, verify, or program PIC devices. It can also set code protection in this mode.

16.10 PICSTART Plus Entry Level Development Programmer

The PICSTART Plus development programmer is an easy-to-use, low cost, prototype programmer. It connects to the PC via a COM (RS-232) port. MPLAB Integrated Development Environment software makes using the programmer simple and efficient.

The PICSTART Plus development programmer supports all PIC devices with up to 40 pins. Larger pin count devices, such as the PIC16C92X and PIC17C76X, may be supported with an adapter socket. The PICSTART Plus development programmer is CE compliant.

16.11 PICDEM 1 Low Cost PIC MCU Demonstration Board

The PICDEM 1 demonstration board is a simple board which demonstrates the capabilities of several of Microchip's microcontrollers. The microcontrollers supported are: PIC16C5X (PIC16C54 to PIC16C58A), PIC16C61, PIC16C62X, PIC16C71, PIC16C8X, PIC17C42, PIC17C43 and PIC17C44. All necessary hardware and software is included to run basic demo programs. The user can program the sample microcontrollers provided with the PICDEM 1 demonstration board on a PRO MATE II device programmer, or a PICSTART Plus development programmer, and easily test firmware. The user can also connect the PICDEM 1 demonstration board to the MPLAB ICE in-circuit emulator and download the firmware to the emulator for testing. A prototype area is available for the user to build some additional hardware and connect it to the microcontroller socket(s). Some of the features include an RS-232 interface, a potentiometer for simulated analog input, push button switches and eight LEDs connected to PORTB.

16.12 PICDEM 2 Low Cost PIC16CXX Demonstration Board

The PICDEM 2 demonstration board is a simple demonstration board that supports the PIC16C62, PIC16C64, PIC16C65, PIC16C73 and PIC16C74 microcontrollers. All the necessary hardware and software is included to run the basic demonstration programs. The user can program the sample microcontrollers provided with the PICDEM 2 demonstration board on a PRO MATE II device programmer, or a PICSTART Plus development programmer, and easily test firmware. The MPLAB ICE in-circuit emulator may also be used with the PICDEM 2 demonstration board to test firmware. A prototype area has been provided to the user for adding additional hardware and connecting it to the microcontroller socket(s). Some of the features include a RS-232 interface, push button switches, a potentiometer for simulated analog input, a serial EEPROM to demonstrate usage of the I^2C™ bus and separate headers for connection to an LCD module and a keypad.

TABLE 16-1: DEVELOPMENT TOOLS FROM MICROCHIP

		PIC12CXXX	PIC14000	PIC16C5X	PIC16C6X	PIC16CXXX	PIC16F62X	PIC16C7X	PIC16C7XX	PIC16C8X	PIC16F8XX	PIC16C9XX	PIC17C4X	PIC17C7XX	PIC18CXX2	PIC18FXXX	24CXX/ 25CXX/ 93CXX	HCSXXX	MCRFXXX	MCP2510
Software Tools	MPLAB® Integrated Development Environment	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓				
	MPLAB® C17 C Compiler												✓	✓						
	MPLAB® C18 C Compiler														✓	✓				
	MPASM™ Assembler/ MPLINK™ Object Linker	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		
Emulators	MPLAB® ICE In-Circuit Emulator	✓	✓	✓	✓	✓	✓**	✓	✓	✓	✓	✓	✓	✓	✓	✓				
	ICEPIC™ In-Circuit Emulator	✓		✓	✓	✓		✓	✓	✓		✓								
Debugger	MPLAB® ICD In-Circuit Debugger				✓*			✓*			✓					✓				
Programmers	PICSTART® Plus Entry Level Development Programmer	✓	✓	✓	✓	✓	✓**	✓	✓	✓	✓	✓	✓	✓	✓	✓				
	PRO MATE® II Universal Device Programmer	✓	✓	✓	✓	✓	✓**	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		
Demo Boards and Eval Kits	PICDEM™ 1 Demonstration Board			✓		✓		✓†		✓			✓							
	PICDEM™ 2 Demonstration Board				✓†			✓†							✓	✓				
	PICDEM™ 3 Demonstration Board											✓								
	PICDEM™ 14A Demonstration Board		✓																	
	PICDEM™ 17 Demonstration Board													✓						
	KEELOQ® Evaluation Kit																	✓		
	KEELOQ® Transponder Kit																	✓		
	microID™ Programmer's Kit																		✓	
	125 kHz microID™ Developer's Kit																		✓	
	125 kHz Anticollision microID™ Developer's Kit																		✓	
	13.56 MHz Anticollision microID™ Developer's Kit																		✓	
	MCP2510 CAN Developer's Kit																			✓

* Contact the Microchip Technology Inc. web site at www.microchip.com for information on how to use the MPLAB® ICD In-Circuit Debugger (DV164001) with PIC16C62, 63, 64, 65, 72, 73, 74, 76, 77.

** Contact Microchip Technology Inc. for availability date.

† Development tool is available on select devices.

17.5 Comparators

TABLE 17-10: DC CHARACTERISTICS: VOLTAGE COMPARATORS C1 AND C2

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated): V_{DD} = 2.7V to 5.5V, T_A = 25°C, V_{CM} = V_{DD}/2 Operating Temperature -40°C to +85°C for Industrial				
Param No.	**Parameters**	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
	Input Offset Voltage	V_{OS}	TBD TBD	±1 ± 2.5	TBD TBD	mV mV	C1SP = 1, C2SP = 1 C1SP = 0, C2SP = 0
	Input Current and Impedance Input Bias Current Input Offset Bias Current	 I_B I_{OS}	 TBD —	 — TBD	 — TBD	 nA nA	
	Common Mode Common Mode Input Range Common Mode Rejection	 V_{CM} CMR	 V_{SS} —	 — 70	 V_{DD}-1.4V	 V dB	 V_{DD} = 5V V_{CM} = V_{DD}/2, Frequency = DC
	Open Loop Gain DC Open Loop Gain	 A_{OL}	 —	 90	 —	 dB	
	Power Supply Rejection	PSR	—	TBD	—	dB	V_{DD} = 5V

TABLE 17-11: AC CHARACTERISTICS: COMPARATORS C1 AND C2

AC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated): V_{DD} = 2.7V to 5.5V, T_A = 25°C, V_{CM} = V_{DD}/2 Operating Temperature -40°C to +85°C for Industrial				
Param No.	**Parameters**	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
	Response Time Response Time	 t_r	 —	 75	 —	 ns	 V_{DD} = 5V, C1SP = 1, C2SP = 1, Comparator output signal is for internal use only, Input overdrive = 10 mV, step = 110 mV, V_{CM} = V_{DD}/2.
		t_r	—	0.5	—	µs	V_{DD} = 5V, C1SP = 0, C2SP = 0, Comparator output signal is for internal use only, Input overdrive = 10 mV, step = 110 mV, V_{CM} = V_{DD}/2.
		t_r	—	100	TBD	ns	V_{DD} = 5 , C_L = 100 pF, C1SP = 1, C2SP = 1, Comparator output is available on I/O pin, Input overdrive = 10 mV, step = 110 mV, V_{CM} = V_{DD}/2.
		t_r	—	0.5	TBD	µs	V_{DD} = 5 , C_L = 100 pF, C1SP = 0, C2SP = 0, Comparator output is available on I/O pin, Input overdrive = 10 mV, step = 110 mV, V_{CM} = V_{DD}/2.
	Turn On Time	T_{ON}	— —	10 TBD	TBD TBD	µs µs	C1SP = 0, C2SP = 0, V_{DD} = 5V C1SP = 1, C2SP = 1, V_{DD} = 5V

18.0 DC AND AC CHARACTERISTICS GRAPHS AND TABLES

The graphs and tables provided in this section are for design guidance and are not tested nor guaranteed. In some graphs or tables the data presented is outside specified operating range (e.g., outside specified V_{DD} range.). This is for information only and devices are ensured to operate properly only within the specified range. The data presented in this section is a statistical summary of data collected on units from different lots over a period of time.

Standard deviation is denoted by sigma (σ).

Typ or Typical represents the mean of the distribution at 25°C.

Max or Maximum represents the mean +3σ over the temperature range of -40°C to 85°C.

Min or Minimum represents the mean -3σ over the temperature range of -40°C to 85°C.

Graphs and Tables are not available at this time.

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NOTES: