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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	13
Program Memory Size	1.75KB (1K x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 8x8b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	20-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lc781t-i-so

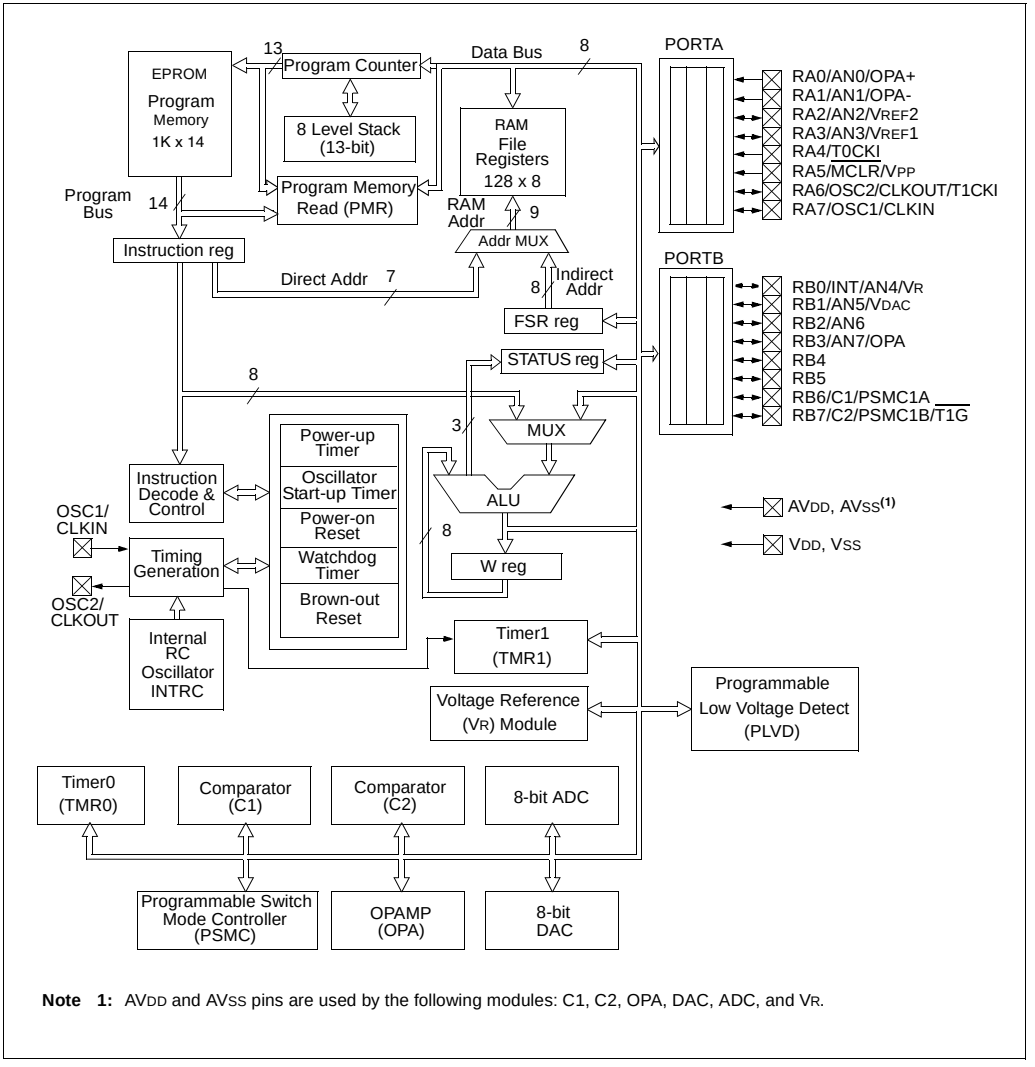
1.0 DEVICE OVERVIEW

This document contains device-specific information. Additional information may be found in the PIC Mid-Range Reference Manual (DS33023), which may be obtained from your local Microchip Sales Representative or downloaded from the Microchip website. The Reference manual should be considered a complementary document to this data sheet. The Reference manual is highly recommended reading for a better understanding of the device architecture and operation of the peripheral modules.

This data sheet covers two devices: PIC16C781 and PIC16C782. Both devices come in a variety of 20-pin packages.

The following figures are block diagrams of the PIC16C781 and the PIC16C782.

FIGURE 1-1: PIC16C781 BLOCK DIAGRAM



Note 1: AVDD and AVSS pins are used by the following modules: C1, C2, OPA, DAC, ADC, and VR.

3.3 PORTB and the TRISB Register

PORTB is an 8-bit wide, bi-directional port. The corresponding data direction register is TRISB. Setting a TRISB bit (= 1) makes the corresponding PORTB pin an input (i.e., puts the corresponding output driver into a Hi-Impedance mode). Clearing a TRISB bit (= 0) makes the corresponding PORTB pin an output (i.e., puts the contents of the output latch on the selected pin.

EXAMPLE 3-2: INITIALIZING PORTB

```
;* This code block will configure PORT B
;* as follows
;*  RB<7:6> analog inputs
;*  RB<5:4> digital inputs
;*  RB<3:2> digital inputs
;*  RB<1:0> digital inputs
;*  RA<3:0> digital I/O

    BANKSEL     PORTB       ; Select Bank 0
    CLRF        PORTB       ; Preset PORTB data
                            ; reg.
    BANKSEL     TRISB       ; Select Bank 1
    MOVLW       B'11001111' ; Digital I/O
                            ;   config data
    MOVWF       TRISB       ; Configure PORTB
                            ; digital
    MOVLW       B'00000011' ; Analog I/O config
                            ; data
    MOVWF       ANSEL       ; Configure PORTB
                            ; analog
```

The RB0 pin can be configured as:

- Digital I/O
- ADC/Comparator Analog Input (AN4)
- External Interrupt (INT)
- Voltage Reference Output (V_R)

When the pin is used as an analog I/O, the ANSEL register must have bit 4 set to configure the RB0 pin as an analog input.

Pin RB1 is multiplexed with two analog functions: ADC/Comparator Analog Input AN5, and the output of the DAC. When the pin is used as an analog I/O, the ANSEL register must have bit 5 set to configure the RB1 pin as an analog I/O.

Pin RB2 is multiplexed with the analog function ADC/Comparator Input AN6. When the pin is used as an analog input, the ANSEL register must have bit 6 to select the Analog mode for the pin.

The RB3 pin is multiplexed with two analog functions: ADC/Comparator Analog Input AN7, and the output of the OPA module. When the pin is used as analog I/O, the ANSEL register must have bit 7 set to select the Analog mode of the pin.

Pins RB<7:6> are multiplexed with the outputs of the two on-board comparators, the outputs of the PSMC module, and the clock gate input for Timer1. Note, when enabled, these peripherals override the PORTB data register; however, TRISB retains control of output drivers. Therefore, TRISB<7:6> must be programmed appropriately for Comparator and PSMC outputs to operate.

3.3.1 PORTB WEAK PULL-UP

Each of the PORTB pins has an internal weak pull-up resistance, which can be individually enabled from the WPUB register. A single global enable bit, $\overline{\text{RBPU}}$ (OPTION_REG<7>), can turn on/off all of the selected pull-ups. Clearing the $\overline{\text{RBPU}}$ bit (OPTION_REG<7>) enables the weak pull-up resistors (see Register 3-2). The weak pull-up is automatically turned off when the port pin is configured as an output. The pull-ups are disabled on a Power-on Reset.

3.3.2 PORTB INTERRUPT-ON-CHANGE

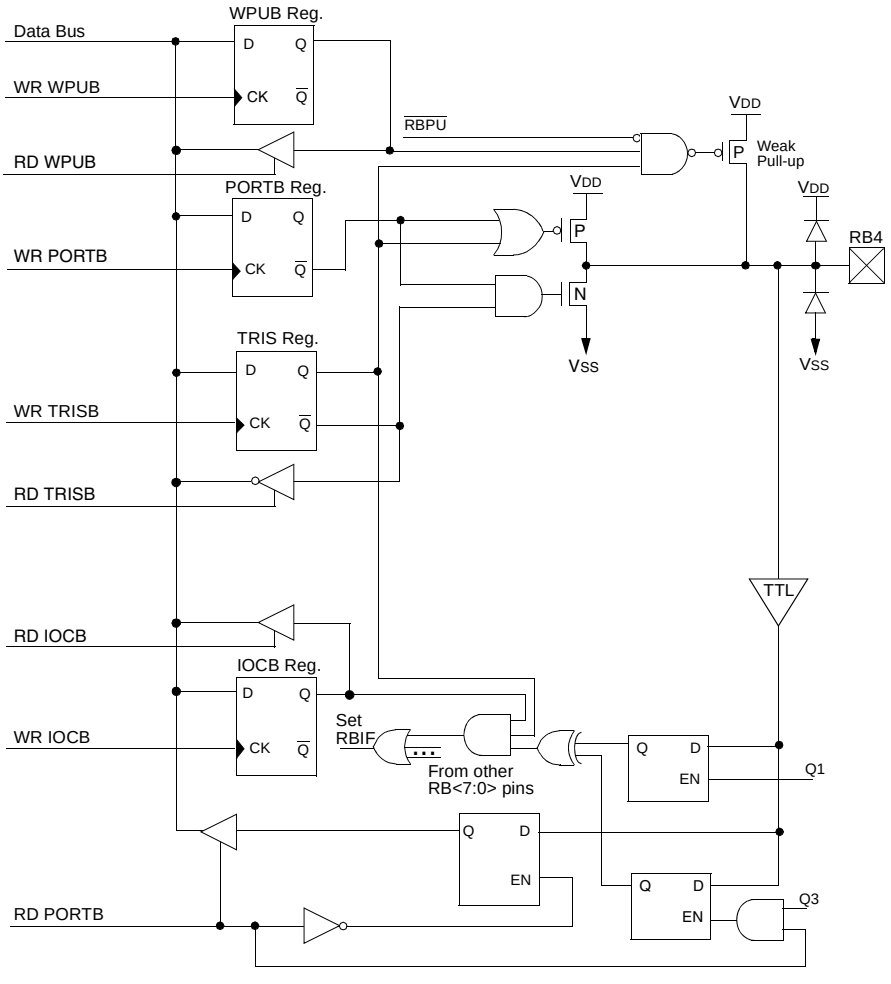
Each of the PORTB pins, if configured as input, has the ability to generate an interrupt-on-change. To enable the interrupt-on-change feature, the corresponding bit must be set in the IOCB register (see Register 3-3). The RBIE bit in the INTCON register functions as a global enable bit to turn on/off the interrupt-on-change feature. The selected inputs are compared to the old value latched on the last read of PORTB. The "mismatch" outputs are OR-ed together to generate the RB Port Change Interrupt with flag bit RBIF (INTCON<0>).

The IOCB interrupt can also awaken the device from SLEEP. The user, in the Interrupt Service Routine, must clear the interrupt in the following manner:

a) A read or write to PORTB. This copies the current state into the latch and ends the mismatch condition.

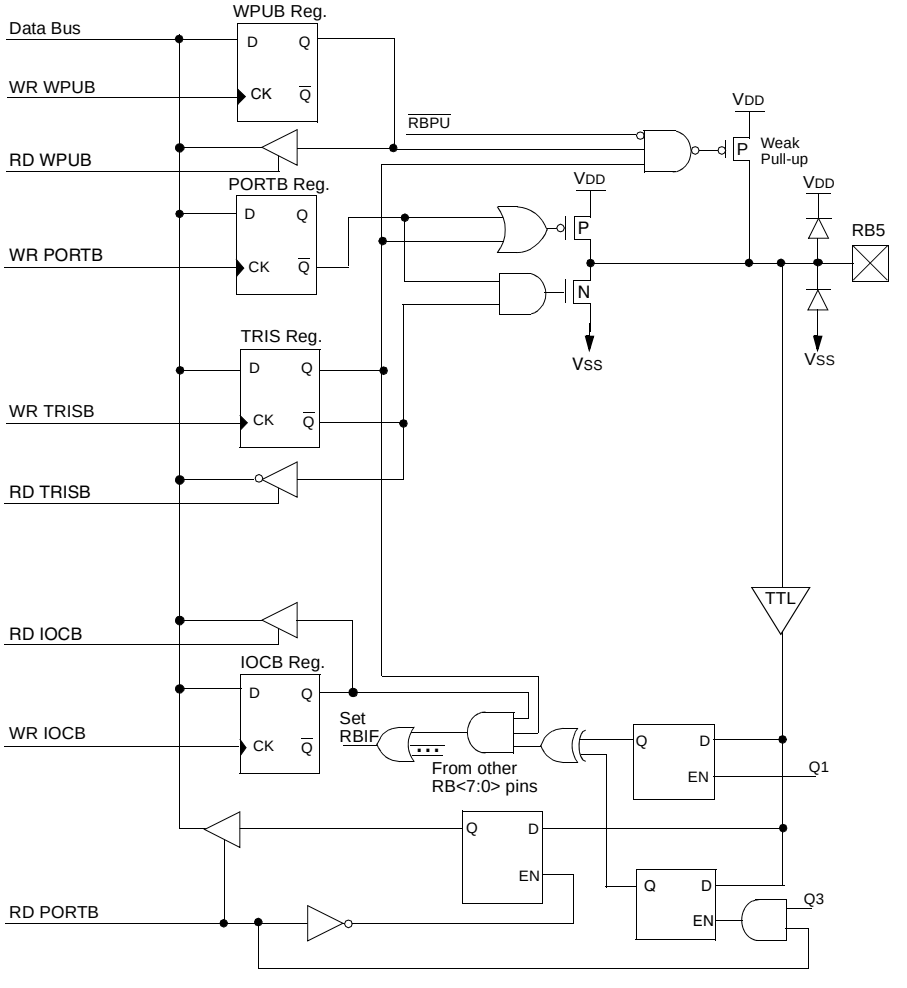
b) Clear flag bit RBIF.

FIGURE 3-13: BLOCK DIAGRAM OF RB4 PIN



TRISB<4>	FUNCTION	PORTB<4> READ
0	Digital Out	Pin
1	Digital In	Pin

FIGURE 3-14: BLOCK DIAGRAM OF RB5 PIN



TRISB<5>	FUNCTION	PORTB<5> READ
0	Digital Out	Pin
1	Digital In	Pin

6.0 TIMER1 MODULE WITH GATE CONTROL

The Timer1 module timer/counter has the following features:

- 16-bit timer/counter
  (two 8-bit registers:TMR1H and TMR1L)
- Readable and writable (both registers)
- Internal or external clock select
- Interrupt on overflow from FFFFh to 0000h
- External enable input ($\overline{T1G}$ pin with TMR1GE bit = 1)
- Option for Timer1 to use LP oscillator if device is configured to use INTRC w/o CLKOUT

Timer1 Control register (T1CON) is shown in Register 6-1.

Figure 6-2 is a simplified block diagram of the Timer1 module.

6.1 Timer1 Operation

Timer1 can operate in one of three modes:

1. 16-bit timer with prescaler.
2. 16-bit synchronous counter.
3. 16-bit asynchronous counter.

In Timer mode, Timer1 is incremented on every instruction cycle. In Counter mode, Timer1 is incremented on the rising edge of the external clock input T1CKI (RA6/OSC2/CLKOUT/T1CKI). In addition, the Counter mode clock can be synchronized to the microcontroller clock or run asynchronously.

In Counter and Timer modes, the counter/timer clock can be gated by the $\overline{T1G}$ input.

If an external clock oscillator is needed (and the microcontroller is using INTRC w/o CLKOUT), Timer1 can use the LP oscillator as a clock source.

Note 1: In Counter mode, the counter increments on the rising edge of the clock.

EXAMPLE 6-1: TIMER1 INITIALIZATION

```
;* This code block will configure Timer1 for
;* Polling, Ext gate of int clk (Fosc/4), &
;* 1:1 prescaler.
;*
;* Wait for TMR1 overflow code included
;*
   BANKSEL  TMR1L           ; Select Bank 0
   CLRF     TMR1L           ; Clear TMR1 LSB
   CLRF     TMR1H           ; Clear TMR1 MSB
   MOVLW    B'01000000'     ; Gate, Ps 1:1
   MOVWF    T1CON           ; Int clk
   BSF      T1CON,TMR1ON    ; Enable timer

;*****************************************
;* Wait for TMR1 overflow

T1_OVFL_WAIT
   BANKSEL  PIR1            ; Select Bank 0
   T1_WAIT                  ;
   TBFSS    PIR1,TMR1IF     ; Overflow?
   GOTO     T1_WAIT         ; If 0, again

   BCF      PIR1,TMR1IF     ; Clear flag
```

6.3 Timer1 Oscillator for the PIC16C781/782

When the microcontroller is using INTRC w/o CLKOUT, Timer1 can enable and use the LP oscillator as the Timer1 oscillator. When enabled, Timer1 oscillator operation is solely controlled by the T1OSCEN bit. The oscillator will operate independently of the TMR1ON bit, allowing the programmer to start and stop the Timer/Counter using the TMR1ON bit. The oscillator will also operate during SLEEP, allowing continuous timekeeping with Timer1. The electrical requirements for the LP oscillator, when used as the Timer1 oscillator, are the same as when the oscillator is used in LP mode.

Note:	The oscillator requires a startup and stabilization time before use. Therefore, T1OSCEN should be set, and a suitable delay observed, prior to enabling Timer1 (see Section 14.2).

6.4 Timer1 Interrupt

The TMR1 register pair (TMR1H and TMR1L) increments from 0000h to FFFFh and then rolls over to 0000h. When Timer1 rolls over, the TMR1IF bit (PIR1<0>) is set. To enable an interrupt, the TMR1IE bit (PIE1<0>), the GIE (INTCON<7>) and the PEIE bit (INTCON<6>) must be set prior to rollover. To clear the interrupt, the TMR1IF must be cleared by software prior to re-enabling interrupts.

Note:	When enabling the Timer1 interrupt, the user should clear both TMR1 registers and the TMR1IF prior to enabling interrupts.

6.5 Effects of RESET

Only POR and BOR Resets clear T1CON, disabling Timer1. All other RESETS do not affect Timer1.

TABLE 6-1: SUMMARY OF REGISTERS ASSOCIATED WITH TIMER1

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other RESETS
0Bh	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000X	0000 000u
0Ch	PIR1	LVDIF	ADIF	C2IF	C1IF	—	—	—	TMRIF	0000 ---0	0000 ---0
8Ch	PIE1	LVDIE	ADIE	C2IE	C1IE	—	—	—	TMRIE	0000 ---0	0000 ---0
0Eh	TMR1L	Least Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	uuuu uuuu
0Fh	TMR1H	Most Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	uuuu uuuu
10h	T1CON	—	TMR1GE	T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	TMR1CS	TMR1ON	-000 0000	-uuu uuuu

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by Timer1.

NOTES:

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9.0 ANALOG-TO-DIGITAL CONVERTER (ADC) MODULE

The 8-bit ADC module, shown in Figure 9-1, has 10 inputs in the PIC16C781/782:

- 8 external channels, AN<7:0> (RA<3:0> and RB<3:0>)
- 2 internal channels, VR and VDAC

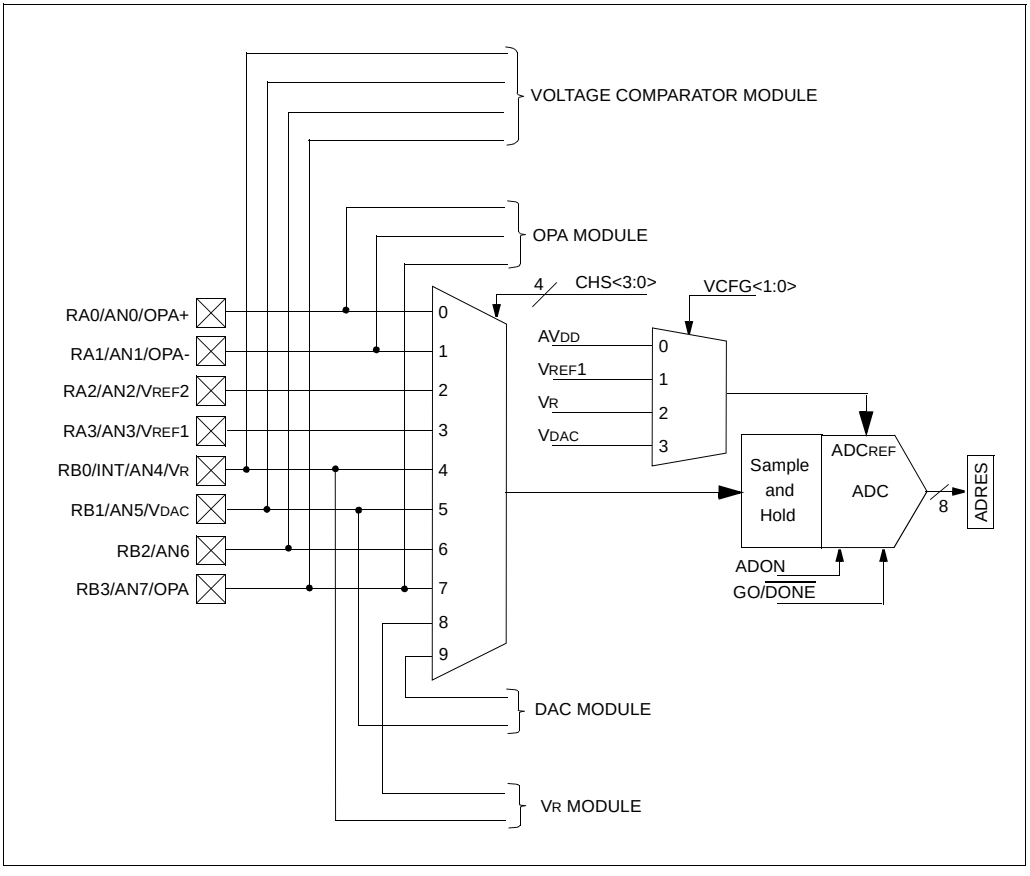
The ADC allows conversion of an analog input signal to a corresponding 8-bit digital value. The desired channel is connected to a Sample-and-Hold by the input multiplexers. The output of the Sample-and-Hold captures a snapshot of the voltage and holds it for the ADC. The ADC then generates the 8-bit result via successive approximation.

The analog reference voltage (ADCREF) is software selectable from the following options:

- The analog positive supply: AVDD
- The reference input for Comparator C1: VREF1
- The Voltage Reference module output: VR
- The DAC Converter module output: VDAC

The ADC has the unique feature of being able to operate while the device is in SLEEP mode. To operate in SLEEP, the ADC conversion clock must be derived from the ADC's dedicated internal RC oscillator.

FIGURE 9-1: ADC MODULE BLOCK DIAGRAM



9.1 Control Registers

The ADC module has three registers. These registers are:

- ADC Result Register: ADRES
- ADC Control Register 0: ADCON0
- ADC Control Register 1: ADCON1

The ADCON0 register, shown in Register 9-1, controls the operations and input channel selection for the ADC module. The ADCON1 register, shown in Register 9-3, selects the voltage reference used by the ADC module. The ADRES register, shown in Register 9-2, holds the 8-bit result of the conversion.

Additional information on using the ADC module can be found in the PIC Mid-Range MCU Family Reference Manual (DS33023) and in Application Note AN546 (DS00546).

9.1.1 ADCON0 REGISTER

The ADCON0 register, shown in Register 9-1, controls the following:

- Clock source and prescaler
- Input channel
- Conversion start/stop
- Enabling of the ADC module

Setting the ADON bit, ADCON0<0>, enables the ADC module. Clearing ADON disables the module and terminates any conversion in process.

The ADCS<1:0> bits (ADCON0<7:6>) determine the clock source used by the ADC module.

The CHS<3:0> bits (ADCON0<5:3,1>) determine the input channel to the ADC module. CHS<3> specifically determines whether the source is internal or external.

Setting the GO/$\overline{\text{DONE}}$ bit (ADCON0<2>) initiates the conversion process. The ADC clears this bit at the completion of the conversion process.

REGISTER 9-1: ADC CONTROL REGISTER 0 (ADCON0: 1Fh)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/S-0	R/W-0	R/W-0
ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/$\overline{\text{DONE}}$	CHS3	ADON
bit 7							bit 0

bit 7-6 **ADCS<1:0>:** ADC Conversion Clock Select bits
00 = FOSC/2
01 = FOSC/8
10 = FOSC/32
11 = ADRC (clock derived from a dedicated RC oscillator)

bit 5-3 **CHS<2:0>:** Analog Channel Select bits (select which channel to convert)

If CHS3 = 0:	If CHS3 = 1:
000 = channel 0 (AN0)	000 = VR
001 = channel 1 (AN1)	001 = VDAC
010 = channel 2 (AN2)	010 = Reserved. Do not use.
011 = channel 3 (AN3)	011 = Reserved. Do not use.
100 = channel 4 (AN4)	100 = Reserved. Do not use.
101 = channel 5 (AN5)	101 = Reserved. Do not use.
110 = channel 6 (AN6)	110 = Reserved. Do not use.
111 = channel 7 (AN7)	111 = Reserved. Do not use.

bit 2 **GO/$\overline{\text{DONE}}$:** ADC Conversion Status bit
1 = ADC conversion cycle in progress. Setting this bit starts an ADC conversion cycle.
0 = ADC conversion is not in progress (this bit is cleared by hardware when conversion is complete)

bit 1 **CHS3:** Analog Channel Select bit
1 = Internal channel selected for conversion
0 = External channel selected for conversion

bit 0 **ADON:** ADC On bit
1 = ADC enabled
0 = ADC disabled

Legend:			
S = Settable bit			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

REGISTER 11-1: OPAMP CONTROL REGISTER (OPACON: 11Ch)

R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0	R/W-0
OPAON	CMPEN	—	—	—	—	—	GBWP
bit 7							bit 0

bit 7 **OPAON:** OPAMP Enable bit
1 = OPAMP is enabled
0 = OPAMP is disabled

bit 6 **CMPEN:** Comparator Mode Enable bit
1 = Comparator mode
0 = OPAMP mode

bit 5-1 **Unimplemented:** Read as '0'

bit 0 **GBWP:** Gain Bandwidth Product Select bits
1 = 2 MHz typ. (fast mode)
0 = 70 kHz typ. (slow mode)

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

11.1.2 CALCON REGISTER

The Automatic Calibration Module (ACM) is an internal state machine which performs an input offset voltage calibration (trim) on the OPA module (see Figure 11-2). Calibration is initiated by setting the CAL bit (CALCON<7>). Upon completion of the calibration sequence, the ACM will clear the CAL bit.

If a problem arises in the calibration process, the CALERR flag (CALCON<6>) will be set to indicate the failure to calibrate.

Setting CALREF (CALCON<5>) forces calibration at a common mode voltage specified by the output of the DAC module. The DAC module must be enabled prior to calibration. Clearing CALREF will perform the calibration with a common mode voltage of 1.2V. The output pin floats during calibration.

Note 1: Auto Calibration must be performed while the module is configured as an OPAMP (CMPEN = 0). Performing Auto Calibration function in the Comparator mode may yield unpredictable results.

2: If the internal 1.2V reference is used for the common mode voltage during Auto Calibration, CALREF = 0 (CALCON<5>), a delay for reference stabilization must be observed before start of calibration.

3: The OPA module shares pins with the ADC module. Performing ADC conversions on the OPA+ or OPA- pins may affect OPAMP stability.

4: When using the DAC as a reference for calibration, CALREF = 1 (CALCON<5>), the V_{DAC} voltage must be within the specified common mode voltage for the OPAMP.

FIGURE 12-1: COMPARATOR C1 SIMPLIFIED BLOCK DIAGRAM

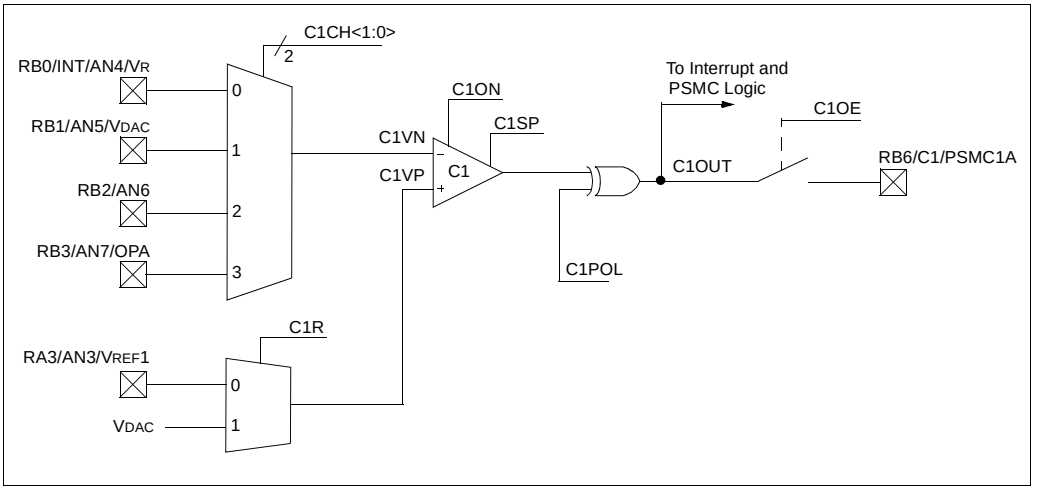
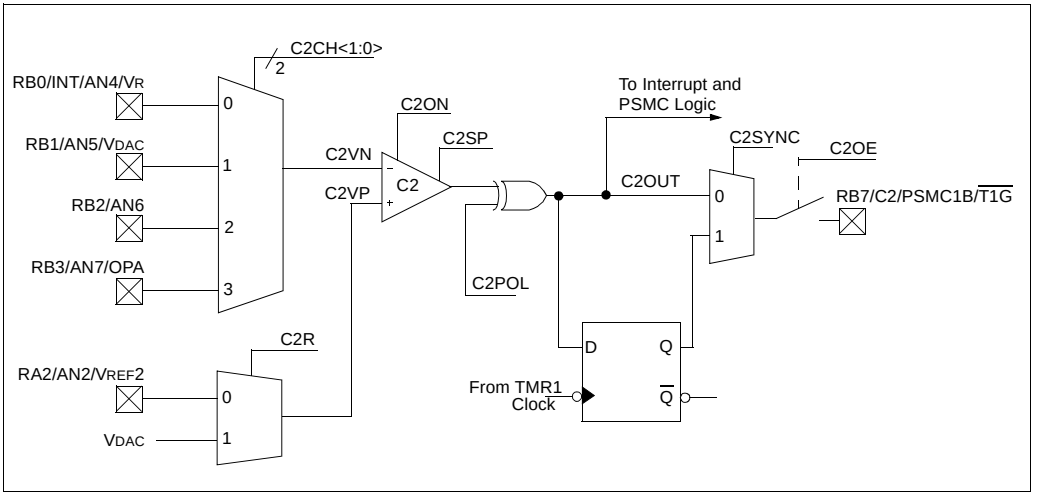


FIGURE 12-2: COMPARATOR C2 SIMPLIFIED BLOCK DIAGRAM



12.2 Comparator Configuration

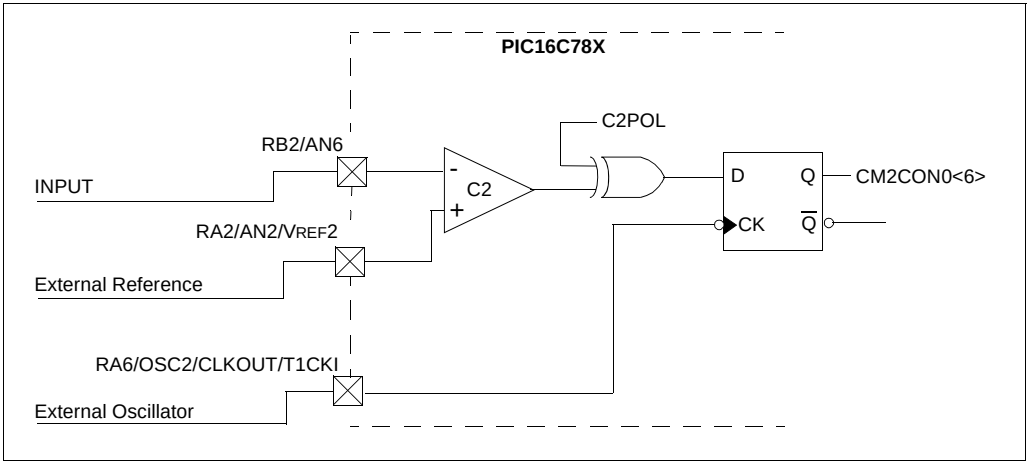
The following examples show the use of the Comparator module in:

- A simple voltage comparator configuration synchronized to the Timer 1 clock input.
- A comparator input to the PSMC with a programmable DAC reference.
- A low power window comparator configuration with interrupt-on-change.

12.2.1 EXAMPLE: C2 SYNCHRONIZED TO T1CKI

In this example, Comparator C2 is configured as a normal voltage comparator synchronized to the T1CKI input. A block diagram of the comparator with external connections is shown in Figure 12-2.

FIGURE 12-3: COMPARATOR C2 CONFIGURATION WITH OUTPUT SYNCHRONIZED TO T1CKI



EXAMPLE 12-1: C2 CONFIGURATION PROGRAM

```
;*  This code block will configure C2
;*  for normal speed and output polarity,
;*  input on AN6, Reference from VREF2, and
;*  output synchronization to TMR1 clock.
;*
    BANKSEL TRISA          ; Select Bank 1
    BSF     TRISA,RA2      ; RA2 as input
    BSF     TRISA,RA6      ; RA6 as input
    BSF     TRISB,RB2      ; RB2 as input

    BSF     ANSEL,AN2      ; AN2 as analog
    BSF     ANSEL,AN6      ; AN6 as analog

    BANKSEL CM2CON0        ; Select Bank 2
    MOVLW   B'10001010'    ; Set C2; no out
    MOVWF   CM2CON0        ; VREF2, AN6

    BSF     CM2CON1,C2SYNC ; CLK sync
```

12.2.2 EXAMPLE: C1 INPUT TO PSMC W/ DAC AS REFERENCE

In this example, Comparator C1 is configured as a non-inverting normal speed voltage comparator input to the PSMC, with a programmable reference voltage. A block diagram of the comparator with external connections is shown in Figure 12-3.

13.3.2 EXAMPLE BUCK LC SWITCHING POWER SUPPLY

In this example, the PSMC controls the buck configuration switching power supply in Figure 13-6.

The PSMC is configured as a typical PWM, current mode, switching power supply controller. The inner current feedback loops consist of:

- PSMC
- 2 MOSFET drivers
- Power MOSFETs Q1 and Q2
- Inductors L1 and L2
- Current transformer
- Comparator C1/C2

The outer voltage feedback loop consists of:

- Diodes D1, D2, D3, and D4
- CMAIN
- OPAMP feedback filter
- DAC reference

The circuit uses two feedback loops, an inner current control loop, and an outer voltage loop. The inner loop is further divided into two channels, Q1/L1, and Q2/L2. The PSMC operates a PWM output, alternately driving Q1 for a cycle, then driving Q2 the next. During the active phase of either output pulse, the inner loop builds up a current flow in the output's inductor, proportional to the error voltage received from the OPAMP. The current flow in the inductor begins the charging of CMAIN. When the voltage (proportional to the current flow in the inductor) exceeds the error voltage:

- The comparator resets the PSMC output
- The MOSFET is turned off
- The flyback diode forward biases
- The inductor discharges into CMAIN for the remainder of the period.

The outer voltage loop monitors the output voltage across CMAIN via R1/R2. The reference voltage from the DAC is subtracted from the feedback voltage to generate the raw error voltage. The raw error voltage is then filtered by the OPAMP and routed to Comparator C1 in the inner current loop.

In using two alternating outputs, the outputs are limited to less than 50% duty cycle. As a result, the circuit avoids the problems associated with instability at duty cycles of >50%.

For more information concerning the design of switching power supplies, refer to:

Switching Power Supply Design, by Abraham I. Pressman, published by McGraw Hill (ISBN 0-07-052236-7).

Note:	Following RESET, both the PSMC1A and PSMC1B outputs are held tri-state until the PSMC is configured. Driver circuitry for all power MOSFET transistors must have a resistor bias to turn off the transistor in the event of tri-state conditions on either output to prevent undo stress on the MOSFET's and their associated circuitry.

MOVF	Move f
Syntax:	[*label*] MOVF f,d
Operands:	0 ≤ f ≤ 127 d ∈ [0,1]
Operation:	(f) → (destination)
Status Affected:	Z
Description:	The contents of register f are moved to a destination dependant upon the status of d. If d = 0, destination is W register. If d = 1, the destination is file register f itself. d = 1 is useful to test a file register, since status flag Z is affected.

MOVLW	Move Literal to W
Syntax:	[*label*] MOVLW k
Operands:	0 ≤ k ≤ 255
Operation:	k → (W)
Status Affected:	None
Description:	The eight-bit literal 'k' is loaded into W register. The don't cares will assemble as 0's.

MOVWF	Move W to f
Syntax:	[*label*] MOVWF f
Operands:	0 ≤ f ≤ 127
Operation:	(W) → (f)
Status Affected:	None
Description:	Move data from W register to register 'f'.

NOP	No Operation
Syntax:	[*label*] NOP
Operands:	None
Operation:	No operation
Status Affected:	None
Description:	No operation.

RETFIE	Return from Interrupt
Syntax:	[*label*] RETFIE
Operands:	None
Operation:	TOS → PC, 1 → GIE
Status Affected:	None

RETLW	Return with Literal in W
Syntax:	[*label*] RETLW k
Operands:	0 ≤ k ≤ 255
Operation:	k → (W); TOS → PC
Status Affected:	None
Description:	The W register is loaded with the eight bit literal 'k'. The program counter is loaded from the top of the stack (the return address). This is a two-cycle instruction.

RETURN	Return from Subroutine
Syntax:	[*label*] RETURN
Operands:	None
Operation:	TOS → PC
Status Affected:	None
Description:	Return from subroutine. The stack is POPed and the top of the stack (TOS) is loaded into the program counter. This is a two-cycle instruction.

RLF	Rotate Left f through Carry
Syntax:	[*label*] RLF f,d
Operands:	0 ≤ f ≤ 127 d ∈ [0,1]
Operation:	See description below
Status Affected:	C
Description:	The contents of register 'f' are rotated one bit to the left through the Carry Flag. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is stored back in register 'f'.

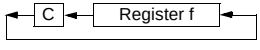


FIGURE 17-5: EXTERNAL CLOCK TIMING

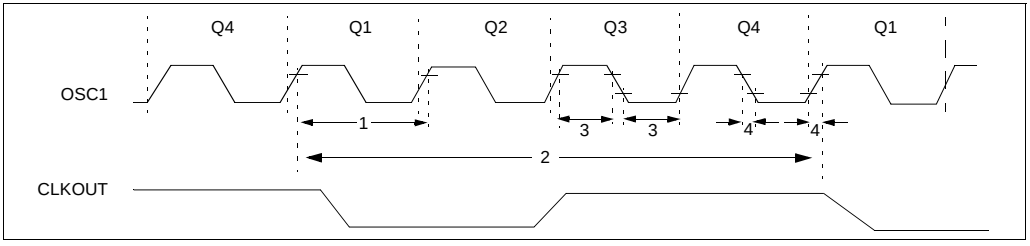


TABLE 17-4: EXTERNAL CLOCK TIMING REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
1A	FOSC	External CLKIN Frequency(1)	DC	—	4	MHz	XT osc mode
			DC	—	20	MHz	EC osc mode
			DC	—	20	MHz	HS osc mode
			DC	—	200	kHz	LP osc mode
		Oscillator Frequency(1)	0.1	—	4	MHz	XT osc mode
			4	—	20	MHz	HS osc mode
			5	—	200	kHz	LP osc mode
1	TOSC	External CLKIN Period(1)	250	—	—	ns	XT and RC osc mode
			50	—	—	ns	EC osc mode
			50	—	—	ns	HS osc mode
			5	—	—	µs	LP osc mode
		Oscillator Period(1)	250	—	10,000	ns	XT osc mode
			50	—	250	ns	HS osc mode
			5	—	—	µs	LP osc mode
2	TCY	Instruction Cycle Time(1)	200	TCY	DC	ns	TCY = 4/FOSC
3*	TOSL, TOSH	External Clock in (OSC1) High or Low Time	100	—	—	ns	XT oscillator
			2.5	—	—	µs	LP oscillator
			15	—	—	ns	HS oscillator
							EC oscillator
4*	TOSR, TOSF	External Clock in (OSC1) Rise or Fall Time	—	—	25	ns	XT oscillator
			—	—	50	ns	LP oscillator
			—	—	15	ns	HS oscillator
							EC oscillator

* These parameters are characterized but not tested.

† Data in “Typ” column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (TCY) equals four times the input oscillator time-base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1/CLKIN pin.
When an external clock input is used, the "Max." cycle time limit is "DC" (no clock) for all devices.

17.4 Operational Amplifier

TABLE 17-8: DC CHARACTERISTICS: OPERATIONAL AMPLIFIER (OPA)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated): V_{DD} = 2.7V to 5.5V, T_A = 25°C, V_{CM} = V_{DD}/2, R_L = 100 kΩ to V_{DD}/2, and V_{OUT} ~ V_{DD}/2 Operating Temperature -40°C to +85°C for Industrial				
Param No.	**Parameters**	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
	Input Offset Voltage						
	Input Offset Voltage	V_{OS}	TBD	±2	TBD	mV	Prior to Auto Calibration
	Input Offset Voltage						
	Input Offset Voltage	V_{OS}	TBD	±100	TBD	µV	Following Auto Calibration
	Input Current and Impedance						
	Input Bias Current	I_B	-50	—	+50	nA	Following Auto Calibration
	Input Offset Bias Current	I_{OS}	—	±1	—	pA	
	Common Mode						Following Auto Calibration
	Common Mode Input Range	V_{CM}	V_{SS}	—	V_{DD}-1.4	V	V_{DD} = 5 V
	Common Mode Rejection	CMR	TBD	80	—	dB	V_{CM} = V_{DD}/2, Frequency = DC
	Open Loop Gain						GBWP = 1 following Auto Calibration
	DC Open Loop Gain	A_{OL}	—	90	—	dB	R_L = 25 kΩ connected to V_{DD}/2, 50 mV < V_{OUT} < V_{DD} - 50 mV
	DC Open Loop Gain	A_{OL}	—	80	—	dB	R_L = 5 kΩ connected to V_{DD}/2, 100 mV < V_{OUT} < V_{DD} - 100 mV
	DC Open Loop Gain	A_{OL}	—	TBD	—	dB	GBWP = 0 following Auto Calibration RL = 50 kΩ connected to V_{DD}/2, 50 mV < V_{OUT} < V_{DD} - 50 mV
	DC Open Loop Gain	A_{OL}	—	TBD	—	dB	RL = 100 kΩ connected to V_{DD}/2, 50 mV < V_{OUT} < V_{DD} - 50 mV
	Output						GBWP = 1 Following Auto Calibration
	Output Voltage Swing	V_{OUT}	V_{SS}+0.1	—	V_{DD}-0.1	V	R_L = 5 kΩ connected to V_{DD}/2 V_{DD} = 5 V
	Output Short Circuit Current	I_{SC}	—	25	TBD	mA	
	Power Supply						
	Power Supply Rejection	PSR	—	80	—	dB	Following Auto Calibration
	Auto Calibration Reference	ACR	TBD	1.2	TBD	V	CALREF = 0

P

R

S

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