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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	13
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 8x8b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	20-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lc782-i-so

TABLE 1-1: PIC16C781/782 PINOUT DESCRIPTION

Name	Function	Input Type	Output Type	Description
RA0/AN0/OPA+	RA0	ST	N/A	Port Input
	AN0	AN	—	ADC Input
	OPA+	AN	—	OPAMP Non-inverting Input
RA1/AN1/OPA-	RA1	ST	N/A	Port Input
	AN1	AN	—	ADC Input
	OPA-	AN	—	OPAMP Inverting Input
RA2/AN2/VREF2	RA2	ST	CMOS	Bi-directional I/O
	AN2	AN	—	ADC Input
	VREF2	AN	—	Comparator 2 Voltage Reference Input
RA3/AN3/VREF1	RA3	ST	CMOS	Bi-directional I/O
	AN3	AN	—	ADC Input
	VREF1	AN	—	Comparator 1, ADC, DACREF Input
RA4/T0CKI	RA4	ST	OD	Bi-directional I/O
	TOCKI	ST	—	Timer0 Clock Input
RA5/$\overline{\text{MCLR}}$/VPP	RA5	ST	N/A	Port Input
	$\overline{\text{MCLR}}$	ST	—	Master Clear Input
	VPP	Power	—	Programming Voltage
RA6/OSC2/CLKOUT/T1CKI	RA6	ST	CMOS	Bi-directional I/O
	OSC2	—	XTAL	Crystal/Resonator
	CLKOUT	—	CMOS	Fosc/4 Output
	T1CKI	ST	—	Timer1 Clock Input
RA7/OSC1/CLKIN	RA7	ST	CMOS	Bi-directional I/O
	OSC1	XTAL	—	Crystal/Resonator
	CLKIN	ST	—	External Clock Input
RB0/INT/AN4/VR	RB0	TTL	CMOS	Bi-directional I/O
	INT	ST	—	External Interrupt
	AN4	AN	—	ADC, Comparator Input
	VR	—	AN	Internal Voltage Reference Output
RB1/AN5/VDAC	RB1	TTL	CMOS	Bi-directional I/O
	AN5	AN	—	ADC, Comparator Input
	VDAC	—	AN	DAC Output
RB2/AN6	RB2	TTL	CMOS	Bi-directional I/O
	AN6	AN	—	ADC, Comparator Input
RB3/AN7/OPA	RB3	TTL	CMOS	Bi-directional I/O
	AN7	AN	—	ADC, Comparator Input
	OPA	—	AN	OPAMP Output
RB4	RB4	TTL	CMOS	Bi-directional I/O
RB5	RB5	TTL	CMOS	Bi-directional I/O
RB6/C1/PSMC1A	RB6	TTL	CMOS	Bi-directional I/O
	C1	—	CMOS	Comparator 1 Output
	PSMC1A	—	CMOS	PSMC Output 1A

TABLE 2-1: PIC16C781/782 SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

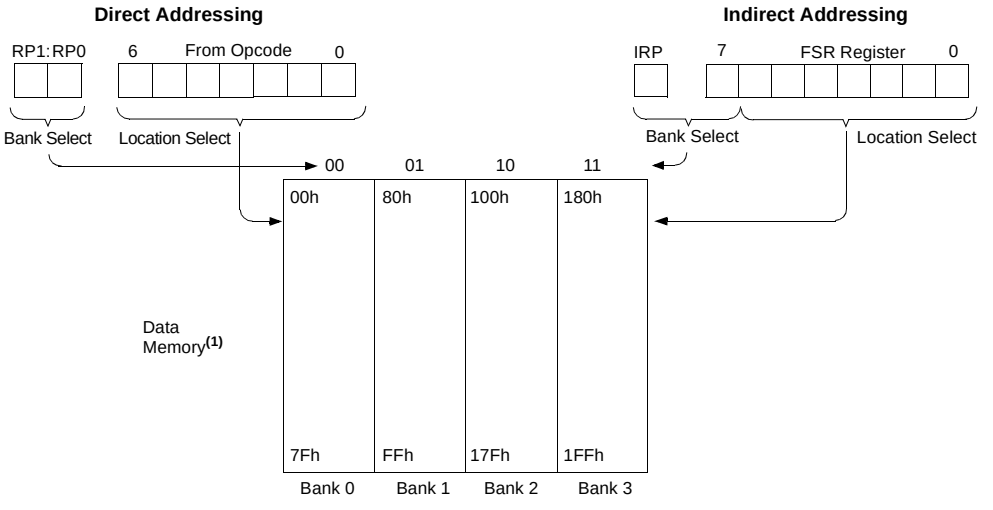
Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Details on Page:
Bank 2											
100h(2)	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								0000 0000	23
101h	TMR0	Timer0 Module's Register								xxxx xxxx	51
102h(2)	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	23
103h(2)	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	17
104h(2)	FSR	Indirect Data Memory Address Pointer								xxxx xxxx	23
105h	—	Unimplemented								—	—
106h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx 0000	35
107h	—	Unimplemented								—	—
108h	—	Unimplemented								—	—
109h	—	Unimplemented								—	—
10Ah(1,2)	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter					---0 0000	23
10Bh(2)	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	19
10Ch	PMDATL	PMD7	PMD6	PMD5	PMD4	PMD3	PMD2	PMD1	PMD0	0000 0000	48
10Dh	PMADRL	PMA7	PMA6	PMA5	PMA4	PMA3	PMA2	PMA1	PMA0	xxxx xxxx	48
10Eh	PMDATH	—	—	PMD13	PMD12	PMD11	PMD10	PMD9	PMD8	--00 0000	47
10Fh	PMADRH	—	—	—	Reserved	Reserved	PMA10	PMA9	PMA8	---x xxxx	48
110h	CALCON	CAL	CALERR	CALREF	—	—	—	—	—	000- ----	85
111h	PSMCCON0	SMCCL1	SMCCL0	MINDC1	MINDC0	MAXDC1	MAXDC0	DC1	DC0	0000 0000	104
112h	PSMCCON1	SMCON	S1APOL	S1BPOL	—	SCEN	SMCOM	PWM/$\overline{PSM}$	SMCCS	000- 0000	104
113h	—	Unimplemented								—	—
114h	—	Unimplemented								—	—
115h	—	Unimplemented								—	—
116h	—	Unimplemented								—	—
117h	—	Unimplemented								—	—
118h	—	Unimplemented								—	—
119h	CM1CON0	C1ON	C1OUT	C1OE	C1POL	C1SP	C1R	C1CH1	C1CH0	0000 0000	91
11Ah	CM2CON0	C2ON	C2OUT	C2OE	C2POL	C2SP	C2R	C2CH1	C2CH0	0000 0000	93
11Bh	CM2CON1	MC1OUT	MC2OUT	—	—	—	—	—	C2SYNC	00-- ---0	94
11Ch	OPACON	OPAON	CMPEN	—	—	—	—	—	GBWP	00-- ---0	84
11Dh	—	Unimplemented								—	—
11Eh	DAC	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0	0000 0000	79
11Fh	DACON0	DAON	DAOE	—	—	—	—	DARS1	DARS0	00-- --00	79

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0'.
Shaded locations are unimplemented, read as '0'.

Note 1: The upper byte of the program counter is not directly accessible. PCLATH is a holding register for the PC<12:8> whose contents are transferred to the upper byte of the program counter. See Section 2.9 for more detail.

2: These registers can be addressed from any bank.

FIGURE 2-5: DIRECT/INDIRECT ADDRESSING



Note 1: For register file map detail, see Figure 2-3.

2.12 Effect of RESET on Core Registers

Refer to Table 2-2 for the effect of a RESET operation on core registers.

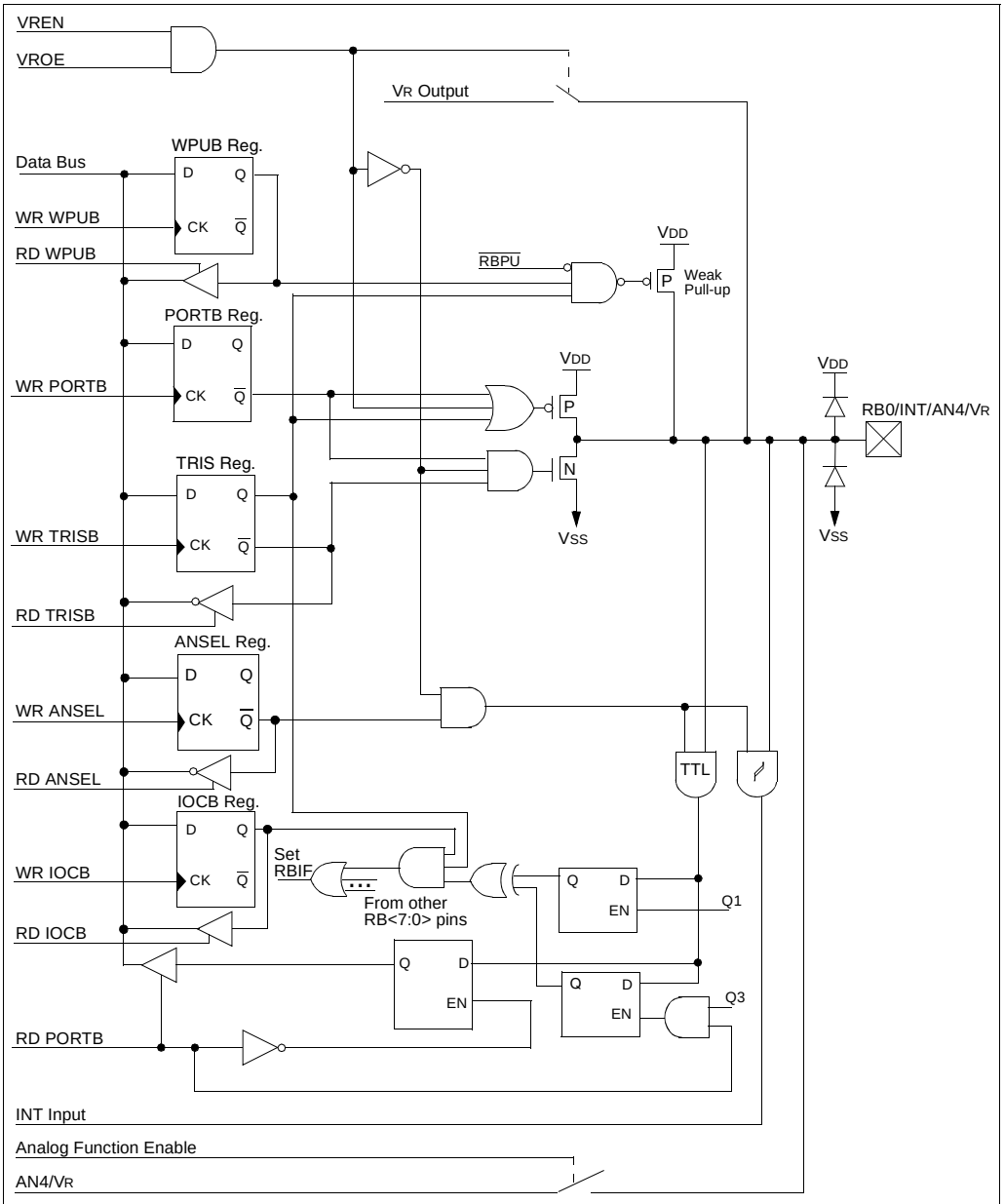
TABLE 2-2: EFFECT OF RESET ON CORE REGISTERS

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other RESETS(1)
Bank 0											
00h	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								0000 0000	0000 0000
02h	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	0000 0000
04h	FSR	Indirect Data Memory Address Pointer								xxxx xxxx	uuuu uuuu
0Ah	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter					---0 0000	---0 0000
0Ch	PIR1	LVDIF	ADIF	C2IF	C1IF	—	—	—	TMR1IF	0000 ---0	0000 ---0
Bank 1											
81h	OPTION_REG	$\overline{RBPU}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	xxxx xxxx	1111 1111
83h	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	000q quuu
8Bh	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
8Ch	PIE1	LVDIE	ADIE	C2IE	C1IE	—	—	—	TMR1IE	0000 ---0	0000 ---0
8Eh	PCON	—	—	—	WDTON	OSCF	—	$\overline{POR}$	$\overline{BOR}$	---q 1-qq	---q 1-qq

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0'.
Shaded locations are unimplemented, read as '0'.

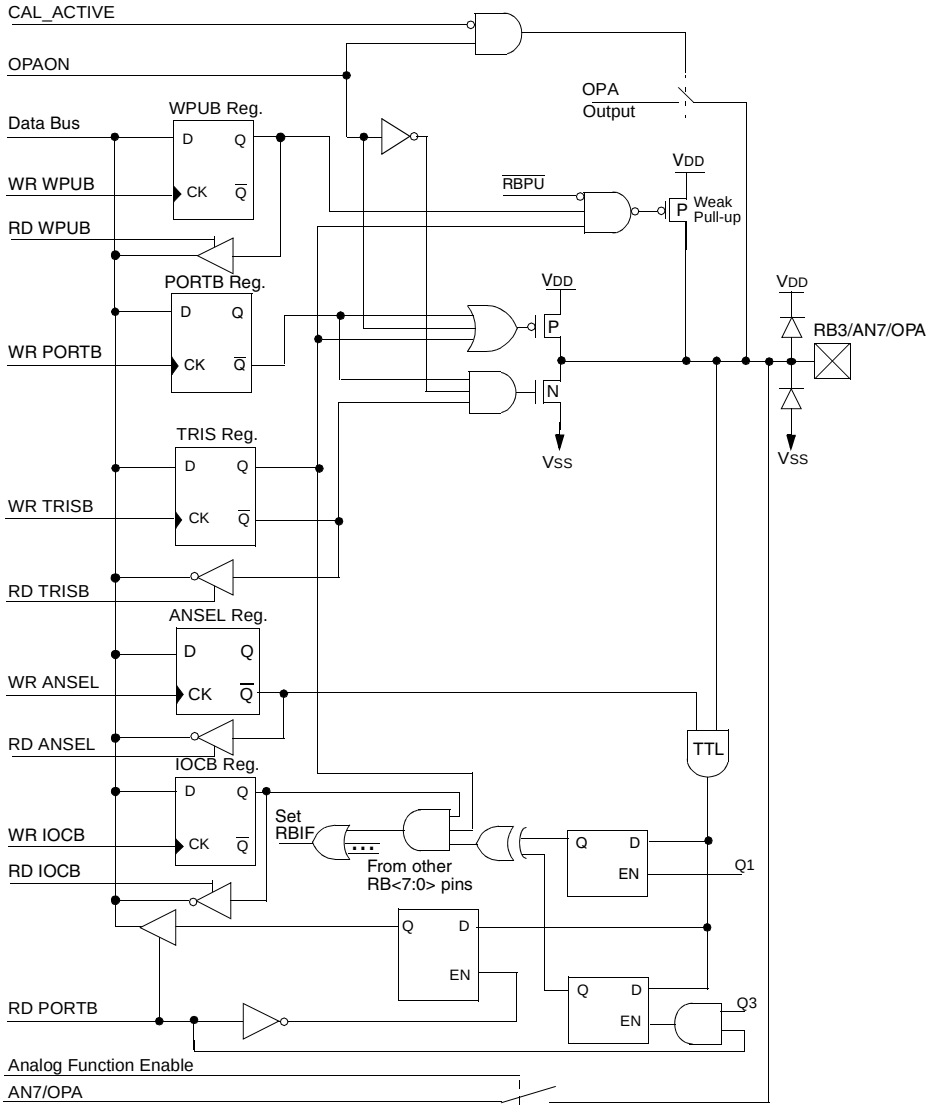
Note 1: Other (non power-up) RESETS include external RESET through $\overline{MCLR}$ and Watchdog Timer Reset.

FIGURE 3-9: BLOCK DIAGRAM OF RB0/INT/AN4/VR PIN



VREN & VROE	ANSEL<4>	TRISB<0>	FUNCTION	PORTB<0> READ
0	0	1	Digital In	Pin
0	0	0	Digital Out	Pin
0	1	x	Analog In	0
1	x	x	Analog Out	0

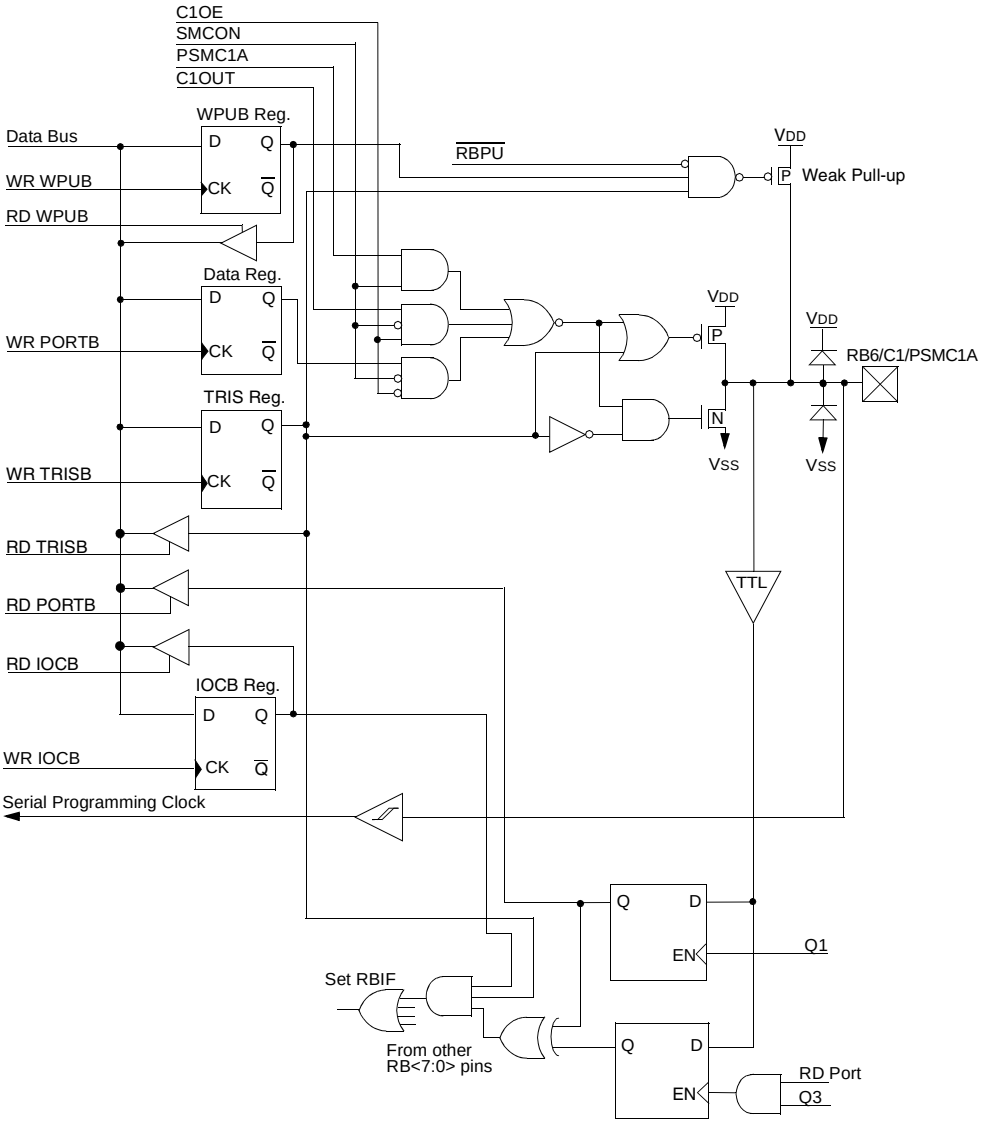
FIGURE 3-12: BLOCK DIAGRAM OF RB3/AN7/OPA PIN



OPA MODULE		ANSEL<7>	ADC/C1/C2 INPUT	FUNCTION	PORTB<3> READ
OPAON	CAL_ACTIVE				
0	x	0	Digital	Digital I/O	Pin
0	x	1	Analog	Analog In	0
1	0	1	Analog	OPA Output	0
1	1	1	Analog HI-Z	Calibration	0

Analog HI-Z = No internal drive on pin (analog input) during calibration.

FIGURE 3-15: BLOCK DIAGRAM OF RB6/C1/PSMC1A PIN



PSMC SMCON	COMPARATOR C1OE	PORTB TRISB<6>	FUNCTION
x	x	1	Digital In
0	0	0	Digital Out
0	1	0	C1OUT
1	x	0	PSMC1A

12.0 COMPARATOR MODULE

The comparator module has two separate voltage comparators: Comparator C1 and Comparator C2 (see Figure 12-1).

Each comparator offers the following list of features:

- Control and configuration register
- Comparator output available externally
- Programmable output polarity
- Interrupt-on-change flags
- Wake-up from SLEEP
- Configurable as feedback input to the PSMC
- Programmable four input multiplexer
- Programmable reference selections
- Programmable speed
- Output synchronization to Timer1 clock input (Comparator C2 only)

12.1 Control Registers

Both comparators have separate control and configuration registers: CM1CON0 for C1 and CM2CON0 for C2. In addition, Comparator C2 has a second control register, CM2CON1, for synchronization control and simultaneous reading of both comparator outputs.

12.1.1 COMPARATOR C1 CONTROL REGISTER

The CM1CON0 register (shown in Register 12-1) contains the control and status bits for the following:

- Comparator enable
- Comparator input selection
- Comparator reference selection
- Output mode
- Comparator speed

Setting C1ON (CM1CON0<7>) enables Comparator C1 for operation.

Bits C1CH<1:0> (CM1CON0<1:0>) select the comparator input from the four analog pins AN<7:4>.

Note:	To use AN<7:4> as analog inputs, the appropriate bits must be programmed in the ANSEL register.

Setting C1R (CM1CON0<2>) selects the output of the DAC module as the reference voltage for the comparator. Clearing C1R selects the VREF1 input on the RA3/AN3/VREF1 pin.

The output of the comparator is available internally via the C1OUT flag (CM1CON0<6>). To make the output available for an external connection, the C1OE flag (CM1CON0<5>) must be set. If the module is disabled with C1OE set, the output will be driven as shown in Table 12-2:

The polarity of the comparator output can be inverted by setting the C1POL flag (CM1CON0<4>). Clearing C1POL results in a non-inverted output. A complete table showing the output state versus input conditions and the polarity bit is shown in Table 12-2.

TABLE 12-1: OUTPUT STATE VERSUS INPUT CONDITIONS

Input Condition	C1POL	C1OUT
C1VN > C1VP	0	0
C1VN < C1VP	0	1
C1VN > C1VP	1	1
C1VN < C1VP	1	0

Note 1:	The internal output of the comparator is latched at the end of each instruction cycle. External outputs are not latched.
2:	The C1 interrupt will operate correctly with C1OE set or cleared.
3:	For the output of C1 on RB6/C1/PSMC1A, the PSMC must be disabled and TRISB<6> must be '0'.

C1SP (CM1CON0<3>) configures the speed of the comparator. When C1SP is set, the comparator operates at its normal speed. Clearing C1SP operates the comparator in a slower, low power mode.

REGISTER 13-1: PSMC CONTROL REGISTER0 (PSMCCON0: 111h)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SMCCL1	SMCCL0	MINDC1	MINDC0	MAXDC1	MAXDC0	DC1	DC0
bit 7							bit 0

bit 7-6 **SMCCL<1:0>:** Clock Frequency Select bits
00 = Output frequency for single output mode is FOSC/128
01 = Output frequency for single output mode is FOSC/64
10 = Output frequency for single output mode is FOSC/32
11 = Output frequency for single output mode is FOSC/16

bit 5-4 **MINDC<1:0>:** Minimum Duty Cycle Select bits for PWM Mode
00 = Min duty cycle of 0
01 = Min duty cycle of 1/8
10 = Min duty cycle of 1/4
11 = Min duty cycle of 3/8

bit 3-2 **MAXDC<1:0>:** Maximum Duty Cycle Select bits for PWM Mode
00 = Max duty cycle of 1/2
01 = Max duty cycle of 5/8
10 = Max duty cycle of 3/4
11 = Max duty cycle of 15/16

bit 1-0 **DC<1:0>:** Duty Cycle Select bits for PSM Mode
00 = Duty cycle of 1/8
01 = Duty cycle of 3/8
10 = Duty cycle of 5/8
11 = Duty cycle of 15/16

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

14.0 SPECIAL FEATURES OF THE CPU

These devices have a host of features intended to maximize system reliability, minimize cost through elimination of external components, provide power saving operating modes and offer code protection. These features include:

- Oscillator selection
- RESET
  - Power-on Reset (POR)
  - Power-up Timer (PWRT)
  - Oscillator Start-up Timer (OST)
  - Programmable Brown-out Reset (PBOR)
- Interrupts
- Watchdog Timer (WDT)
- Programmable Low Voltage Detection (PLVD)
- SLEEP
- Code protection
- ID locations
- In-Circuit Serial Programming™ (ICSP™)

Several oscillator options are available to allow the part to fit the application. The INTRC oscillator options save system cost while the LP crystal option saves power. A set of configuration bits is used to select various options.

The CPU also features a Watchdog Timer (WDT), which can be enabled either through a configuration bit during programming, or by the software. For added reliability, the WDT runs off its own internal RC oscillator instead of the main CPU clock.

In addition to the WDT, the CPU incorporates both an Oscillator Start-up Timer and a Power-up Timer. The Oscillator Start-up Timer (OST) is intended to hold the chip in RESET until the crystal oscillator has stabilized. The Power-up Timer (PWRT) holds the CPU in a fixed RESET delay of 72ms (nominal) on Power-up Resets (POR and PBOR), while the power supply stabilizes. With these two timers on-chip, most applications need no external RESET circuitry.

SLEEP mode is designed to offer a very low current power-down mode. The user can awaken from SLEEP through:

- External RESET
- Watchdog Timer Wake-up
- Interrupt

Additional information on special features is available in the PIC Mid-Range Reference Manual, (DS33023).

14.1 Configuration Bits

The configuration bits can be programmed (read as '0'), or left unprogrammed (read as '1'), to select various device configurations. These bits are mapped in program memory location 2007h.

Note:	Address 2007h is beyond the user program memory space, which can be accessed only during programming.

Some of the core features provided may not be necessary for each application in which a device may be used. The configuration word bits allow these features to be configured/enabled/disabled as necessary. These features include:

- Code Protection
- PBOR Trip Point
- Power-up Timer
- Watchdog Timer
- Device Oscillator Mode

As can be seen in Table 14-1, some additional configuration word bits have been provided for Brown-out Reset trip point selection.

REGISTER 14-2: POWER CONTROL REGISTER (PCON: 8Eh)

U-0	U-0	U-0	R/W-q	R/W-1	U-0	R/W-q	R/W-x
—	—	—	WDTON	OSCF	—	$\overline{\text{POR}}$	$\overline{\text{BOR}}$
bit 7							bit 0

bit 7-5 **Unimplemented:** Read as '0'

bit 4 **WDTON:** WDT Software Enable bit

If WDTE bit (Configuration Word <3>) = 1:
This bit is not writable, always reads '1'

If WDTE bit (Configuration Word <3>) = 0:
1 = WDT is enabled
0 = WDT is disabled and cleared

bit 3 **OSCF:** Oscillator Speed bit (pending on new internal oscillator decision)

INTRC mode:
1 = 4 MHz typical
0 = 37 kHz typical

All other oscillator modes:
Ignored

bit 2 **Unimplemented:** Read as '0'

bit 1 **$\overline{\text{POR}}$:** Power-on Reset Status bit

1 = No Power-on Reset occurred
0 = A Power-on Reset occurred (must be set in software after a Power-on Reset occurs)

bit 0 **$\overline{\text{BOR}}$:** Brown-out Reset Status bit

1 = No Brown-out Reset occurred
0 = A Brown-out Reset occurred (must be set in software after a Brown-out Reset occurs)

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared
x = Bit is unknown	'q' = Value depends on condition	

TABLE 14-4: STATUS BITS AND THEIR SIGNIFICANCE

$\overline{\text{POR}}$	$\overline{\text{BOR}}$	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Bit Significance
0	1	1	1	Power-on Reset
0	x	0	x	Illegal, $\overline{\text{TO}}$ is set on $\overline{\text{POR}}$
0	x	x	0	Illegal, $\overline{\text{PD}}$ is set on $\overline{\text{POR}}$
1	0	1	1	Brown-out Reset
1	1	0	1	WDT Reset
1	1	0	0	WDT Wake-up
1	1	u	u	$\overline{\text{MCLR}}$ Reset during normal operation
1	1	1	0	$\overline{\text{MCLR}}$ Reset during SLEEP or interrupt wake-up from SLEEP

TABLE 14-5: RESET CONDITION FOR SPECIAL REGISTERS

Condition	Program Counter	STATUS Register	PCON Register
Power-on Reset	000h	0001 1xxx	---0 1-01
$\overline{MCLR}$ Reset during normal operation	000h	000u uuuu	---0 1-uu
$\overline{MCLR}$ Reset during SLEEP	000h	0001 0uuu	---0 1-uu
WDT Reset	000h	0000 1uuu	---0 1-uu
WDT Wake-up	PC + 1	uuu0 0uuu	---0 u-uu
Brown-out Reset	000h	0001 1uuu	---0 1-u0
Interrupt wake-up from SLEEP, GIE = 0	PC + 1	uuu1 0uuu	---u u-uu
Interrupt wake-up from SLEEP, GIE = 1	0004h	uuu1 0uuu	---u u-uu

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as '0'.

FIGURE 14-6: TIME-OUT SEQUENCE ON POWER-UP ($\overline{MCLR}$ TIED TO VDD)

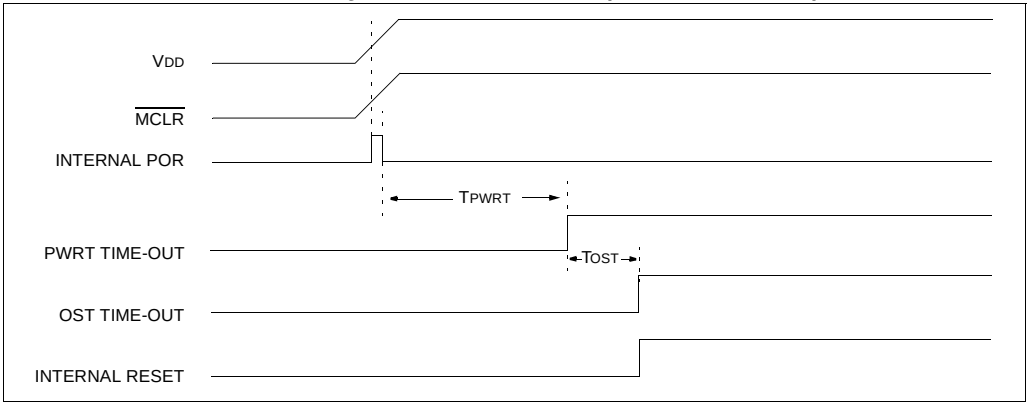
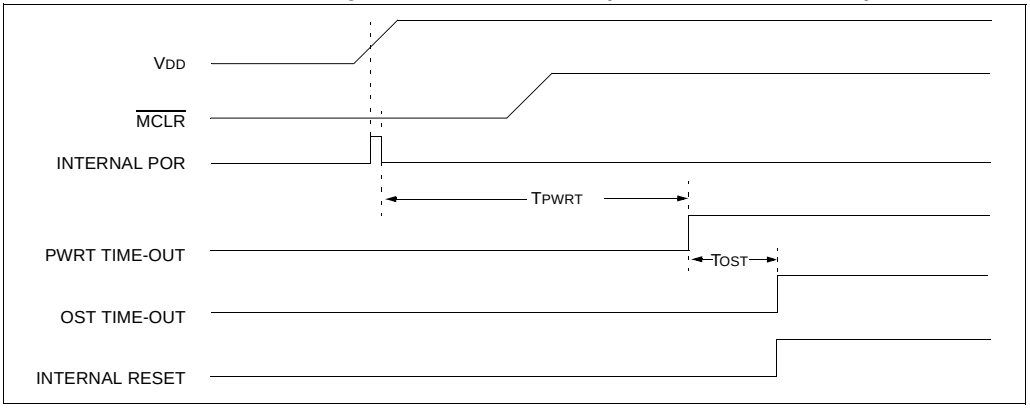


FIGURE 14-7: TIME-OUT SEQUENCE ON POWER-UP ($\overline{MCLR}$ NOT TIED TO VDD)



14.9.2 TMR0 INTERRUPT

An overflow (FFh → 00h) in the TMR0 register sets the flag bit, T0IF (INTCON<2>). The interrupt can be enabled/disabled by setting/clearing enable bit, T0IE (INTCON<5>) (Section 2.5).

14.9.3 PORTB INTERRUPT-ON-CHANGE (IOCB)

An input change on PORTB<7:0> sets flag bit RBIF (INTCON<0>). The PORTB pin(s) which can individually generate interrupt are selectable in the IOCB register. The interrupt can be enabled/disabled by setting/clearing enable bit RBIE (INTCON<4>) (Section 2.5). PORTB must be configured as a digital input.

14.10 Context Saving During Interrupts

During an interrupt, only the PC is saved on the stack. At minimum, W and STATUS should be saved to preserve the context for the interrupted program. All registers that may be corrupted by the Interrupt Service Routine (ISR), such as PCLATH or FSR, should be saved.

Example 14-1 stores and restores the STATUS, W and PCLATH registers. The register, W_TEMP, is defined in Common RAM, the last 16 bytes of each bank that may be accessed from any bank. The STATUS_TEMP and PCLATH_TEMP are defined in bank 0.

The example:

a) Stores the W register.
b) Stores the STATUS register in bank 0.
c) Stores the PCLATH register in bank 0.
d) Executes the ISR code.
e) Restores the PCLATH register.
f) Restores the STATUS register.
g) Restores W.

Note:	The W_TEMP, STATUS_TEMP and PCLATH_TEMP are defined in the common RAM area (70h - 7Fh) to avoid register bank switching during context save and restore.

EXAMPLE 14-1: SAVING STATUS, W, AND PCLATH REGISTERS

```
#define    W_TEMP          0x70
#define    STATUS_TEMP     0x71
#define    PCLATH_TEMP     0x72
    org    0x04            ; Int Vector
    MOVWF   W_TEMP         ; Save W
    MOVF   STATUS,w
    MOVWF  STATUS_TEMP     ; save STATUS
    MOVF   PCLATH,w
    MOVWF  PCLATH_TEMP     ; save PCLATH
    :
    (Interrupt Service Routine)
    :
    MOVF   PCLATH_TEMP,w
    MOVWF  PCLATH
    MOVF   STATUS_TEMP,w
    MOVWF  STATUS
    SWAPF  W_TEMP,f        ; swapf loads W
    SWAPF  W_TEMP,w        ; w/o affect STATUS
    RETFIE
```

14.11 Watchdog Timer (WDT)

The Watchdog Timer uses a free running, on-chip RC oscillator, which does not require any external components. This oscillator is independent from the processor clock. The WDT runs even if the main clock of the device has been stopped (for example, by execution of a SLEEP instruction).

During normal operation, a WDT time-out generates a device RESET (Watchdog Timer Reset). If the device is in SLEEP mode, a WDT time-out causes the device to wake-up and continue with normal operation (Watchdog Timer Wake-up). The $\overline{TO}$ bit in the STATUS register is cleared upon a Watchdog Timer time-out.

The WDT can be permanently enabled by programming the configuration bit WDTE, or by software via the WDTON bit in the Power Control register (PCON: 8EH). See Section 14.8 and Section 14.1.

WDT time-out period values may be found in the Electrical Specifications. Values for the WDT prescaler may be assigned using the OPTION_REG register.

Note 1:	The CLRWDT and SLEEP instructions clear the WDT and the postscaler, if assigned to the WDT.
2:	When a CLRWDT instruction is executed and the prescaler is assigned to the WDT, the prescaler count is cleared, but the prescaler assignment is not changed.

15.0 INSTRUCTION SET SUMMARY

Each PIC16CXXX instruction is a 14-bit word divided into an OPCODE which specifies the instruction type and one or more operands which further specify the operation of the instruction. The PIC16CXXX instruction set summary in Table 15-2 lists **byte-oriented**, **bit-oriented**, and **literal and control** operations. Table 15-1 shows the opcode field descriptions.

For **byte-oriented** instructions, 'f' represents a file register designator and 'd' represents a destination designator. The file register designator specifies which file register is to be used by the instruction.

The destination designator specifies where the result of the operation is to be placed. If 'd' is zero, the result is placed in the W register. If 'd' is one, the result is placed in the file register specified in the instruction.

For **bit-oriented** instructions, 'b' represents a bit field designator which selects the number of the bit affected by the operation, while 'f' represents the number of the file in which the bit is located.

For **literal and control** operations, 'k' represents an eight or eleven bit constant or literal value.

TABLE 15-1: OPCODE FIELD DESCRIPTIONS

Field	Description
f	Register file address (0x00 to 0x7F)
W	Working register (accumulator)
b	Bit address within an 8-bit file register
k	Literal field, constant data or label
x	Don't care location (= 0 or 1) The assembler will generate code with x = 0. It is the recommended form of use for compatibility with all Microchip software tools.
d	Destination select; d = 0: store result in W, d = 1: store result in file register f. Default is d = 1
PC	Program Counter
TO	Time-out bit
PD	Power-down bit

The instruction set is highly orthogonal and is grouped into three basic categories:

- **Byte-oriented** operations
- **Bit-oriented** operations
- **Literal and control** operations

All instructions are executed within one single instruction cycle, unless a conditional test is true or the program counter is changed as a result of an instruction. In this case, the execution takes two instruction cycles with the second cycle executed as a NOP. One instruction cycle consists of four oscillator periods. Thus, for an oscillator frequency of 4 MHz, the normal instruction execution time is 1 μs. If a conditional test is true or the program counter is changed as a result of an instruction, the instruction execution time is 2 μs.

Table 15-2 lists the instructions recognized by the MPASM™ assembler.

Figure 15-1 shows the general formats that the instructions can have.

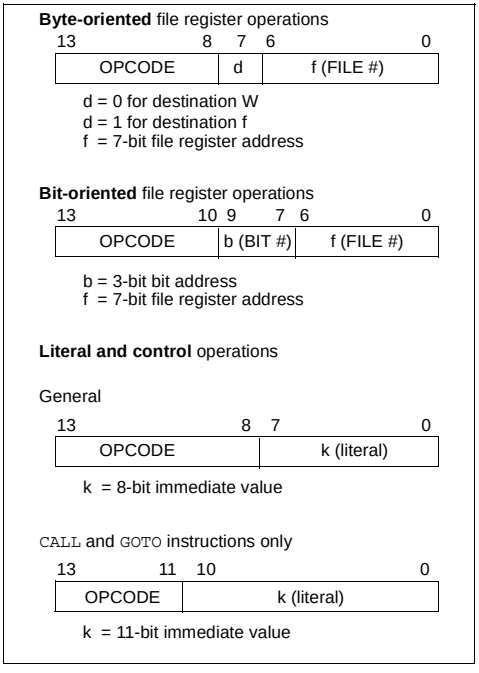
Note: To maintain upward compatibility with future PIC16CXXX products, do not use the OPTION and TRIS instructions.

All examples use the following format to represent a hexadecimal number:

0xhh

where h signifies a hexadecimal digit.

FIGURE 15-1: GENERAL FORMAT FOR INSTRUCTIONS



A description of each instruction is available in the PIC Mid-Range Reference Manual, (DS33023).

XORWF	Exclusive OR W with f
Syntax:	[*label*] XORWF f,d
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	(W) .XOR. (f) $\rightarrow$ (destination)
Status Affected:	Z
Description:	Exclusive OR the contents of the W register with register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.

17.2 DC Characteristics: Input/Output Pins

TABLE 17-2: DC CHARACTERISTICS: PIC16C781/782, DSTEMP (INDUSTRIAL)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial and Operating voltage VDD range as described in DC spec Section 17-1				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
		Input Low Voltage					
	VIL	I/O ports:					
D030		with TTL buffer	VSS	—	0.15VDD	V	For entire VDD range
D030A			VSS	—	0.8V	V	4.5V ≤ VDD ≤ 5.5V
D031		with Schmitt Trigger buffer	VSS	—	0.2VDD	V	For entire VDD range
D032		$\overline{MCLR}$	VSS	—	0.2VDD	V	
D033		OSC1 (in XT, HS, LP and EC)	VSS	—	0.3 VD	V	
		Input High Voltage					
	VIH	I/O ports:		—			
D040		with TTL buffer	2.0	—	VDD	V	4.5V ≤ VDD ≤ 5.5V
D040A			(0.25VDD + 0.8V)	—	VDD	V	For entire VDD range
D041		with Schmitt Trigger buffer	0.8VDD	—	VDD	V	For entire VDD range
D042		$\overline{MCLR}$	0.8VDD	—	VDD	V	
D042A		OSC1 (XT, HS, LP and EC)	0.7VDD	—	VDD	V	
D070	IPURB	**PORTB Weak Pull-up Current Per Pin**	50	250	400	µA	VDD = 5V, VPIN = VSS
		Input Leakage Current(1,2)					
D060	IIL	I/O ports (with digital functions)	—	—	±1	µA	Vss ≤ VPIN ≤ VDD, Pin at hi-impedance
D060A	IIL	I/O ports (with analog functions)	—	—	±100	nA	Vss ≤ VPIN ≤ VDD, Pin at hi-impedance
D061		RA5/$\overline{MCLR}$/VPP	—	—	±5	µA	Vss ≤ VPIN ≤ VDD
D063		OSC1	—	—	±5	µA	Vss ≤ VPIN ≤ VDD, XT, HS, LP and EC osc configuration
		Output Low Voltage					
D080	VOL	I/O ports (Includes CLKOUT)	—	—	0.6	V	IOL = 8.5 mA, VDD = 4.5V
		Output High Voltage					
D090	VOH	I/O ports(2) (Includes CLKOUT)	VDD - 0.7	—	—	V	IOH = -3.0 mA, VDD = 4.5V
D150*	VOD	**Open Drain High Voltage**	—	—	10.5	V	RA4 pin
		Capacitive Loading Specs on Output Pins*					
D100	Cosc2	OSC2 pin	—	—	15	pF	In XT, HS and LP modes when external clock is used to drive OSC1.
D101	CIO	All I/O pins and OSC2 (in RC mode)	—	—	50	pF	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

2: Negative current is defined as current sourced by the pin.

17.4 Operational Amplifier

TABLE 17-8: DC CHARACTERISTICS: OPERATIONAL AMPLIFIER (OPA)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated): V_{DD} = 2.7V to 5.5V, T_A = 25°C, V_{CM} = V_{DD}/2, R_L = 100 kΩ to V_{DD}/2, and V_{OUT} ~ V_{DD}/2 Operating Temperature -40°C to +85°C for Industrial				
Param No.	**Parameters**	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
	Input Offset Voltage						
	Input Offset Voltage	V_{OS}	TBD	±2	TBD	mV	Prior to Auto Calibration
	Input Offset Voltage						
	Input Offset Voltage	V_{OS}	TBD	±100	TBD	µV	Following Auto Calibration
	Input Current and Impedance						
	Input Bias Current	I_B	-50	—	+50	nA	Following Auto Calibration
	Input Offset Bias Current	I_{OS}	—	±1	—	pA	
	Common Mode						Following Auto Calibration
	Common Mode Input Range	V_{CM}	V_{SS}	—	V_{DD}-1.4	V	V_{DD} = 5 V
	Common Mode Rejection	CMR	TBD	80	—	dB	V_{CM} = V_{DD}/2, Frequency = DC
	Open Loop Gain						GBWP = 1 following Auto Calibration
	DC Open Loop Gain	A_{OL}	—	90	—	dB	R_L = 25 kΩ connected to V_{DD}/2, 50 mV < V_{OUT} < V_{DD} - 50 mV
	DC Open Loop Gain	A_{OL}	—	80	—	dB	R_L = 5 kΩ connected to V_{DD}/2, 100 mV < V_{OUT} < V_{DD} - 100 mV
	DC Open Loop Gain	A_{OL}	—	TBD	—	dB	GBWP = 0 following Auto Calibration RL = 50 kΩ connected to V_{DD}/2, 50 mV < V_{OUT} < V_{DD} - 50 mV
	DC Open Loop Gain	A_{OL}	—	TBD	—	dB	RL = 100 kΩ connected to V_{DD}/2, 50 mV < V_{OUT} < V_{DD} - 50 mV
	Output						GBWP = 1 Following Auto Calibration
	Output Voltage Swing	V_{OUT}	V_{SS}+0.1	—	V_{DD}-0.1	V	R_L = 5 kΩ connected to V_{DD}/2 V_{DD} = 5 V
	Output Short Circuit Current	I_{SC}	—	25	TBD	mA	
	Power Supply						
	Power Supply Rejection	PSR	—	80	—	dB	Following Auto Calibration
	Auto Calibration Reference	ACR	TBD	1.2	TBD	V	CALREF = 0

TABLE 17-9: AC CHARACTERISTICS: OPERATIONAL AMPLIFIER (OPA)

AC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated): V_{DD} = 2.7V to 5.5V, V_{SS} = GND, T_A = 25°C, VCM = V_{DD}/2, RL = 100kΩ to V_{DD}/2, and V_{OUT} = V_{DD}/2 Operating Temperature -40°C to +85°C for Industrial				
Param No.	**Parameters**	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
	Gain Bandwidth Product	GBWP	—	75	—	kHz	V_{DD} = 5V, GBWP = 0
		GBWP	—	2	—	MHz	V_{DD} = 5V, GBWP = 1
	Input Offset Auto	T_Z	—	300	TBD	µs	V_{DD} = 5V, GBWP = 1
	Calibration Time	T_Z	—	TBD	TBD	µs	V_{DD} = 5V GBWP = 0
		T_{ON}	—	10	TBD	µs	V_{DD} = 5V, GWBP = 1
	Turn On Time	T_{ON}	—	TBD	TBD	µs	V_{DD} = 5V, GBWP = 0
	Phase Margin	ΘM	—	TBD	—	degrees	V_{DD} = 5V, GBWP = 0
		ΘM	—	TBD	—	degrees	V_{DD} = 5V, GBWP = 1
	Slew Rate	SR	—	TBD	—	V/µs	V_{DD} = 5V, GBWP = 0
		SR	—	TBD	—	V/µs	V_{DD} = 5V, GBWP = 1

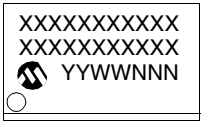
Note: Data in 'Typ' column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

NOTES:

19.0 PACKAGING INFORMATION

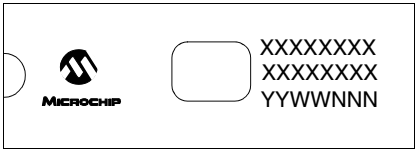
19.1 Package Marking Information

20-Lead SSOP

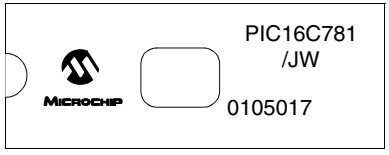


Example

20-Lead CERDIP Windowed

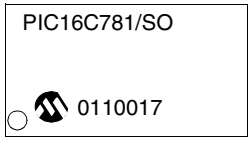


Example

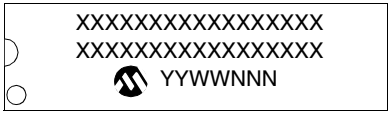


20-Lead SOIC

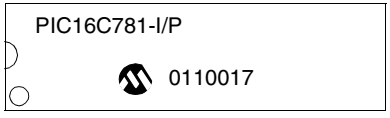
Example



20-Lead PDIP



Example



Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

P