Welcome to E-XFL.COM

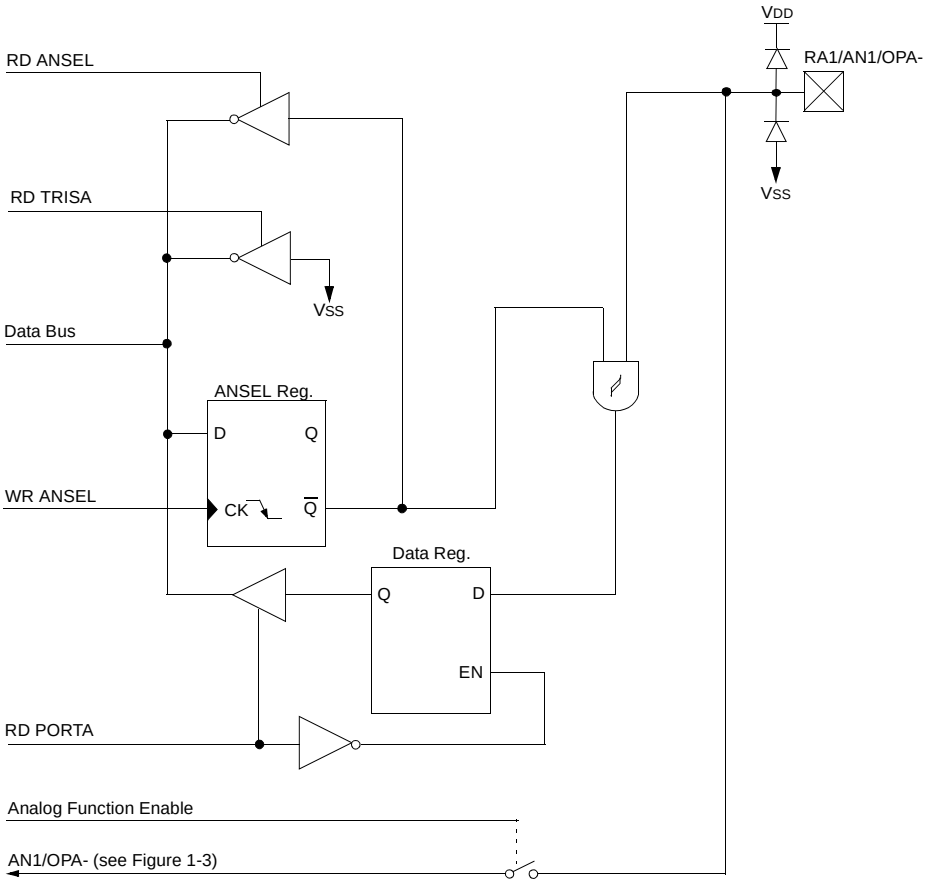
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

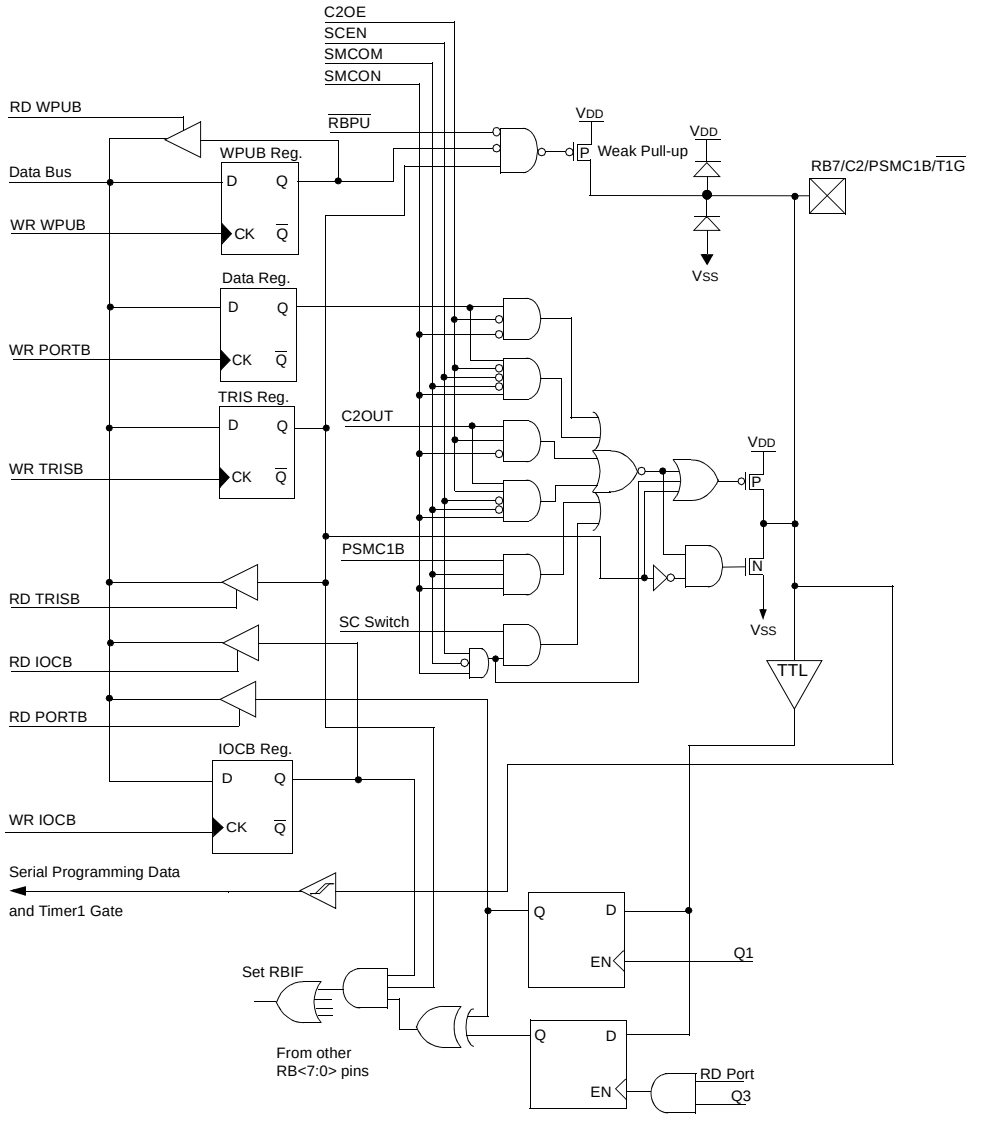
Details	
Product Status	Obsolete
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	13
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 8x8b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	20-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lc782t-i-so

FIGURE 3-2: BLOCK DIAGRAM OF RA1/AN1/OPA- PIN



ANSEL<1>	TRISA<1>	FUNCTION	PORTA<1> READ
0	x	Digital In	Pin
1	x	Analog In	0

FIGURE 3-16: BLOCK DIAGRAM OF RB7/C2/PSMC1B/$\overline{T1G}$ PIN



PSMC MODULE			COMPARATOR C2OE	PORTB TRISB<7>	FUNCTION
SMCON	SMCOM	SCEN			
x	x	x	x	1	Digital In
0	x	x	0	0	Digital Out
1	0	0	0	0	Digital Out
0	x	x	1	0	C2OUT
1	0	0	1	0	C2OUT
1	0	1	x	0	Slope Compensation
1	1	x	x	0	PSMC1B

NOTES:

4.0 PROGRAM MEMORY READ (PMR)

Program memory is readable during normal operation (full VDD range). It is read by indirect addressing through the following Special Function Registers:

- PMCON1: Control
- PMDATH: Data High
- PMDATL: Data Low
- PMADRH: Address High
- PMADRL: Address Low

When interfacing to the program memory block, the PMDATH and PMDATL registers form a 2-byte word, which holds the 14-bit data. The PMADRH and PMADRL registers form a 2-byte word, which holds the 12-bit address of the program memory location being accessed. Mid-range devices have up to 8K words of program EPROM with an address range from 0h to 3FFFh. When the device contains less memory than the full address range of the PMADRH:PMARDL registers, the Most Significant bits of the PMADRH register are ignored.

4.1 PMCON1 Register

PMCON1 is the control register for program memory accesses.

Control bit RD initiates a read operation. This bit cannot be cleared, only set, in software. It is cleared in hardware at completion of the read operation.

4.2 PMDATH and PMDATL Registers

The PMDATH:PMDATL registers are loaded with the contents of program memory addressed by the PMADRH and PMADRL registers upon completion of a Program Memory Read command.

REGISTER 4-1: PROGRAM MEMORY READ CONTROL REGISTER 1 (PMCON1: 18Ch)

R-1	U-0	U-0	U-0	U-0	U-0	U-0	R/S-0
Reserved	—	—	—	—	—	—	RD
bit7							bit0

bit 7 **Reserved:** Read as ‘1’

bit 6-1 Unimplemented: Read as '0

bit 0 RD: Read Control bit

1 = Initiates a Program memory read (read takes 2 cycles, RD is cleared in hardware)
0 = Reserved

Legend:			
S = Settable bit			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
- n = Value at POR	’1’ = Bit is set	’0’ = Bit is cleared	x = Bit is unknown

REGISTER 4-2: PROGRAM MEMORY DATA HIGH (PMDATH: 10Eh)

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	PMD13	PMD12	PMD11	PMD10	PMD9	PMD8
bit7							bit0

bit 7-6 **Unimplemented:** Read as '0

bit 5-0 **PMD<13:8>:** Program Memory Data bits
The value of the program memory word pointed to by PMADRH and PMADRL after a program memory read command.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
- n = Value at POR	’1’ = Bit is set	’0’ = Bit is cleared	x = Bit is unknown

6.2 Control Register T1CON

Control and configuration of Timer1 is by means of the T1CON register shown in Register 6-1.

Timer1 is enabled by setting the TMR1ON bit (T1CON<0>). Clearing TMR1ON stops the timer, but does not clear the Timer1 register.

The TMR1CS bit (T1CON<1>) determines the Timer mode. When TMR1CS is set, the timer is configured as a counter and receives its clock from RA6/OSC2/CLKOUT/T1CKI. When cleared, the timer is configured as a timer and its clock is derived from FOSC/4.

The $\overline{\text{T1SYNC}}$ bit (T1CON<2>) determines Timer1's synchronization. If cleared, the timer clock is synchronized to the system clock. If set, the timer is asynchronous.

The Timer1 clock gate function is enabled by setting the TMR1GE bit (T1CON<6>). When TMR1GE is set, the $\overline{\text{T1G}}$ input will control the clock input to the timer/counter. A low on the $\overline{\text{T1G}}$ input will cause Timer1 to increment at the clock rate, a high will hold the timer at its present value.

The T1OSCEN bit (T1CON<3>) enables the LP oscillator as a clock source for Timer1. This mode is a replacement for the regular external oscillator.

T1CKPS<1:0> determines the prescaler value for the timer. Available prescaler values are:

T1CKPS<1:0>		Prescaler Value
Bit 1	Bit 0	
1	1	1:8
1	0	1:4
0	1	1:2
0	0	1:1

Note: To use the LP oscillator as the Timer1 oscillator:
1. TMR1CS must be set.
2. T1OSCEN must be set.
3. The Configuration Word must select INTRC w/o CLKOUT.

NOTES:

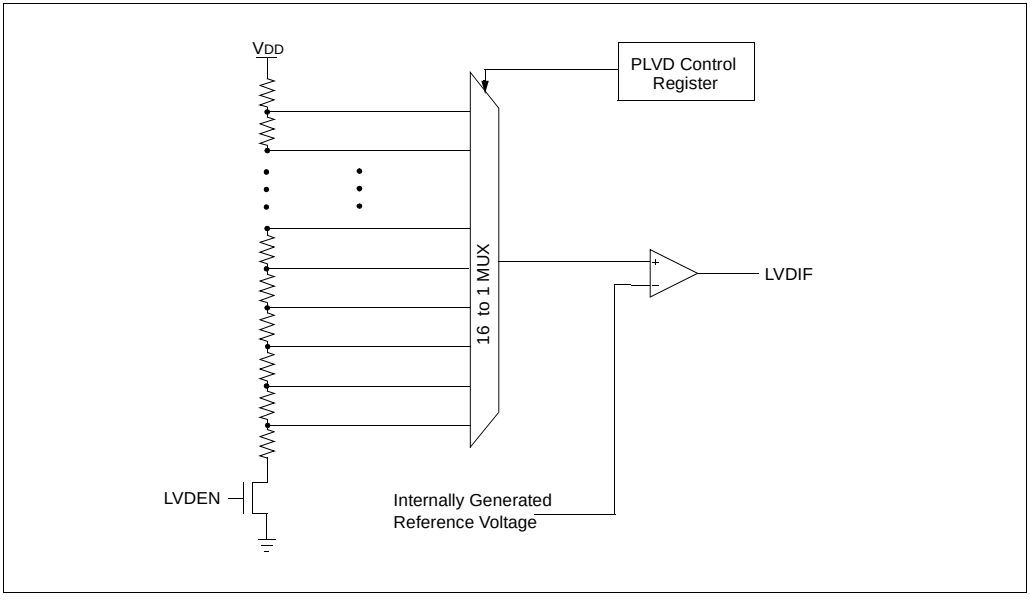
8.2 Operation

The PLVD indicates a low voltage condition by setting the LVDIF bit in the PIR1 register. Once set by the PLVD module, the LVDIF bit will remain set until cleared by software. For proper indication of a low voltage condition, the user should clear this bit prior to testing.

To test for a low voltage condition, the PLVD module compares the divided output of VDD against an internal bandgap reference. The PLVD module automatically enables this reference whenever it is enabled and provides a stability bit, BGST, to indicate when it has stabilized. The bandgap reference is also enabled by other modules within the PIC16C781/782 as part of their operation. Other modules using the bandgap include the following:

- VR module
- BOR module
- OPA calibration module

FIGURE 8-2: LOW VOLTAGE DETECT BLOCK DIAGRAM



10.3 DAC Configuration

Example 10-1 shows a sample configuration for the DAC module. The port pin is configured, AVDD is selected for the voltage reference, and the DAC output is enabled.

EXAMPLE 10-1: DAC CONFIGURATION

```
;*  This code block will configure the DAC
;*  for AVDD Voltage Ref, and RB1/AN5/VDAC as
;*  output.

    BANKSEL TRISB          ; Select bank 1
    BSF     TRISB,1        ; Set RB1 input
    BSF     ANSEL,1        ; Set RB1 as analog

    BANKSEL DACON0         ; Select Bank 2
    CLRF    DAC            ; DAC to 00
    MOVLW   B'11000000'    ; Enable DAC output
    MOVWF   DACON0         ; Set REF = VDD

    MOVLW   DAC_VALUE
    MOVWF   DAC            ; Set DAC output
```

10.4 Effects of RESET

A device RESET forces all registers to their RESET state. This forces the following conditions:

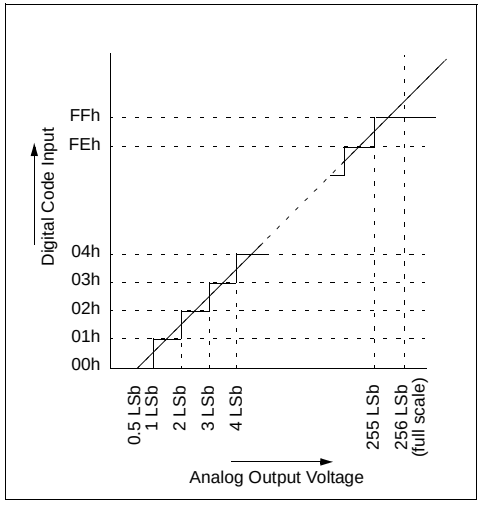
- DAC module is off
- Reference input to AVDD
- Output disabled
- DAC register is cleared

10.5 DAC Module Accuracy/Error

The accuracy/error specified for the DAC includes:

- Integral non-linearity error
- Differential non-linearity error
- Gain error
- Offset error
- Monotonicity

FIGURE 10-2: DAC TRANSFER FUNCTION



Offset error measures the first actual transition of a code versus the first ideal transition of a code. Offset error shifts the entire transfer function. Offset error can be calibrated out of a system or introduced into a system through the interaction of the output drive capability with the load impedance.

Gain error measures the maximum deviation of the last actual transition and the last ideal transition adjusted for offset error. This error appears as a change in slope of the transfer function. The difference in gain error to full scale error is that full scale does not take offset error into account. Gain error can be calibrated out by adjusting the reference voltage.

Linearity error refers to the uniformity of the voltage change with code change. Linearity errors cannot be calibrated out of the system. **Integral non-linearity error** measures the actual voltage output versus the ideal voltage output adjusted by the gain error for each code.

Differential non-linearity error measures the maximum actual voltage step versus the ideal voltage step. This measure is unadjusted.

TABLE 10-1: REGISTERS/BITS ASSOCIATED WITH DAC

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on All Other RESETS
11Fh	DACON0	DAON	DAOE	—	—	—	—	DARS1	DARS0	00-- --00	00-- --00
11Eh	DAC	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0	0000 0000	0000 0000
86h	TRISB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	1111 1111	1111 1111
9Dh	ANSEL	AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0	1111 1111	1111 1111

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used for DAC conversion.

11.2 Configuration as OPAMP or Comparator

The following example demonstrates calibration of the OPA module as an Operational Amplifier.

EXAMPLE 11-1: CALIBRATION FOR OPAMP MODE

```
;*  This code block will configure the OPA
;*  module as an Op Amp, 2 MHz GBWP, and
;*  calibrated for a common mode voltage of
;*  1.2V. Routine returns w=0 if
;*  calibration good.

    BANKSEL     OPACON       ; Select Bank 2
    MOVLW       B'10000001'  ; Op Amp mode &
    MOVWF       OPACON       ; 2 MHz GBWP

    BCF         CALCON,CALREF; Set 1.2V
    BSF         CALCON,CAL   ; Start

CAL_LOOP
    BTFSC       CALCON,CAL   ; Test for end
    GOTO        CAL_LOOP     ; If not, wait
    MOVLW       ERROR_FLAG
    BTFSS       CALCON,CALERR; Test for error
    CLRW                     ; If no, return 0
    RETURN
```

The following example demonstrates how to configure and calibrate the OPA module as a Voltage Comparator.

EXAMPLE 11-2: CALIBRATION FOR COMPARATOR MODE

```
;*  This code block will configure the OPA
;*  module as a voltage comparator, slow
;*  speed, and calibrated for a common mode
;*  voltage of 2.5 V (assumes VDD=5V).
;*  Routine returns w=0 if calibration good.

    BANKSEL     OPACON       ; Select Bank 2
    MOVLW       B'10000000'
    MOVWF       OPACON       ; Op Amp mode,
                             ; slow
    BSF         CALCON,CALREF; Common mode=DAC

    MOVLW       H'0x80'
    MOVWF       DAC          ; DAC at VDD/2
    MOVLW       B'10000000'
    MOVWF       DACON0       ; enable DAC,
                             ; VDD ref
    BSF         CALCON,CAL   ; Start
CAL_LOOP
    BTFSC       CALCON,CAL   ; Test for end
    GOTO        CAL_LOOP     ; If not, wait

    MOVLW       ERROR_FLAG
    BTFSS       CALCON,CALERR; Test for error
    CLRW                     ; If no, return 0
    BSF         OPACON,CMPEN ; Comparator mode
    RETURN
```

11.3 Effects of RESET

A device RESET forces all registers to their RESET state. This disables the OPA module and clears any calibration.

11.4 OPA Module Performance

Common AC and DC performance specifications for the OPA module:

- Common Mode Voltage Range
- Leakage Current
- Input Offset Voltage
- Open Loop Gain
- Gain Bandwidth Product

Common mode voltage range is the specified voltage range for the OPA+ and OPA- inputs, for which the OPA module will perform to within its specifications. The OPA module is designed to operate with input voltages between 0 and V_{DD}-1.4V. Behavior for Common mode voltages greater than V_{DD}-1.4V, or below 0V, are not guaranteed.

Leakage current is a measure of the small source or sink currents on the OPA+ and OPA- inputs. To minimize the effect of leakage currents, the effective impedances connected to the OPA+ and OPA- inputs should be kept as small as possible and equal.

Input offset voltage is a measure of the voltage difference between the OPA+ and OPA- inputs in a closed loop circuit with the OPA in its linear region. The offset voltage will appear as a DC offset in the output equal to the input offset voltage, multiplied by the gain of the circuit. The input offset voltage is also affected by the Common mode voltage. The OPA has an automatic calibration module which can minimize the input offset voltage of the module.

Open loop gain is the ratio of the output voltage to the differential input voltage, (OPA+) - (OPA-). The gain is greatest at DC and falls off with frequency.

Gain Bandwidth Product or GBWP is the frequency at which the open loop gain falls off to 0 dB. The lower GBWP is optimized for systems requiring low frequency response and low power consumption.

12.3 Effects of RESET

A RESET forces all registers to their RESET state. This disables both comparators.

TABLE 12-2: REGISTERS ASSOCIATED WITH THE COMPARATOR MODULE

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other RESETS
119h	CM1CON0	C1ON	C1OUT	C1OE	C1POL	C1SP	C1R	C1CH1	C1CH0	0000 0000	0000 0000
11Ah	CM2CON0	C2ON	C2OUT	C2OE	C2POL	C2SP	C2R	C2CH1	C2CH0	0000 0000	0000 0000
11Bh	CM2CON1	MC1OUT	MC2OUT	—	—	—	—	—	C2SYNC	00-- ---0	00-- ---0
85h	TRISA	PORTA Data Direction Register								1111 1111	1111 1111
86h	TRISB	PORTB Data Direction Register								1111 1111	1111 1111
05h	PORTA	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	xxxx 0000	uuuu 0000
06h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx 0000	uuuu 0000
9Dh	ANSEL	AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0	1111 1111	1111 1111
0Ch	PIR1	LVDIF	ADIF	C2IF	C1IF	—	—	—	TMR1ON	0000 ---0	0000 ---0
8Ch	PIE1	LVDIE	ADIE	C2IE	C1IE	—	—	—	TMR1IE	0000 ---0	0000 ---0

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used for comparator.

REGISTER 14-1: CONFIGURATION WORD FOR PIC16C781/782 DEVICE (CONFIG:2007h)

$\overline{CP}$	$\overline{CP}$	BORV1	BORV0	$\overline{CP}$	$\overline{CP}$	—	BODEN	MCLRE	$\overline{PWRTE}$	WDTE	F0SC2	F0SC1	F0SC0
bit13													bit0

bit 13-12, 9-8 **CP:** Program Memory Code Protection bits
1 = Code Protection off
0 = All program memory is protected(1)

bit 11-10 **BORV<1:0>:** Brown-out Reset Voltage bits
00 = PBOR set to 4.5V
01 = PBOR set to 4.2V
10 = PBOR set to 2.7V
11 = PBOR set to 2.5V

bit 7 **Unimplemented:** Read as '1'

bit 6 **BODEN**: Brown-out Detect Reset Enable bit(1)
1 = Brown-out Detect Reset enabled
0 = Brown-out Detect Reset disabled

bit 5 **MCLRE:** RA5/$\overline{MCLR}$ Pin Function Select bit
1 = RA5/$\overline{MCLR}$ pin function is $\overline{MCLR}$
0 = RA5/$\overline{MCLR}$ pin function is digital input, $\overline{MCLR}$ internally tied to V_{DD}

bit 4 **$\overline{PWRTE}$**: Power-up Timer Enable bit(1)
1 = PWRT disabled
0 = PWRT enabled

bit 3 **WDTE**: Watchdog Timer Enable bit
1 = WDT enabled
0 = WDT disabled

bit 2-0 **FOSC<2:0>**: Oscillator Selection bits

FOSC<2:0>	OSCILLATOR	RA6/OSC2/CLKOUT/T1CKI	RA7/OSC1/CLKIN
000	LP	Crystal/Resonator	Crystal/Resonator
001	XT	Crystal/Resonator	Crystal/Resonator
010	HS	Crystal/Resonator	Crystal/Resonator
011	EC	Digital I/O	CLKIN
100	INTRC	Digital I/O	Digital I/O
101	INTRC	CLKOUT	Digital I/O
110	RC	Digital I/O	RC
111	RC	CLKOUT	RC

Note 1: All of the CP bits must be given the same value to enable code protection.

TABLE 14-5: RESET CONDITION FOR SPECIAL REGISTERS

Condition	Program Counter	STATUS Register	PCON Register
Power-on Reset	000h	0001 1xxx	---0 1-01
$\overline{MCLR}$ Reset during normal operation	000h	000u uuuu	---0 1-uu
$\overline{MCLR}$ Reset during SLEEP	000h	0001 0uuu	---0 1-uu
WDT Reset	000h	0000 1uuu	---0 1-uu
WDT Wake-up	PC + 1	uuu0 0uuu	---0 u-uu
Brown-out Reset	000h	0001 1uuu	---0 1-u0
Interrupt wake-up from SLEEP, GIE = 0	PC + 1	uuu1 0uuu	---u u-uu
Interrupt wake-up from SLEEP, GIE = 1	0004h	uuu1 0uuu	---u u-uu

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as '0'.

FIGURE 14-6: TIME-OUT SEQUENCE ON POWER-UP ($\overline{MCLR}$ TIED TO VDD)

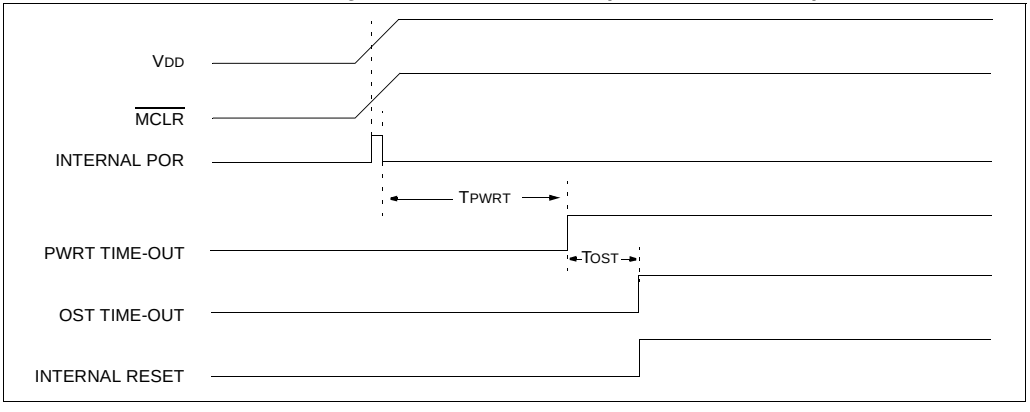


FIGURE 14-7: TIME-OUT SEQUENCE ON POWER-UP ($\overline{MCLR}$ NOT TIED TO VDD)

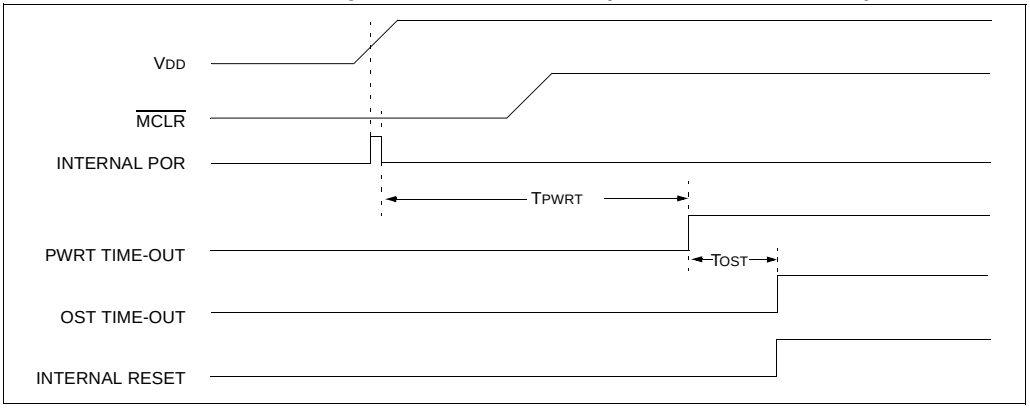
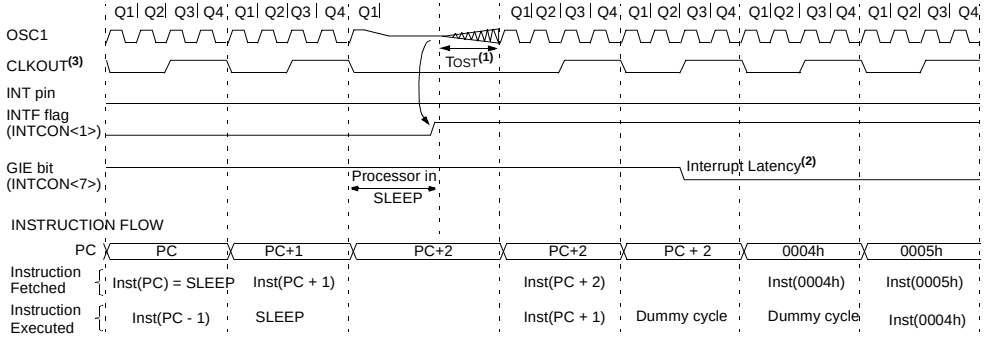


FIGURE 14-12: WAKE-UP FROM SLEEP THROUGH INTERRUPT



Note 1: TOST = 1024TOSC (drawing not to scale). This delay applies to LP, XT and HS modes only.
2: GIE = '1' assumed. In this case after wake- up, the processor jumps to the interrupt routine. If GIE = '0', execution will continue in-line.
3: CLKOUT is not available in these osc modes, but shown here for timing reference.

TABLE 15-2: PIC16CXXX INSTRUCTION SET

Mnemonic, Operands		Description	Cycles	14-Bit Opcode MSb LSb	Status Affected	Notes
BYTE-ORIENTED FILE REGISTER OPERATIONS						
ADDWF	f, d	Add W and f	1	00 0111 dfff ffff	C,DC,Z	1,2
ANDWF	f, d	AND W with f	1	00 0101 dfff ffff	Z	1,2
CLRF	f	Clear f	1	00 0001 lfff ffff	Z	2
CLRW	-	Clear W	1	00 0001 0000 0011	Z	
COMF	f, d	Complement f	1	00 1001 dfff ffff	Z	1,2
DECF	f, d	Decrement f	1	00 0011 dfff ffff	Z	1,2
DECFSZ	f, d	Decrement f, Skip if 0	1(2)	00 1011 dfff ffff		1,2,3
INCF	f, d	Increment f	1	00 1010 dfff ffff	Z	1,2
INCFSZ	f, d	Increment f, Skip if 0	1(2)	00 1111 dfff ffff		1,2,3
IORWF	f, d	Inclusive OR W with f	1	00 0100 dfff ffff	Z	1,2
MOVF	f, d	Move f	1	00 1000 dfff ffff	Z	1,2
MOVWF	f	Move W to f	1	00 0000 lfff ffff		
NOP	-	No Operation	1	00 0000 0xx0 0000		
RLF	f, d	Rotate Left f through Carry	1	00 1101 dfff ffff	C	1,2
RRF	f, d	Rotate Right f through Carry	1	00 1100 dfff ffff	C	1,2
SUBWF	f, d	Subtract W from f	1	00 0010 dfff ffff	C,DC,Z	1,2
SWAPF	f, d	Swap nibbles in f	1	00 1110 dfff ffff		1,2
XORWF	f, d	Exclusive OR W with f	1	00 0110 dfff ffff	Z	1,2
BIT-ORIENTED FILE REGISTER OPERATIONS						
BCF	f, b	Bit Clear f	1	01 00bb bfff ffff		1,2
BSF	f, b	Bit Set f	1	01 01bb bfff ffff		1,2
BTFSC	f, b	Bit Test f, Skip if Clear	1 (2)	01 10bb bfff ffff		3
BTFSS	f, b	Bit Test f, Skip if Set	1 (2)	01 11bb bfff ffff		3
LITERAL AND CONTROL OPERATIONS						
ADDLW	k	Add literal and W	1	11 111x kkkk kkkk	C,DC,Z	
ANDLW	k	AND literal with W	1	11 1001 kkkk kkkk	Z	
CALL	k	Call subroutine	2	10 0kkk kkkk kkkk		
CLRWDT	-	Clear Watchdog Timer	1	00 0000 0110 0100	$\overline{TO}$,$\overline{PD}$	
GOTO	k	Go to address	2	10 1kkk kkkk kkkk		
IORLW	k	Inclusive OR literal with W	1	11 1000 kkkk kkkk	Z	
MOVLW	k	Move literal to W	1	11 00xx kkkk kkkk		
RETFIE	-	Return from interrupt	2	00 0000 0000 1001		
RETLW	k	Return with literal in W	2	11 01xx kkkk kkkk		
RETURN	-	Return from Subroutine	2	00 0000 0000 1000		
SLEEP	-	Go into standby mode	1	00 0000 0110 0011	$\overline{TO}$,$\overline{PD}$	
SUBLW	k	Subtract W from literal	1	11 110x kkkk kkkk	C,DC,Z	
XORLW	k	Exclusive OR literal with W	1	11 1010 kkkk kkkk	Z	

Note 1: When an I/O register is modified as a function of itself (e.g., `MOVF PORTB, 1`), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.

2: If this instruction is executed on the TMR0 register (and, where applicable, d = 1), the prescaler will be cleared if assigned to the Timer0 Module.

3: If the Program Counter (PC) is modified or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a `NOP`.

16.4 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK object linker combines relocatable objects created by the MPASM assembler and the MPLAB C17 and MPLAB C18 C compilers. It can also link relocatable objects from pre-compiled libraries, using directives from a linker script.

The MPLIB object librarian is a librarian for pre-compiled code to be used with the MPLINK object linker. When a routine from a library is called from another source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications. The MPLIB object librarian manages the creation and modification of library files.

The MPLINK object linker features include:

- Integration with MPASM assembler and MPLAB C17 and MPLAB C18 C compilers.
- Allows all memory areas to be defined as sections to provide link-time flexibility.

The MPLIB object librarian features include:

- Easier linking because single libraries can be included instead of many smaller files.
- Helps keep code maintainable by grouping related modules together.
- Allows libraries to be created and modules to be added, listed, replaced, deleted or extracted.

16.5 MPLAB SIM Software Simulator

The MPLAB SIM software simulator allows code development in a PC-hosted environment by simulating the PIC series microcontrollers on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a file, or user-defined key press, to any of the pins. The execution can be performed in single step, execute until break, or trace mode.

The MPLAB SIM simulator fully supports symbolic debugging using the MPLAB C17 and the MPLAB C18 C compilers and the MPASM assembler. The software simulator offers the flexibility to develop and debug code outside of the laboratory environment, making it an excellent multi-project software development tool.

16.6 MPLAB ICE High Performance Universal In-Circuit Emulator with MPLAB IDE

The MPLAB ICE universal in-circuit emulator is intended to provide the product development engineer with a complete microcontroller design tool set for PIC microcontrollers (MCUs). Software control of the MPLAB ICE in-circuit emulator is provided by the MPLAB Integrated Development Environment (IDE), which allows editing, building, downloading and source debugging from a single environment.

The MPLAB ICE 2000 is a full-featured emulator system with enhanced trace, trigger and data monitoring features. Interchangeable processor modules allow the system to be easily reconfigured for emulation of different processors. The universal architecture of the MPLAB ICE in-circuit emulator allows expansion to support new PIC microcontrollers.

The MPLAB ICE in-circuit emulator system has been designed as a real-time emulation system, with advanced features that are generally found on more expensive development tools. The PC platform and Microsoft® Windows environment were chosen to best make these features available to you, the end user.

16.7 ICEPIC In-Circuit Emulator

The ICEPIC low cost, in-circuit emulator is a solution for the Microchip Technology PIC16C5X, PIC16C6X, PIC16C7X and PIC16CXXX families of 8-bit One-Time-Programmable (OTP) microcontrollers. The modular system can support different subsets of PIC16C5X or PIC16CXXX products through the use of interchangeable personality modules, or daughter boards. The emulator is capable of emulating without target application circuitry being present.

TABLE 16-1: DEVELOPMENT TOOLS FROM MICROCHIP

		PIC12CXXX	PIC14000	PIC16C5X	PIC16C6X	PIC16CXXX	PIC16F62X	PIC16C7X	PIC16C7XX	PIC16C8X	PIC16F8XX	PIC16C9XX	PIC17C4X	PIC17C7XX	PIC18CXX2	PIC18FXXX	24CXX/ 25CXX/ 93CXX	HCSXXX	MCRFXXX	MCP2510
Software Tools	MPLAB® Integrated Development Environment	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓				
	MPLAB® C17 C Compiler												✓	✓						
	MPLAB® C18 C Compiler														✓	✓				
	MPASM™ Assembler/ MPLINK™ Object Linker	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		
Emulators	MPLAB® ICE In-Circuit Emulator	✓	✓	✓	✓	✓	✓**	✓	✓	✓	✓	✓	✓	✓	✓	✓				
	ICEPIC™ In-Circuit Emulator	✓		✓	✓	✓		✓	✓	✓		✓								
Debugger	MPLAB® ICD In-Circuit Debugger				✓*			✓*			✓					✓				
Programmers	PICSTART® Plus Entry Level Development Programmer	✓	✓	✓	✓	✓	✓**	✓	✓	✓	✓	✓	✓	✓	✓	✓				
	PRO MATE® II Universal Device Programmer	✓	✓	✓	✓	✓	✓**	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		
Demo Boards and Eval Kits	PICDEM™ 1 Demonstration Board			✓		✓		✓†		✓			✓							
	PICDEM™ 2 Demonstration Board				✓†			✓†							✓	✓				
	PICDEM™ 3 Demonstration Board											✓								
	PICDEM™ 14A Demonstration Board		✓																	
	PICDEM™ 17 Demonstration Board													✓						
	KEELOQ® Evaluation Kit																	✓		
	KEELOQ® Transponder Kit																	✓		
	microID™ Programmer's Kit																		✓	
	125 kHz microID™ Developer's Kit																		✓	
	125 kHz Anticollision microID™ Developer's Kit																		✓	
	13.56 MHz Anticollision microID™ Developer's Kit																		✓	
	MCP2510 CAN Developer's Kit																			✓

* Contact the Microchip Technology Inc. web site at www.microchip.com for information on how to use the MPLAB® ICD In-Circuit Debugger (DV164001) with PIC16C62, 63, 64, 65, 72, 73, 74, 76, 77.

** Contact Microchip Technology Inc. for availability date.

† Development tool is available on select devices.

17.1 DC Characteristics: Power Supply

TABLE 17-1: DC CHARACTERISTICS: PIC16C781/782, DSTEMP (INDUSTRIAL)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature-40°C ≤ TA ≤ +85°C for industrial				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
D001	VDD	**Supply Voltage**	4.0 4.5	— —	5.5 5.5	V —	XT, EC, RC, INTRC Oscillator HS Oscillator
D001A	VDD	**Supply Voltage** (DSTEMP)	2.7 4.5	— —	5.5 5.5	V V	XT, EC, RC, INTRC Oscillator HS Oscillator
D002*	VDR	**RAM Data Retention Voltage(1)**	—	1.5	—	V	
D003	VPOR	**VDD Start Voltage** to ensure internal Power-on Reset signal	—	TBD	—	V	See section on Power-on Reset for details
D004*	SVDD	**VDD Rise Rate** to ensure internal Power-on Reset signal	0.05	—	—	V/ms	See section on Power-on Reset for details. PWRT enabled
D010	IDD	**Supply Current(2)**	— — — —	TBD TBD TBD TBD	TBD TBD TBD TBD	mA mA mA mA	FOSC = 20 MHz, VDD = 5.5V* HS Oscillator FOSC = 20 MHz, VDD = 4.5V HS Oscillator FOSC = 4 MHz, VDD = 4.0V* XT, RC w/CLKOUT FOSC = 32 kHz, VDD = 4.0V LP Oscillator
D020 D020A	IPD	**Power-down Current(3)**	— —	TBD 1.5	TBD 19	µA µA	VDD = 5.5V VDD = 4.0V
	IOPA	**Operational Amplifier**	—	TBD TBD	TBD TBD	mA mA	VDD = 5.0V, GBWP = 0 VDD = 5.0V, GBWP = 1
	IVC*	**Voltage Comparators C1 and C2**	— —	TBD TBD	TBD TBD	mA mA	VDD = 5.0V, VID>100 mV C1SP = 0 VDD = 5.0 , VID>100 mV C1SP = 1
	IADC*	**Digital to Analog Converter (DAC)**	—	TBD	TBD	mA	VDD = 5.0V
D021	IWDT*	**Watchdog Timer**	—	TBD	TBD	mA	VDD = 4.0V
D026	IAD*	**Analog-to-Digital Converter (ADC)**	—	TBD	TBD	mA	VDD = 5.5V, ADC not converting
	IPLVD*	**Programmable Low Voltage Detect**		TBD	TBD	mA	VDD = 4.0V
	IPBOR*	**Programmable Brown-out Reset**		TBD	TBD	mA	VDD = 5.0V
1A	FOSC	**LP Oscillator, Operating Freq.** **INTRC Oscillator Operating Freq.** **XT Oscillator Operating Freq.** **HS Oscillator Operating Freq.**	9 — — 0 0	— 4 37 — —	200 — — 4 20	kHz MHz kHz MHz MHz	All temperatures All temperatures, OSCF = 1 All temperatures, OSCF = 0 All temperatures All temperatures

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail-to-rail; all I/O pins configured as inputs, pulled to VDD
$\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins configured as iputs and tied to VDD or VSS.

FIGURE 17-5: EXTERNAL CLOCK TIMING

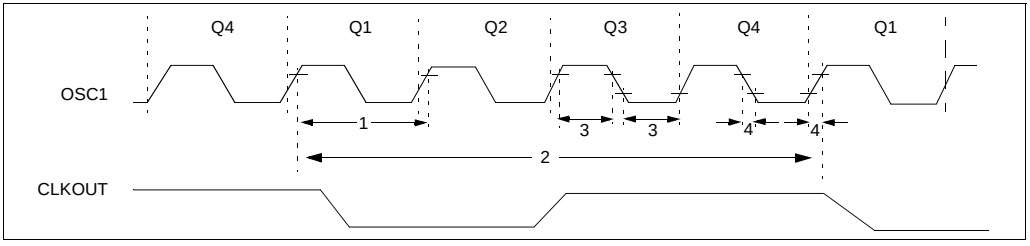


TABLE 17-4: EXTERNAL CLOCK TIMING REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
1A	FOSC	External CLKIN Frequency(1)	DC	—	4	MHz	XT osc mode
			DC	—	20	MHz	EC osc mode
			DC	—	20	MHz	HS osc mode
			DC	—	200	kHz	LP osc mode
		Oscillator Frequency(1)	0.1	—	4	MHz	XT osc mode
			4	—	20	MHz	HS osc mode
			5	—	200	kHz	LP osc mode
1	TOSC	External CLKIN Period(1)	250	—	—	ns	XT and RC osc mode
			50	—	—	ns	EC osc mode
			50	—	—	ns	HS osc mode
			5	—	—	µs	LP osc mode
		Oscillator Period(1)	250	—	10,000	ns	XT osc mode
			50	—	250	ns	HS osc mode
			5	—	—	µs	LP osc mode
2	TCY	Instruction Cycle Time(1)	200	TCY	DC	ns	TCY = 4/FOSC
3*	TOSL, TOSH	External Clock in (OSC1) High or Low Time	100	—	—	ns	XT oscillator
			2.5	—	—	µs	LP oscillator
			15	—	—	ns	HS oscillator
							EC oscillator
4*	TOSR, TOSF	External Clock in (OSC1) Rise or Fall Time	—	—	25	ns	XT oscillator
			—	—	50	ns	LP oscillator
			—	—	15	ns	HS oscillator
							EC oscillator

* These parameters are characterized but not tested.

† Data in “Typ” column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

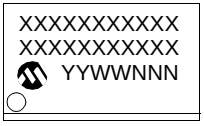
Note 1: Instruction cycle period (TCY) equals four times the input oscillator time-base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1/CLKIN pin.
When an external clock input is used, the "Max." cycle time limit is "DC" (no clock) for all devices.

NOTES:

19.0 PACKAGING INFORMATION

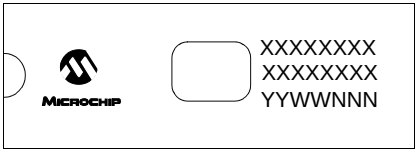
19.1 Package Marking Information

20-Lead SSOP

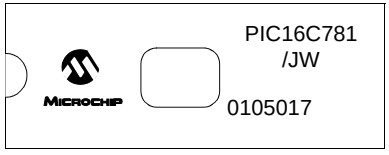


Example

20-Lead CERDIP Windowed

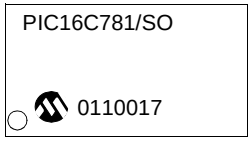


Example

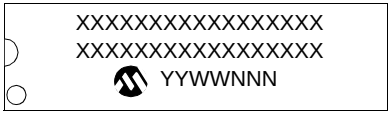


20-Lead SOIC

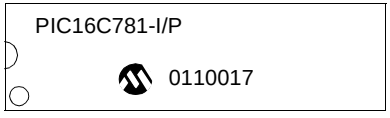
Example



20-Lead PDIP



Example



Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.