Microchip Technology - PIC16LC782T-I/SS Datasheet

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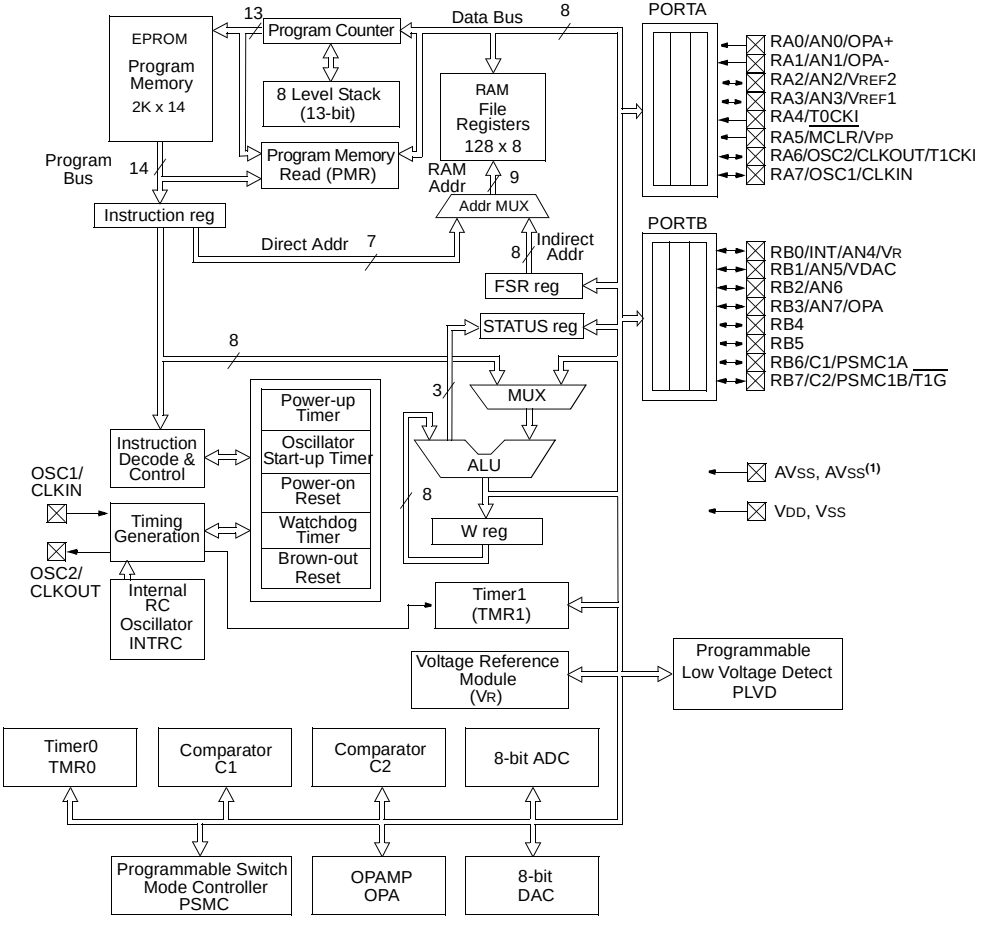
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	13
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 8x8b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	20-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lc782t-i-ss

FIGURE 1-2: PIC16C782 BLOCK DIAGRAM



Note 1: AVDD and AVSS pins are used for the following modules: C1, C2, OPA, DAC, ADC, and VR.

TABLE 1-1: PIC16C781/782 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RB7/C2/PSMC1B/$\overline{T1G}$	RB7	TTL	CMOS	Bi-directional I/O
	C2	—	CMOS	Comparator 2 Output
	PSMC1B	—	CMOS	PSMC Output 1B
	$\overline{T1G}$	ST	—	Timer 1 Gate Input
AVDD	AVDD	Power	—	Positive Supply for Analog
AVSS	AVSS	Power	—	Ground Reference for Analog
VDD	VDD	Power	—	Positive Supply for Logic and I/O pins
VSS	VSS	Power	—	Ground Reference for Logic and I/O pins

Legend: ST = Schmitt Trigger AN = Analog OD = open drain TTL = Logic Level
XTAL = Crystal CMOS = CMOS Output Power = Power Supply

NOTES:

2.8 PCON Register

The Power Control (PCON) register contains two flag bits to allow determination of the source of the most recent RESET:

- Power-on Reset ($\overline{POR}$)
- External $\overline{MCLR}$ Reset
- Power Supply Brown-out ($\overline{BOR}$) Reset

The Power Control register also contains frequency select bits for the INTRC oscillator and the WDT software enable bit.

Note: $\overline{BOR}$ is unknown on Power-on Reset. It must then be set by the user and checked on subsequent RESETS to see if $\overline{BOR}$ is clear, indicating a brown-out has occurred. The $\overline{BOR}$ status bit is a don't care and is not necessarily predictable if the brown-out circuit is disabled (by clearing the BODEN bit in the Configuration word).

Direction of Change	Typical Time Inactive	
	Minimum	Maximum
4 MHz → 37 kHz	100 μs	300 μs
37 kHz→4 MHz	1.25 μs	3.25 μs

Note: When changing the internal oscillator speed (i.e., the OSCF bit, INTRC mode), the processor will be inactive during the oscillator frequency change.

REGISTER 2-6: POWER CONTROL REGISTER (PCON: 8Eh)

U-0	U-0	U-0	R/W-q	R/W-1	U-0	R/W-q	R/W-q
—	—	—	WDTON	OSCF	—	$\overline{POR}$	$\overline{BOR}$
bit 7							bit 0

bit 7-5 **Unimplemented:** Read as '0'

bit 4 **WDTON:** WDT Software Enable bit

If WDTE bit (Configuration Word <3>) = 1:
This bit is not writable, always reads '1'

If WDTE bit (Configuration Word <3>) = 0:
1 = WDT is enabled
0 = WDT is disabled

bit 3 **OSCF:** Oscillator Speed INTRC Mode bit

1 = 4 MHz typical
0 = 37 kHz typical
All other oscillator modes (X = Ignored)

bit 2 **Unimplemented:** Read as '0'

bit 1 **$\overline{POR}$:** Power-on Reset Status bit

1 = No Power-on Reset occurred
0 = A Power-on Reset occurred (must be set in software after a Power-on Reset occurs)

bit 0 **$\overline{BOR}$:** Brown-out Reset Status bit

1 = No Brown-out Reset occurred
0 = A Brown-out Reset occurred

Legend:			
q = Value depends on conditions			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

REGISTER 3-2: WEAK PULL-UP PORTB REGISTER (WPUB: 95h)

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
WPUB7	WPUB6	WPUB5	WPUB4	WPUB3	WPUB2	WPUB1	WPUB0
bit7							bit0

bit 7-0 **WPUB<7:0>:** PORTB Weak Pull-Up Control bits

1 = Weak pull-up enabled for corresponding pin

0 = Weak pull-up disabled for corresponding pin

Note 1: For the WPUB register setting to take effect, the $\overline{\text{RBPU}}$ bit in the OPTION_REG register must be cleared.

2: The weak pull-up device is automatically disabled if the pin is in output mode, i.e., (TRISB = 0) for corresponding pin.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

REGISTER 3-3: INTERRUPT-ON-CHANGE PORTB REGISTER (IOCB: 96h)

R/W-1	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0
IOCB7	IOCB6	IOCB5	IOCB4	IOCB3	IOCB2	IOCB1	IOCB0
bit7							bit0

bit 7-0 **IOCB<7:0>:** Interrupt-on-Change PORTB Control bits

1 = Interrupt-on-change enabled for corresponding pin

0 = Interrupt-on-change disabled for corresponding pin

Note 1: The interrupt enable bits, GIE and RBIE in the INTCON register, must be set for individual interrupts to be recognized.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

3.3.3 TRISB, ANSEL, AND CONTROL PRECEDENCE

The ANSEL and TRISB registers are the primary controls for the configuration of PORTB pins. TRISB tri-states the output drivers of PORTB, and the ANSEL register disables the input buffers. It is important to program both registers when configuring a port pin, since most peripherals do not have precedence over the TRISB and ANSEL registers' control of the pin. Even if a peripheral has the ability to override the control of the TRISB and ANSEL registers, it is good practice to program both registers appropriately.

Note 1: Upon RESET, the ANSEL register configures the RB<3:0> pins as analog inputs.

2: When programmed as analog inputs, RB<3:0> pins will read as '0'.

3: There are specific cases in which the functions of the TRISB and ANSEL registers can be overridden by a peripheral or configuration word (see Figure 3-9 through Figure 3-16 for details).

4.4 Program Memory Read With Code Protect Set

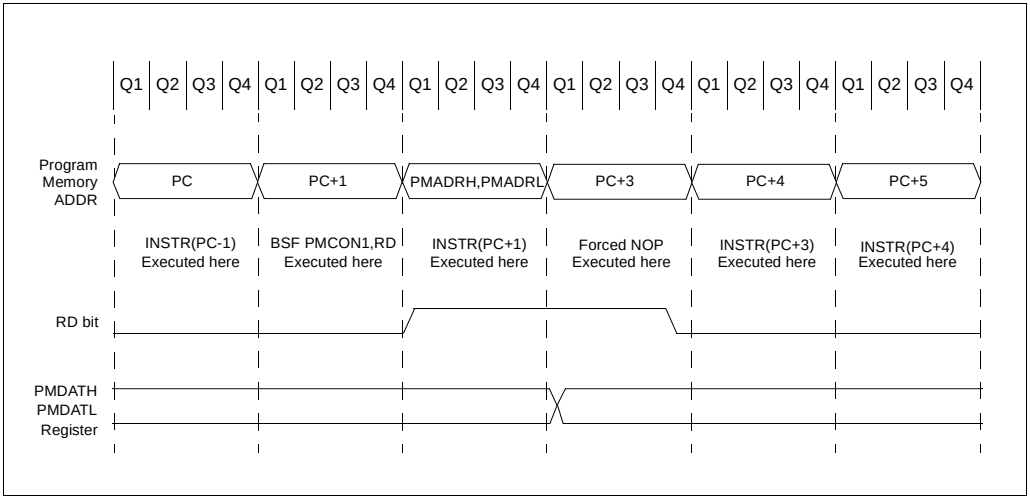
When the device is code protected, the CPU can still perform the program memory read function.

TABLE 4-1: SUMMARY OF REGISTERS ASSOCIATED WITH PMR

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other RESETS
10Ch	PMDATL	PMD7	PMD6	PMD5	PMD4	PMD3	PMD2	PMD1	PMD0	0000 0000	0000 0000
10Dh	PMADRL	PMA7	PMA6	PMA5	PMA4	PMA3	PMA2	PMA1	PMA0	xxxx xxxx	uuuu uuuu
10Eh	PMDATH	—	—	PMD13	PMD12	PMD11	PMD10	PMD9	PMD8	--00 0000	--00 0000
10Fh	PMADRH	—	—	—	Reserved	Reserved	PMA10	PMA9	PMA8	---x xxxx	---u uuuu
18Ch	PMCON1	Reserved	—	—	—	—	—	—	RD	1--- ---0	1--- ---0

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by PMR.

FIGURE 4-1: PROGRAM MEMORY READ CYCLE EXECUTION



8.2 Operation

The PLVD indicates a low voltage condition by setting the LVDIF bit in the PIR1 register. Once set by the PLVD module, the LVDIF bit will remain set until cleared by software. For proper indication of a low voltage condition, the user should clear this bit prior to testing.

To test for a low voltage condition, the PLVD module compares the divided output of VDD against an internal bandgap reference. The PLVD module automatically enables this reference whenever it is enabled and provides a stability bit, BGST, to indicate when it has stabilized. The bandgap reference is also enabled by other modules within the PIC16C781/782 as part of their operation. Other modules using the bandgap include the following:

- VR module
- BOR module
- OPA calibration module

FIGURE 8-2: LOW VOLTAGE DETECT BLOCK DIAGRAM

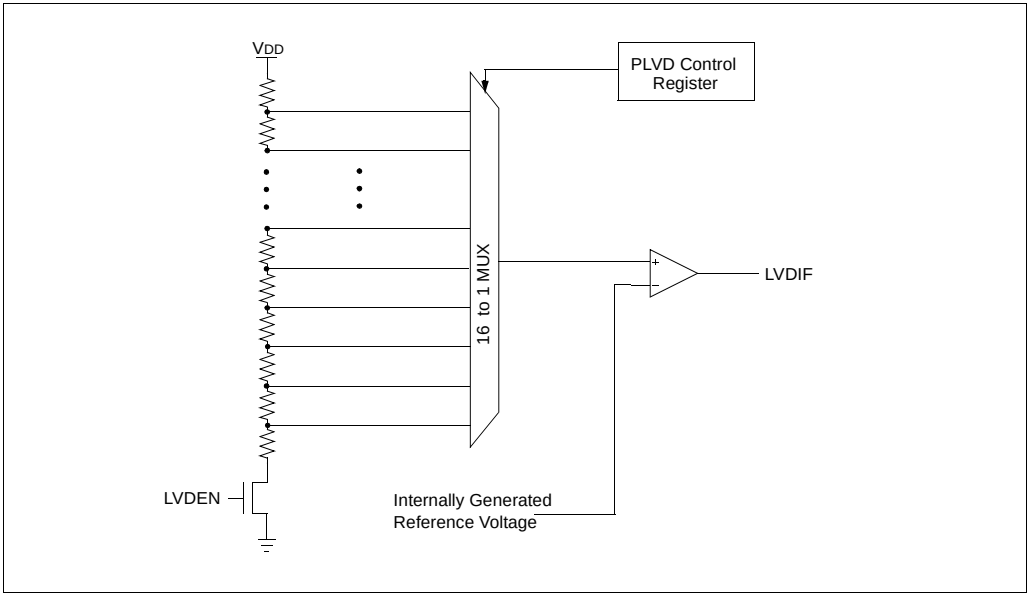
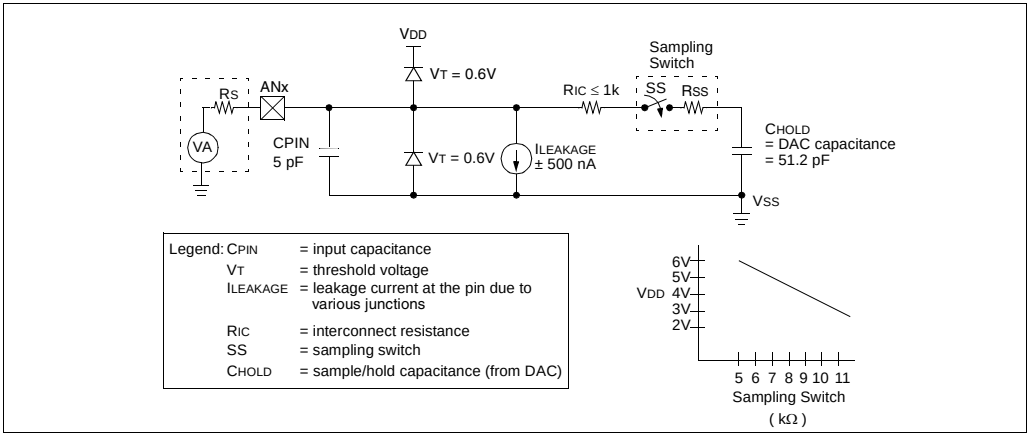


FIGURE 9-2: ANALOG INPUT MODEL



9.4 ADC Configuration and Conversion

Example 9-2 demonstrates an ADC conversion. The RA0/AN0 pin is configured as the analog input. The reference voltage selected is the device AVDD. The ADC interrupt is enabled, and the ADC conversion clock is ADRC.

Clearing the GO/$\overline{\text{DONE}}$ bit during a conversion aborts the current conversion. The ADRES register is NOT updated with the partially completed ADC conversion sample. That is, the ADRES register continues to contain the value of the last completed conversion (or the last value written to the ADRES register). After the ADC conversion is aborted, a 2TAD wait period is required before the next acquisition is started. After this 2TAD wait period, an acquisition is automatically started on the selected channel.

EXAMPLE 9-2: ADC CONVERSION

```
;*****************************************
;*  This code block will configure the ADC
;*  for polling, AVDD as reference, RC clock
;*  and RA0 input.
;*
;*  Conversion start & wait for complete
;*  polling code included.
;*
    BANKSEL    ADCON1      ; Select Bank 1
    CLRF       ADCON1      ; AVDD as VREF
    BSF        TRISA,0     ; Set RA0 as input
    BSF        ANSEL,0     ; Set RA0 as analog

    BANKSEL    ADCON0      ; Select Bank0
    MOVLW      B'11000001'
    MOVWF      ADCON0      ; RC, Ch 0, ADC on

;*****************************************
;*  Start & Wait for ADC complete, assumes
;*  minimum acquisition delay from
;*  configuration.

ADC_CNVRT
    BANKSEL    ADCON0      ; Select Bank 0
    BSF        ADCON0,GO   ; Start convert
ADC_CN_LOOP
    BTFSC      ADCON0,GO   ; Test for end
    GOTO       ADC_CN_LOOP ; If not, wait
    MOVF       ADRES,W     ; Get result
```


TABLE 11-1: REGISTERS ASSOCIATED WITH THE OPA MODULE

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other RESETS
11Ch	OPACON	OPAON	CMPEN	—	—	—	—	—	GBWP	00-- ---0	00-- ---0
110h	CALCON	CAL	CALERR	CALREF	—	—	—	—	—	000- ----	000- ----
9Dh	ANSEL	AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0	1111 1111	1111 1111
86h	TRISB	PORTB Data Direction Register								1111 1111	1111 1111
85h	TRISA	PORTA Data Direction Register								1111 1111	1111 1111
11Eh	DAC	DA7	DA6	DA5	DA4	DA3	DA1	DA1	DA0	0000 0000	0000 0000
11Fh	DACON0	DAON	DAOE	—	—	—	—	DARS1	DARS0	00-- --00	00-- --00

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used for the OPA module.

12.0 COMPARATOR MODULE

The comparator module has two separate voltage comparators: Comparator C1 and Comparator C2 (see Figure 12-1).

Each comparator offers the following list of features:

- Control and configuration register
- Comparator output available externally
- Programmable output polarity
- Interrupt-on-change flags
- Wake-up from SLEEP
- Configurable as feedback input to the PSMC
- Programmable four input multiplexer
- Programmable reference selections
- Programmable speed
- Output synchronization to Timer1 clock input (Comparator C2 only)

12.1 Control Registers

Both comparators have separate control and configuration registers: CM1CON0 for C1 and CM2CON0 for C2. In addition, Comparator C2 has a second control register, CM2CON1, for synchronization control and simultaneous reading of both comparator outputs.

12.1.1 COMPARATOR C1 CONTROL REGISTER

The CM1CON0 register (shown in Register 12-1) contains the control and status bits for the following:

- Comparator enable
- Comparator input selection
- Comparator reference selection
- Output mode
- Comparator speed

Setting C1ON (CM1CON0<7>) enables Comparator C1 for operation.

Bits C1CH<1:0> (CM1CON0<1:0>) select the comparator input from the four analog pins AN<7:4>.

Note:	To use AN<7:4> as analog inputs, the appropriate bits must be programmed in the ANSEL register.

Setting C1R (CM1CON0<2>) selects the output of the DAC module as the reference voltage for the comparator. Clearing C1R selects the VREF1 input on the RA3/AN3/VREF1 pin.

The output of the comparator is available internally via the C1OUT flag (CM1CON0<6>). To make the output available for an external connection, the C1OE flag (CM1CON0<5>) must be set. If the module is disabled with C1OE set, the output will be driven as shown in Table 12-2:

The polarity of the comparator output can be inverted by setting the C1POL flag (CM1CON0<4>). Clearing C1POL results in a non-inverted output. A complete table showing the output state versus input conditions and the polarity bit is shown in Table 12-2.

TABLE 12-1: OUTPUT STATE VERSUS INPUT CONDITIONS

Input Condition	C1POL	C1OUT
C1VN > C1VP	0	0
C1VN < C1VP	0	1
C1VN > C1VP	1	1
C1VN < C1VP	1	0

Note 1:	The internal output of the comparator is latched at the end of each instruction cycle. External outputs are not latched.
2:	The C1 interrupt will operate correctly with C1OE set or cleared.
3:	For the output of C1 on RB6/C1/PSMC1A, the PSMC must be disabled and TRISB<6> must be '0'.

C1SP (CM1CON0<3>) configures the speed of the comparator. When C1SP is set, the comparator operates at its normal speed. Clearing C1SP operates the comparator in a slower, low power mode.

REGISTER 12-1: COMPARATOR C1 CONTROL REGISTER0 (CM1CON0: 119h)

R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
C1ON	C1OUT	C1OE	C1POL	C1SP	C1R	C1CH1	C1CH0
bit 7							bit 0

bit 7 **C1ON:** Comparator C1 Enable bit
1 = C1 Comparator is enabled
0 = C1 Comparator is disabled

bit 6 **C1OUT:** Comparator C1 Output bit
If C1POL = 1 (inverted polarity):
C1OUT = 1, C1VP < C1VN
C1OUT = 0, C1VP > C1VN
If C1POL = 0 (non-inverted polarity):
C1OUT = 1, C1VP > C1VN
C1OUT = 0, C1VP < C1VN

bit 5 **C1OE:** Comparator C1 Output Enable bit
1 = C1OUT is present on the RB6/C1/PSMC1A pin(1)
0 = C1OUT is internal only

bit 4 **C1POL:** Comparator C1 Output Polarity Select bit
1 = C1OUT logic is inverted
0 = C1OUT logic is not inverted

bit 3 **C1SP:** Comparator C1 Speed Select bit
1 = C1 operates in normal speed mode
0 = C1 operates in low power, slow speed mode

bit 2 **C1R:** Comparator C1 Reference Select bits (non-inverting input)
1 = C1VP connects to V_{DAC} output
0 = C1VP connects to $V_{REF}1$

bit 1-0 **C1CH<1:0>:** Comparator C1 Channel Select bits
00 = C1VN of C1 connects to AN4
01 = C1VN of C1 connects to AN5
10 = C1VN of C1 connects to AN6
11 = C1VN of C1 connects to AN7

Note 1: C1OUT will only drive RB6/C1/PSMC1A if:
(C2OE = 1) & (C2ON = 1) & (TRISB<7> = 0) & ((SMCON = 0)
or ((SMCOM = 0) & (SCEN = 0))).

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

12.1.2.2 Control Register CM2CON1

Comparator C2 has one additional feature: its output can be synchronized to the Timer1 clock input. Setting C2SYNC (CM2CON1<0>) synchronizes the output of Comparator 2 to the falling edge of Timer 1's clock input (see Figure 12-1 and Register 12-3).

The CM2CON1 register also contains mirror copies of both comparator outputs, MC1OUT and MC2OUT (CM2CON1<7:6>). The ability to read both outputs simultaneously from a single register eliminates the timing skew of reading separate registers.

REGISTER 12-3: COMPARATOR C2 CONTROL REGISTER1 (CM2CON1: 11Bh)

R-0	R-0	U-0	U-0	U-0	U-0	U-0	R/W-0
MC1OUT	MC2OUT	—	—	—	—	—	C2SYNC
bit 7							bit 0

bit 7 **MC1OUT:** Mirror Copy of C1OUT (CM1CON0<6>)

bit 6 **MC2OUT:** Mirror Copy of C2OUT (CM2CON0<6>)

bit 5-1 **Unimplemented:** Read as '0'

bit 0 **C2SYNC:** C2 Output Synchronous Mode bit

1 = C2 output is synchronous to falling edge of TMR1 clock

0 = C2 output is asynchronous

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

FIGURE 13-2: PSMC MODULE IN DUAL ALTERNATING OUTPUT PWM MODE (SIMPLIFIED BLOCK DIAGRAM)

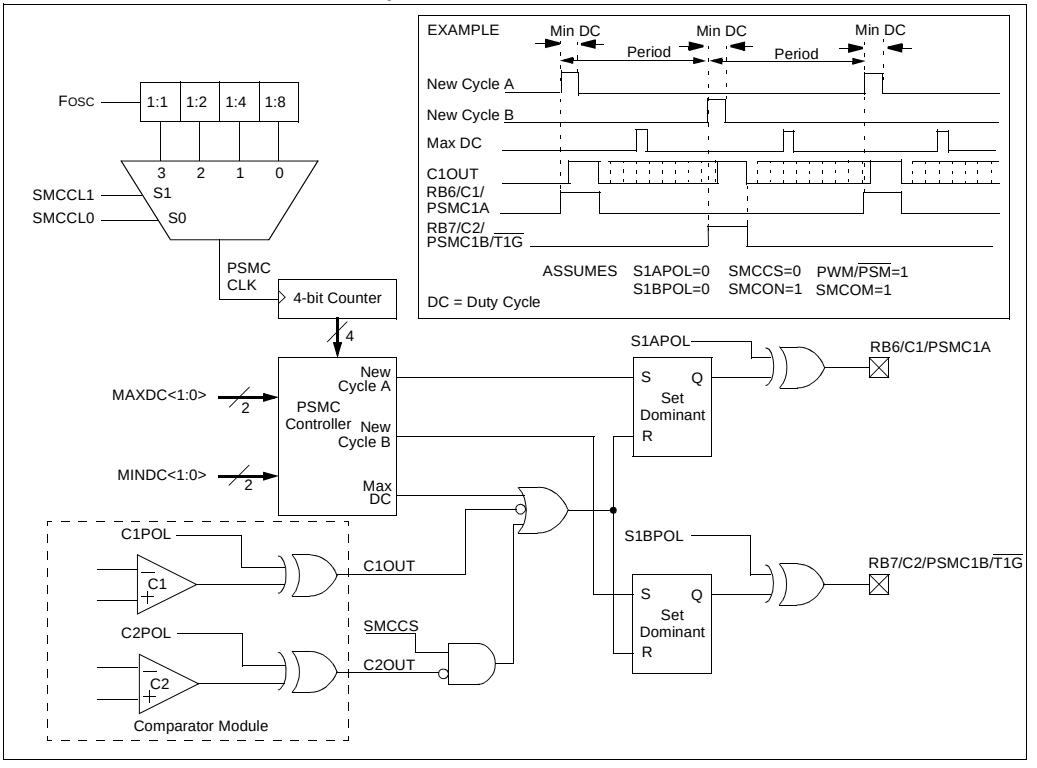


TABLE 13-1: PSMC1A OUTPUT SEQUENCE IN PWM MODE USING C1 COMPARATOR ONLY

Time	MINDC<1:0>	C1OUT	PSMC1A Output Signal
Beginning of PWM cycle	00	H	0 → 1
		L	0
	non-zero	x	0 → 1
During Min Duty Cycle	non-zero	x	1
After Min Duty Cycle, Before Max Duty Cycle	x	H → L	q→ 0
		L → H	0
Max Duty Cycle	x	x	q→ 0

Legend: x = Don't Care q = Prior State 0 = Inactive 1 = Active H = High L = Low

NOTES:

14.0 SPECIAL FEATURES OF THE CPU

These devices have a host of features intended to maximize system reliability, minimize cost through elimination of external components, provide power saving operating modes and offer code protection. These features include:

- Oscillator selection
- RESET
  - Power-on Reset (POR)
  - Power-up Timer (PWRT)
  - Oscillator Start-up Timer (OST)
  - Programmable Brown-out Reset (PBOR)
- Interrupts
- Watchdog Timer (WDT)
- Programmable Low Voltage Detection (PLVD)
- SLEEP
- Code protection
- ID locations
- In-Circuit Serial Programming™ (ICSP™)

Several oscillator options are available to allow the part to fit the application. The INTRC oscillator options save system cost while the LP crystal option saves power. A set of configuration bits is used to select various options.

The CPU also features a Watchdog Timer (WDT), which can be enabled either through a configuration bit during programming, or by the software. For added reliability, the WDT runs off its own internal RC oscillator instead of the main CPU clock.

In addition to the WDT, the CPU incorporates both an Oscillator Start-up Timer and a Power-up Timer. The Oscillator Start-up Timer (OST) is intended to hold the chip in RESET until the crystal oscillator has stabilized. The Power-up Timer (PWRT) holds the CPU in a fixed RESET delay of 72ms (nominal) on Power-up Resets (POR and PBOR), while the power supply stabilizes. With these two timers on-chip, most applications need no external RESET circuitry.

SLEEP mode is designed to offer a very low current power-down mode. The user can awaken from SLEEP through:

- External RESET
- Watchdog Timer Wake-up
- Interrupt

Additional information on special features is available in the PIC Mid-Range Reference Manual, (DS33023).

14.1 Configuration Bits

The configuration bits can be programmed (read as '0'), or left unprogrammed (read as '1'), to select various device configurations. These bits are mapped in program memory location 2007h.

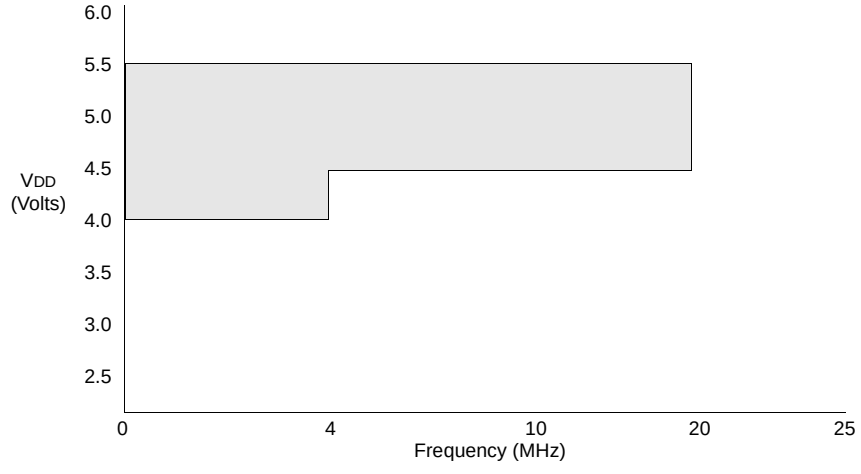
Note:	Address 2007h is beyond the user program memory space, which can be accessed only during programming.

Some of the core features provided may not be necessary for each application in which a device may be used. The configuration word bits allow these features to be configured/enabled/disabled as necessary. These features include:

- Code Protection
- PBOR Trip Point
- Power-up Timer
- Watchdog Timer
- Device Oscillator Mode

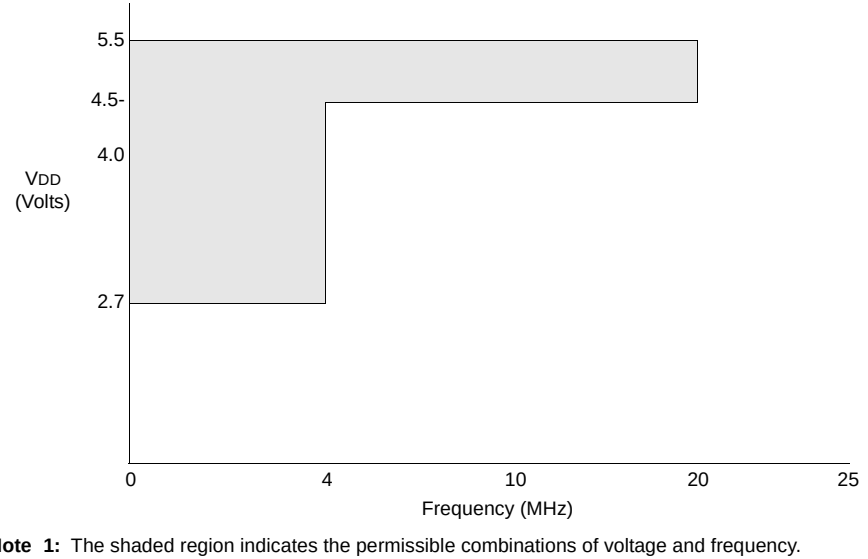
As can be seen in Table 14-1, some additional configuration word bits have been provided for Brown-out Reset trip point selection.

FIGURE 17-1: PIC16C781/782 VOLTAGE-FREQUENCY GRAPH, -40°C ≤ TA ≤ +85°C



Note 1: The shaded region indicates the permissible combinations of voltage and frequency.

FIGURE 17-2: PIC16LC781/782 VOLTAGE-FREQUENCY GRAPH, -40°C ≤ TA ≤ +85°C



Note 1: The shaded region indicates the permissible combinations of voltage and frequency.

17.1 DC Characteristics: Power Supply

TABLE 17-1: DC CHARACTERISTICS: PIC16C781/782, DSTEMP (INDUSTRIAL)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature-40°C ≤ TA ≤ +85°C for industrial				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
D001	VDD	**Supply Voltage**	4.0 4.5	— —	5.5 5.5	V —	XT, EC, RC, INTRC Oscillator HS Oscillator
D001A	VDD	**Supply Voltage** (DSTEMP)	2.7 4.5	— —	5.5 5.5	V V	XT, EC, RC, INTRC Oscillator HS Oscillator
D002*	VDR	**RAM Data Retention Voltage(1)**	—	1.5	—	V	
D003	VPOR	**VDD Start Voltage** to ensure internal Power-on Reset signal	—	TBD	—	V	See section on Power-on Reset for details
D004*	SVDD	**VDD Rise Rate** to ensure internal Power-on Reset signal	0.05	—	—	V/ms	See section on Power-on Reset for details. PWRT enabled
D010	IDD	**Supply Current(2)**	— — — —	TBD TBD TBD TBD	TBD TBD TBD TBD	mA mA mA mA	FOSC = 20 MHz, VDD = 5.5V* HS Oscillator FOSC = 20 MHz, VDD = 4.5V HS Oscillator FOSC = 4 MHz, VDD = 4.0V* XT, RC w/CLKOUT FOSC = 32 kHz, VDD = 4.0V LP Oscillator
D020 D020A	IPD	**Power-down Current(3)**	— —	TBD 1.5	TBD 19	µA µA	VDD = 5.5V VDD = 4.0V
	IOPA	**Operational Amplifier**	—	TBD TBD	TBD TBD	mA mA	VDD = 5.0V, GBWP = 0 VDD = 5.0V, GBWP = 1
	IVC*	**Voltage Comparators C1 and C2**	— —	TBD TBD	TBD TBD	mA mA	VDD = 5.0V, VID>100 mV C1SP = 0 VDD = 5.0 , VID>100 mV C1SP = 1
	IADC*	**Digital to Analog Converter (DAC)**	—	TBD	TBD	mA	VDD = 5.0V
D021	IWDT*	**Watchdog Timer**	—	TBD	TBD	mA	VDD = 4.0V
D026	IAD*	**Analog-to-Digital Converter (ADC)**	—	TBD	TBD	mA	VDD = 5.5V, ADC not converting
	IPLVD*	**Programmable Low Voltage Detect**		TBD	TBD	mA	VDD = 4.0V
	IPBOR*	**Programmable Brown-out Reset**		TBD	TBD	mA	VDD = 5.0V
1A	FOSC	**LP Oscillator, Operating Freq.** **INTRC Oscillator Operating Freq.** **XT Oscillator Operating Freq.** **HS Oscillator Operating Freq.**	9 — — 0 0	— 4 37 — —	200 — — 4 20	kHz MHz kHz MHz MHz	All temperatures All temperatures, OSCF = 1 All temperatures, OSCF = 0 All temperatures All temperatures

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail-to-rail; all I/O pins configured as inputs, pulled to VDD
$\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins configured as iputs and tied to VDD or VSS.

NOTES:

NOTES:

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