What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HCS12
Core Size	16-Bit
Speed	25MHz
Connectivity	CANbus, I²C, SCI, SPI
Peripherals	PWM, WDT
Number of I/O	91
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	2.35V ~ 5.25V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	112-LQFP
Supplier Device Package	112-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc9s12dg256bvpv

- 5V A/D converter inputs
- Operation at 50MHz equivalent to 25MHz Bus Speed
- Development support
- Single-wire background debug™ mode (BDM)
- On-chip hardware breakpoints

1.3 Modes of Operation

User modes

- Normal and Emulation Operating Modes
  - Normal Single-Chip Mode
  - Normal Expanded Wide Mode
  - Normal Expanded Narrow Mode
  - Emulation Expanded Wide Mode
  - Emulation Expanded Narrow Mode
- Special Operating Modes
  - Special Single-Chip Mode with active Background Debug Mode
  - Special Test Mode (**Motorola use only**)
  - Special Peripheral Mode (**Motorola use only**)

Low power modes

- Stop Mode
- Pseudo Stop Mode
- Wait Mode

$00A0 - $00C7 PWM (Pulse Width Modulator 8 Bit 8 Channel)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$00B1	PWMCNT5	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:	0	0	0	0	0	0	0	0
$00B2	PWMCNT6	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:	0	0	0	0	0	0	0	0
$00B3	PWMCNT7	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:	0	0	0	0	0	0	0	0
$00B4	PWMPER0	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$00B5	PWMPER1	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$00B6	PWMPER2	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$00B7	PWMPER3	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$00B8	PWMPER4	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$00B9	PWMPER5	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$00BA	PWMPER6	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$00BB	PWMPER7	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$00BC	PWMDTY0	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$00BD	PWMDTY1	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$00BE	PWMDTY2	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$00BF	PWMDTY3	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$00C0	PWMDTY4	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$00C1	PWMDTY5	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$00C2	PWMDTY6	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$00C3	PWMDTY7	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$00C4	PWMSDN	Read:	PWMIF	PWMIE	PWMRSTRT	PWMLVL	0	PWM7IN	PWM7INL	PWM7ENA
		Write:								
$00C5	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$00C6	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$00C7	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$0100 - $010F Flash Control Register (fts512k4)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0104	FPROT	Read:	FPOPEN	NV6	FPHDIS	FPHS1	FPHS0	FPLDIS	FPLS1	FPLS0
		Write:								
$0105	FSTAT	Read:	CBEIF	CCIF	PVIOL	ACCERR	0	BLANK	0	0
		Write:								
$0106	FCMD	Read:	0	CMDB6	CMDB5	0	0	CMDB2	0	CMDB0
		Write:								
$0107	Reserved for Factory Test	Read:	0	0	0	0	0	0	0	0
		Write:								
$0108	FADDRHI	Read:	0	Bit 14	13	12	11	10	9	Bit 8
		Write:								
$0109	FADDRLO	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$010A	FDATAHI	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$010B	FDATALO	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$010C	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$010D	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$010E	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$010F	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$0110 - $011B EEPROM Control Register (eets4k)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0110	ECLKDIV	Read:	EDIVLD	PRDIV8	EDIV5	EDIV4	EDIV3	EDIV2	EDIV1	EDIV0
		Write:								
$0111	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0112	Reserved for Factory Test	Read:	0	0	0	0	0	0	0	0
		Write:								
$0113	ECNFG	Read:	CBEIE	CCIE	0	0	0	0	0	0
		Write:								
$0114	EPROT	Read:	EPOPEN	NV6	NV5	NV4	EPDIS	EP2	EP1	EP0
		Write:								
$0115	ESTAT	Read:	CBEIF	CCIF	PVIOL	ACCERR	0	BLANK	0	0
		Write:								
$0116	ECMD	Read:	0	CMDB6	CMDB5	0	0	CMDB2	0	CMDB0
		Write:								
$0117	Reserved for Factory Test	Read:	0	0	0	0	0	0	0	0
		Write:								
$0118	EADDRHI	Read:	0	0	0	0	0	10	9	Bit 8
		Write:								

$0120 - $013F ATD1 (Analog to Digital Converter 10 Bit 8 Channel)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$012D	ATD1DIEN	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$012E	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$012F	PORTAD1	Read:	Bit7	6	5	4	3	2	1	BIT 0
		Write:								
$0130	ATD1DR0H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$0131	ATD1DR0L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$0132	ATD1DR1H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$0133	ATD1DR1L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$0134	ATD1DR2H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$0135	ATD1DR2L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$0136	ATD1DR3H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$0137	ATD1DR3L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$0138	ATD1DR4H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$0139	ATD1DR4L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$013A	ATD1DR5H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$013B	ATD1DR5L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$013C	ATD1DR6H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$013D	ATD1DR6L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$013E	ATD1DR7H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$013F	ATD1DR7L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								

$0140 - $017F CAN0 (Motorola Scalable CAN - MSCAN)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0140	CAN0CTL0	Read:	RXFRM	RXACT	CSWAI	SYNCH	TIME	WUPE	SLPRQ	INITRQ
		Write:								
$0141	CAN0CTL1	Read:	CANE	CLKSRC	LOOPB	LISTEN	0	WUPM	SLPAK	INITAK
		Write:								
$0142	CAN0BTR0	Read: Write:	SJW1	SJW0	BRP5	BRP4	BRP3	BRP2	BRP1	BRP0

$0200 - $023F CAN3 (Motorola Scalable CAN - MSCAN)

<table>
<tr><th>Address</th><th>Name</th><th></th><th>Bit 7</th><th>Bit 6</th><th>Bit 5</th><th>Bit 4</th><th>Bit 3</th><th>Bit 2</th><th>Bit 1</th><th>Bit 0</th></tr>
<tr><td rowspan="2">$0200</td><td rowspan="2">CAN3CTL0</td><td>Read:</td><td rowspan="2">RXFRM</td><td>RXACT</td><td rowspan="2">CSWAI</td><td>SYNCH</td><td rowspan="2">TIME</td><td rowspan="2">WUPE</td><td rowspan="2">SLPRQ</td><td rowspan="2">INITRQ</td></tr>
<tr><td>Write:</td><td></td><td></td></tr>
<tr><td rowspan="2">$0201</td><td rowspan="2">CAN3CTL1</td><td>Read:</td><td rowspan="2">CANE</td><td rowspan="2">CLKSRC</td><td rowspan="2">LOOPB</td><td rowspan="2">LISTEN</td><td>0</td><td rowspan="2">WUPM</td><td>SLPAK</td><td>INITAK</td></tr>
<tr><td>Write:</td><td></td><td></td><td></td></tr>
<tr><td rowspan="2">$0202</td><td rowspan="2">CAN3BTR0</td><td>Read:</td><td rowspan="2">SJW1</td><td rowspan="2">SJW0</td><td rowspan="2">BRP5</td><td rowspan="2">BRP4</td><td rowspan="2">BRP3</td><td rowspan="2">BRP2</td><td rowspan="2">BRP1</td><td rowspan="2">BRP0</td></tr>
<tr><td>Write:</td></tr>
<tr><td rowspan="2">$0203</td><td rowspan="2">CAN3BTR1</td><td>Read:</td><td rowspan="2">SAMP</td><td rowspan="2">TSEG22</td><td rowspan="2">TSEG21</td><td rowspan="2">TSEG20</td><td rowspan="2">TSEG13</td><td rowspan="2">TSEG12</td><td rowspan="2">TSEG11</td><td rowspan="2">TSEG10</td></tr>
<tr><td>Write:</td></tr>
<tr><td rowspan="2">$0204</td><td rowspan="2">CAN3RFLG</td><td>Read:</td><td rowspan="2">WUPIF</td><td rowspan="2">CSCIF</td><td>RSTAT1</td><td>RSTAT0</td><td>TSTAT1</td><td>TSTAT0</td><td rowspan="2">OVRIF</td><td rowspan="2">RXF</td></tr>
<tr><td>Write:</td><td></td><td></td><td></td><td></td></tr>
<tr><td rowspan="2">$0205</td><td rowspan="2">CAN3RIER</td><td>Read:</td><td rowspan="2">WUPIE</td><td rowspan="2">CSCIE</td><td rowspan="2">RSTATE1</td><td rowspan="2">RSTATE0</td><td rowspan="2">TSTATE1</td><td rowspan="2">TSTATE0</td><td rowspan="2">OVRIE</td><td rowspan="2">RXFIE</td></tr>
<tr><td>Write:</td></tr>
<tr><td rowspan="2">$0206</td><td rowspan="2">CAN3TFLG</td><td>Read:</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td rowspan="2">TXE2</td><td rowspan="2">TXE1</td><td rowspan="2">TXE0</td></tr>
<tr><td>Write:</td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td rowspan="2">$0207</td><td rowspan="2">CAN3TIER</td><td>Read:</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td rowspan="2">TXEIE2</td><td rowspan="2">TXEIE1</td><td rowspan="2">TXEIE0</td></tr>
<tr><td>Write:</td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td rowspan="2">$0208</td><td rowspan="2">CAN3TARQ</td><td>Read:</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td rowspan="2">ABTRQ2</td><td rowspan="2">ABTRQ1</td><td rowspan="2">ABTRQ0</td></tr>
<tr><td>Write:</td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td rowspan="2">$0209</td><td rowspan="2">CAN3TAAK</td><td>Read:</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>ABTAK2</td><td>ABTAK1</td><td>ABTAK0</td></tr>
<tr><td>Write:</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td rowspan="2">$020A</td><td rowspan="2">CAN3TBSEL</td><td>Read:</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td rowspan="2">TX2</td><td rowspan="2">TX1</td><td rowspan="2">TX0</td></tr>
<tr><td>Write:</td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td rowspan="2">$020B</td><td rowspan="2">CAN3IDAC</td><td>Read:</td><td>0</td><td>0</td><td rowspan="2">IDAM1</td><td rowspan="2">IDAM0</td><td>0</td><td>IDHIT2</td><td>IDHIT1</td><td>IDHIT0</td></tr>
<tr><td>Write:</td><td></td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td rowspan="2">$020C</td><td rowspan="2">Reserved</td><td>Read:</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>Write:</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td rowspan="2">$020D</td><td rowspan="2">Reserved</td><td>Read:</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>Write:</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td rowspan="2">$020E</td><td rowspan="2">CAN3RXERR</td><td>Read:</td><td>RXERR7</td><td>RXERR6</td><td>RXERR5</td><td>RXERR4</td><td>RXERR3</td><td>RXERR2</td><td>RXERR1</td><td>RXERR0</td></tr>
<tr><td>Write:</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td rowspan="2">$020F</td><td rowspan="2">CAN3TXERR</td><td>Read:</td><td>TXERR7</td><td>TXERR6</td><td>TXERR5</td><td>TXERR4</td><td>TXERR3</td><td>TXERR2</td><td>TXERR1</td><td>TXERR0</td></tr>
<tr><td>Write:</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td rowspan="2">$0210</td><td rowspan="2">CAN3IDAR0</td><td>Read:</td><td rowspan="2">AC7</td><td rowspan="2">AC6</td><td rowspan="2">AC5</td><td rowspan="2">AC4</td><td rowspan="2">AC3</td><td rowspan="2">AC2</td><td rowspan="2">AC1</td><td rowspan="2">AC0</td></tr>
<tr><td>Write:</td></tr>
<tr><td rowspan="2">$0211</td><td rowspan="2">CAN3IDAR1</td><td>Read:</td><td rowspan="2">AC7</td><td rowspan="2">AC6</td><td rowspan="2">AC5</td><td rowspan="2">AC4</td><td rowspan="2">AC3</td><td rowspan="2">AC2</td><td rowspan="2">AC1</td><td rowspan="2">AC0</td></tr>
<tr><td>Write:</td></tr>
<tr><td rowspan="2">$0212</td><td rowspan="2">CAN3IDAR2</td><td>Read:</td><td rowspan="2">AC7</td><td rowspan="2">AC6</td><td rowspan="2">AC5</td><td rowspan="2">AC4</td><td rowspan="2">AC3</td><td rowspan="2">AC2</td><td rowspan="2">AC1</td><td rowspan="2">AC0</td></tr>
<tr><td>Write:</td></tr>
<tr><td rowspan="2">$0213</td><td rowspan="2">CAN3IDAR3</td><td>Read:</td><td rowspan="2">AC7</td><td rowspan="2">AC6</td><td rowspan="2">AC5</td><td rowspan="2">AC4</td><td rowspan="2">AC3</td><td rowspan="2">AC2</td><td rowspan="2">AC1</td><td rowspan="2">AC0</td></tr>
<tr><td>Write:</td></tr>
<tr><td rowspan="2">$0214</td><td rowspan="2">CAN3IDMR0</td><td>Read:</td><td rowspan="2">AM7</td><td rowspan="2">AM6</td><td rowspan="2">AM5</td><td rowspan="2">AM4</td><td rowspan="2">AM3</td><td rowspan="2">AM2</td><td rowspan="2">AM1</td><td rowspan="2">AM0</td></tr>
<tr><td>Write:</td></tr>
<tr><td rowspan="2">$0215</td><td rowspan="2">CAN3IDMR1</td><td>Read:</td><td rowspan="2">AM7</td><td rowspan="2">AM6</td><td rowspan="2">AM5</td><td rowspan="2">AM4</td><td rowspan="2">AM3</td><td rowspan="2">AM2</td><td rowspan="2">AM1</td><td rowspan="2">AM0</td></tr>
<tr><td>Write:</td></tr>
<tr><td rowspan="2">$0216</td><td rowspan="2">CAN3IDMR2</td><td>Read:</td><td rowspan="2">AM7</td><td rowspan="2">AM6</td><td rowspan="2">AM5</td><td rowspan="2">AM4</td><td rowspan="2">AM3</td><td rowspan="2">AM2</td><td rowspan="2">AM1</td><td rowspan="2">AM0</td></tr>
<tr><td>Write:</td></tr>
<tr><td rowspan="2">$0217</td><td rowspan="2">CAN3IDMR3</td><td>Read:</td><td rowspan="2">AM7</td><td rowspan="2">AM6</td><td rowspan="2">AM5</td><td rowspan="2">AM4</td><td rowspan="2">AM3</td><td rowspan="2">AM2</td><td rowspan="2">AM1</td><td rowspan="2">AM0</td></tr>
<tr><td>Write:</td></tr>
<tr><td rowspan="2">$0218</td><td rowspan="2">CAN3IDAR4</td><td>Read:</td><td rowspan="2">AC7</td><td rowspan="2">AC6</td><td rowspan="2">AC5</td><td rowspan="2">AC4</td><td rowspan="2">AC3</td><td rowspan="2">AC2</td><td rowspan="2">AC1</td><td rowspan="2">AC0</td></tr>
<tr><td>Write:</td></tr>
</table>

$0240 - $027F PIM (Port Integration Module PIM_9DP256)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$024E	WOMS	Read: Write:	WOMS7	WOMS6	WOMS5	WOMS4	WOMS3	WOMS2	WOMS1	WOMS0
$024F	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0250	PTM	Read: Write:	PTM7	PTM6	PTM5	PTM4	PTM3	PTM2	PTM1	PTM0
$0251	PTIM	Read:	PTIM7	PTIM6	PTIM5	PTIM4	PTIM3	PTIM2	PTIM1	PTIM0
		Write:								
$0252	DDRM	Read: Write:	DDRM7	DDRM7	DDRM5	DDRM4	DDRM3	DDRM2	DDRM1	DDRM0
$0253	RDRM	Read: Write:	RDRM7	RDRM6	RDRM5	RDRM4	RDRM3	RDRM2	RDRM1	RDRM0
$0254	PERM	Read: Write:	PERM7	PERM6	PERM5	PERM4	PERM3	PERM2	PERM1	PERM0
$0255	PPSM	Read: Write:	PPSM7	PPSM6	PPSM5	PPSM4	PPSM3	PPSM2	PPSM1	PPSM0
$0256	WOMM	Read: Write:	WOMM7	WOMM6	WOMM5	WOMM4	WOMM3	WOMM2	WOMM1	WOMM0
$0257	MODRR	Read:	0	MODRR6	MODRR5	MODRR4	MODRR3	MODRR2	MODRR1	MODRR0
		Write:								
$0258	PTP	Read: Write:	PTP7	PTP6	PTP5	PTP4	PTP3	PTP2	PTP1	PTP0
$0259	PTIP	Read:	PTIP7	PTIP6	PTIP5	PTIP4	PTIP3	PTIP2	PTIP1	PTIP0
		Write:								
$025A	DDRP	Read: Write:	DDRP7	DDRP7	DDRP5	DDRP4	DDRP3	DDRP2	DDRP1	DDRP0
$025B	RDRP	Read: Write:	RDRP7	RDRP6	RDRP5	RDRP4	RDRP3	RDRP2	RDRP1	RDRP0
$025C	PERP	Read: Write:	PERP7	PERP6	PERP5	PERP4	PERP3	PERP2	PERP1	PERP0
$025D	PPSP	Read: Write:	PPSP7	PPSP6	PPSP5	PPSP4	PPSP3	PPSP2	PPSP1	PPSS0
$025E	PIEP	Read: Write:	PIEP7	PIEP6	PIEP5	PIEP4	PIEP3	PIEP2	PIEP1	PIEP0
$025F	PIFP	Read: Write:	PIFP7	PIFP6	PIFP5	PIFP4	PIFP3	PIFP2	PIFP1	PIFP0
$0260	PTH	Read: Write:	PTH7	PTH6	PTH5	PTH4	PTH3	PTH2	PTH1	PTH0
$0261	PTIH	Read:	PTIH7	PTIH6	PTIH5	PTIH4	PTIH3	PTIH2	PTIH1	PTIH0
		Write:								
$0262	DDRH	Read: Write:	DDRH7	DDRH7	DDRH5	DDRH4	DDRH3	DDRH2	DDRH1	DDRH0
$0263	RDRH	Read: Write:	RDRH7	RDRH6	RDRH5	RDRH4	RDRH3	RDRH2	RDRH1	RDRH0
$0264	PERH	Read: Write:	PERH7	PERH6	PERH5	PERH4	PERH3	PERH2	PERH1	PERH0
$0265	PPSH	Read: Write:	PPSH7	PPSH6	PPSH5	PPSH4	PPSH3	PPSH2	PPSH1	PPSH0
$0266	PIEH	Read: Write:	PIEH7	PIEH6	PIEH5	PIEH4	PIEH3	PIEH2	PIEH1	PIEH0

1.7 Part ID Assignments

The part ID is located in two 8-bit registers PARTIDH and PARTIDL (addresses $001A and $001B after reset). The read-only value is a unique part ID for each revision of the chip. **Table 1-3** shows the assigned part ID number.

Table 1-3 Assigned Part ID Numbers

Device	Mask Set Number	Part ID[1]
MC9S12DP256	0K79X	$0010
MC9S12DP256	1K79X	$0011
MC9S12DP256	2K79X	$0012

NOTES:
1. The coding is as follows:
Bit 15-12: Major family identifier
Bit 11-8: Minor family identifier
Bit 7-4: Major mask set revision number including FAB transfers
Bit 3-0: Minor - non full - mask set revision

The device memory sizes are located in two 8-bit registers MEMSIZ0 and MEMSIZ1 (addresses $001C and $001D after reset). **Table 1-4** shows the read-only values of these registers. Refer to section Module Mapping and Control (MMC) of HCS12 Core User Guide for further details.

Table 1-4 Memory size registers

Register name	Value
MEMSIZ0	$25
MEMSIZ1	$81

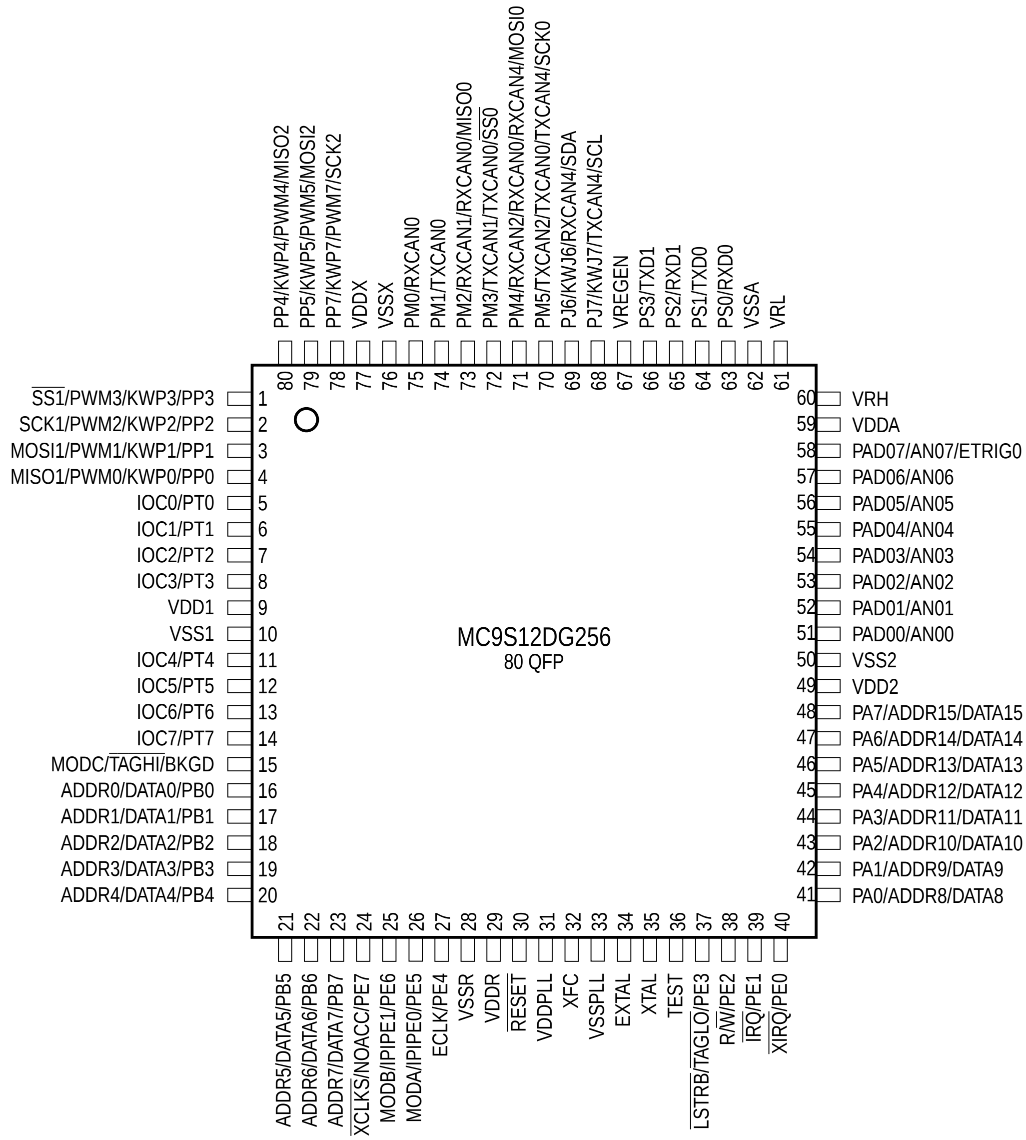


Figure 2-2 Pin Assignments in 80-pin QFP for MC9S12DG256

2.3.2 $\overline{\text{RESET}}$ — External Reset Pin

An active low bidirectional control signal, it acts as an input to initialize the MCU to a known start-up state, and an output when an internal MCU function causes a reset.

2.3.3 TEST — Test Pin

This input only pin is reserved for test.

NOTE: *The TEST pin must be tied to VSS in all applications.*

2.3.4 VREGEN — Voltage Regulator Enable Pin

This input only pin enables or disables the on-chip voltage regulator.

2.3.5 XFC — PLL Loop Filter Pin

PLL loop filter. Please ask your Motorola representative for the interactive application note to compute PLL loop filter elements. Any current leakage on this pin must be avoided.

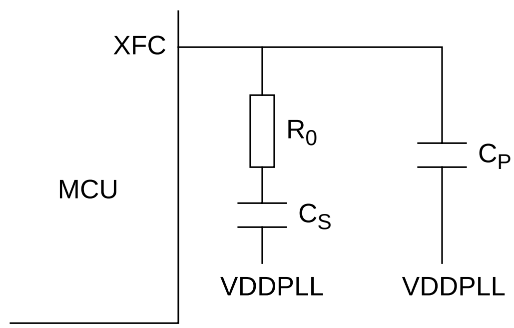


Figure 2-4 PLL Loop Filter Connections

2.3.6 BKGD / $\overline{\text{TAGHI}}$ / MODC — Background Debug, Tag High, and Mode Pin

The BKGD/$\overline{\text{TAGHI}}$/MODC pin is used as a pseudo-open-drain pin for the background debug communication. In MCU expanded modes of operation when instruction tagging is on, an input low on this pin during the falling edge of E-clock tags the high half of the instruction word being read into the instruction queue. It is used as a MCU operating mode select pin during reset. The state of this pin is latched to the MODC bit at the rising edge of $\overline{\text{RESET}}$.

2.3.7 PAD15 / AN15 / ETRIG1 — Port AD Input Pin of ATD1

PAD15 is a general purpose input pin and analog input AN7 of the analog to digital converter ATD1. It can act as an external trigger input for the ATD1.

- Every supply pair must be decoupled by a ceramic capacitor connected as near as possible to the corresponding pins(C1 - C6).
- Central point of the ground star should be the VSSR pin.
- Use low ohmic low inductance connections between VSS1, VSS2 and VSSR.
- VSSPLL must be directly connected to VSSR.
- Keep traces of VSSPLL, EXTAL and XTAL as short as possible and occupied board area for C7, C8, C11 and Q1 as small as possible.
- Do not place other signals or supplies underneath area occupied by C7, C8, C10 and Q1 and the connection area to the MCU.
- Central power input should be fed in at the VDDA/VSSA pins.

The VDDX, VSSX, VDDR and VSSR pairs supply the I/O pins, VDDR supplies also the internal voltage regulator.

VDD1, VSS1, VDD2 and VSS2 are the supply pins for the digital logic, VDDPLL, VSSPLL supply the oscillator and the PLL.

VSS1 and VSS2 are internally connected by metal.

VDDA, VDDX, VDDR as well as VSSA, VSSX, VSSR are connected by anti-parallel diodes for ESD protection.

NOTE: *In the following context VDD5 is used for either VDDA, VDDR and VDDX; VSS5 is used for either VSSA, VSSR and VSSX unless otherwise noted.*
IDD5 denotes the sum of the currents flowing into the VDDA, VDDX and VDDR pins.
VDD is used for VDD1, VDD2 and VDDPLL, VSS is used for VSS1, VSS2 and VSSPLL.
IDD is used for the sum of the currents flowing into VDD1 and VDD2.

A.1.3 Pins

There are four groups of functional pins.

A.1.3.1 5V I/O pins

Those I/O pins have a nominal level of 5V. This class of pins is comprised of all port I/O pins, the analog inputs, BKGD and the RESET pins.The internal structure of all those pins is identical, however some of the functionality may be disabled. E.g. for the analog inputs the output drivers, pull-up and pull-down resistors are disabled permanently.

A.1.3.2 Analog Reference

This group is made up by the VRH and VRL pins.

A.1.3.3 Oscillator

The pins XFC, EXTAL, XTAL dedicated to the oscillator have a nominal 2.5V level. They are supplied by VDDPLL.

A.1.3.4 TEST

This pin is used for production testing only.

A.1.3.5 VREGEN

This pin is used to enable the on chip voltage regulator.

$$T_J = T_A + (P_D \bullet \Theta_{JA})$$

T_J = Junction Temperature, [°C]

T_A = Ambient Temperature, [°C]

P_D = Total Chip Power Dissipation, [W]

Θ_{JA} = Package Thermal Resistance, [°C/W]

The total power dissipation can be calculated from:

$$P_D = P_{INT} + P_{IO}$$

P_{INT} = Chip Internal Power Dissipation, [W]

Two cases with internal voltage regulator enabled and disabled must be considered:

1. Internal Voltage Regulator disabled

$$P_{INT} = I_{DD} \cdot V_{DD} + I_{DDPLL} \cdot V_{DDPLL} + I_{DDA} \cdot V_{DDA}$$

$$P_{IO} = \sum_i R_{DSON} \cdot I_{IO_i}^{\ 2}$$

P_{IO} is the sum of all output currents on I/O ports associated with VDDX and VDDR.

For R_{DSON} is valid:

$$R_{DSON} = \frac{V_{OL}}{I_{OL}}\text{;for outputs driven low}$$

respectively

$$R_{DSON} = \frac{V_{DD5} - V_{OH}}{I_{OH}}\text{;for outputs driven high}$$

2. Internal voltage regulator enabled

$$P_{INT} = I_{DDR} \cdot V_{DDR} + I_{DDA} \cdot V_{DDA}$$

I_{DDR} is the current shown in **Table A-7** and not the overall current flowing into VDDR, which additionally contains the current flowing into the external loads with output high.

$$P_{IO} = \sum_i R_{DSON} \cdot I_{IO_i}^{\ 2}$$

P_{IO} is the sum of all output currents on I/O ports associated with VDDX and VDDR.

A.1.10 Supply Currents

This section describes the current consumption characteristics of the device as well as the conditions for the measurements.

A.1.10.1 Measurement Conditions

All measurements are without output loads. Unless otherwise noted the currents are measured in single chip mode, internal voltage regulator enabled and at 25MHz bus frequency using a 4MHz oscillator in Colpitts mode. Production testing is performed using a square wave signal at the EXTAL input.

A.1.10.2 Additional Remarks

In expanded modes the currents flowing in the system are highly dependent on the load at the address, data and control signals as well as on the duty cycle of those signals. No generally applicable numbers can be

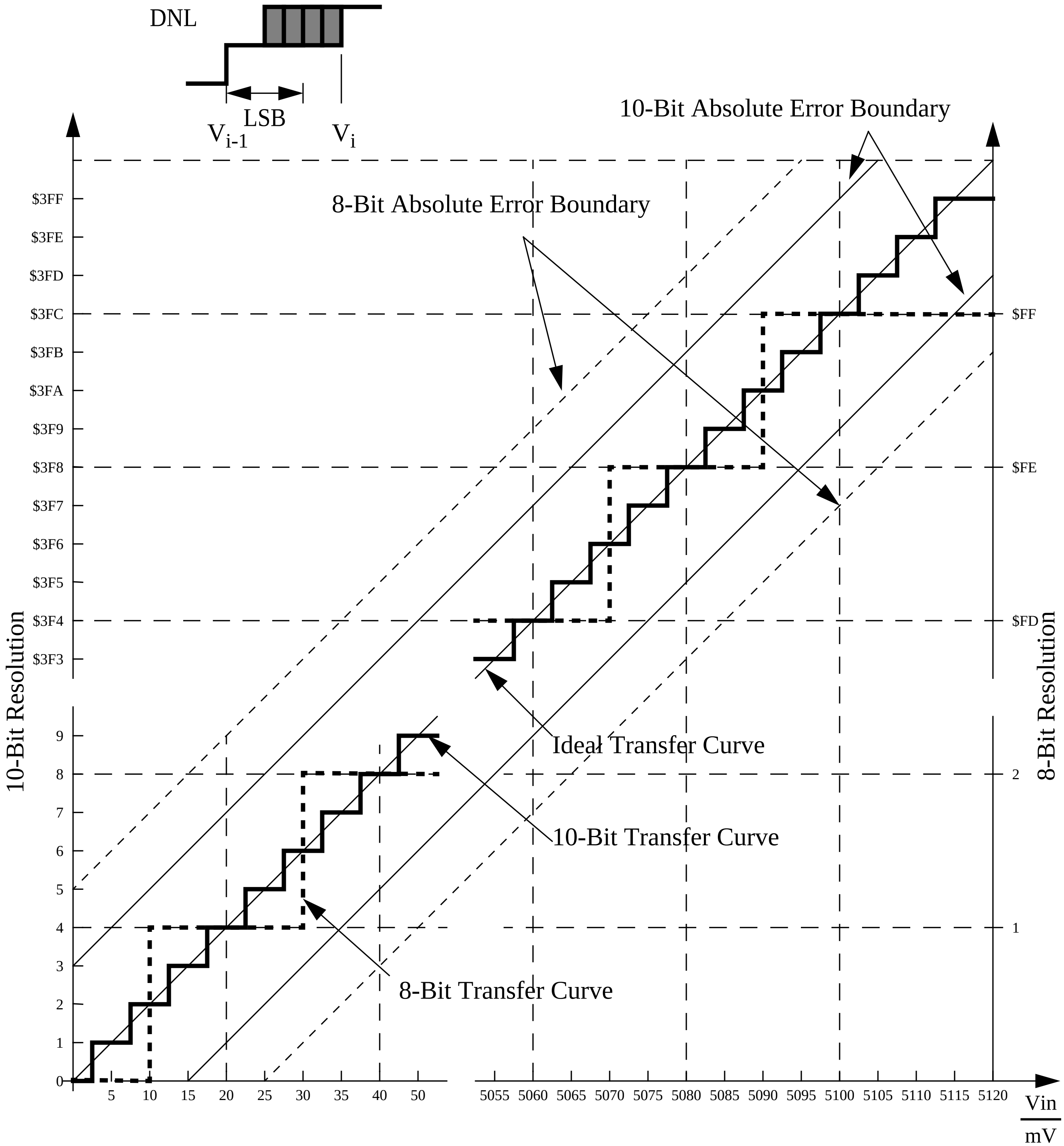


Figure A-1 ATD Accuracy Definitions

NOTE: ***Figure A-1*** *shows only definitions, for specification values refer to* ***Table A-10****.*

A.5.3 Phase Locked Loop

The oscillator provides the reference clock for the PLL. The PLL´s Voltage Controlled Oscillator (VCO) is also the system clock source in self clock mode.

A.5.3.1 XFC Component Selection

This section describes the selection of the XFC components to achieve a good filter characteristics.

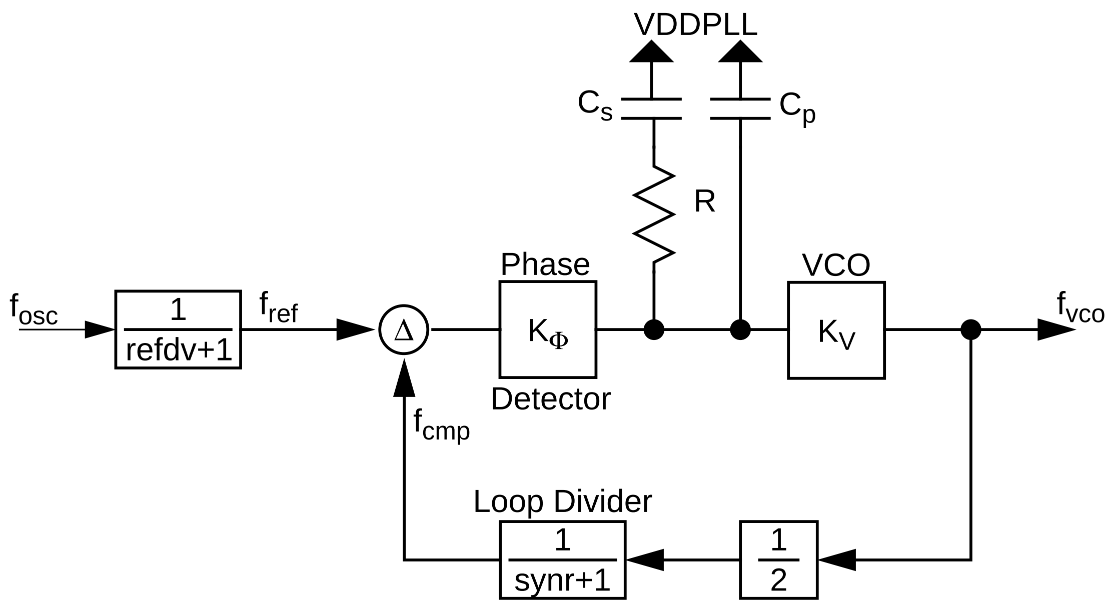


Figure A-2 Basic PLL functional diagram

The following procedure can be used to calculate the resistance and capacitance values using typical values for K_1, f_1 and i_{ch} from **Table A-16**.

The VCO Gain at the desired VCO output frequency is approximated by:

$$K_V = K_1 \cdot e^{\frac{(f_1 - f_{vco})}{K_1 \cdot 1V}}$$

The phase detector relationship is given by:

$$K_\Phi = -|i_{ch}| \cdot K_V$$

i_{ch} is the current in tracking mode.

This is very important to notice with respect to timers, serial modules where a pre-scaler will eliminate the effect of the jitter to a large extent.

Table A-16 PLL Characteristics

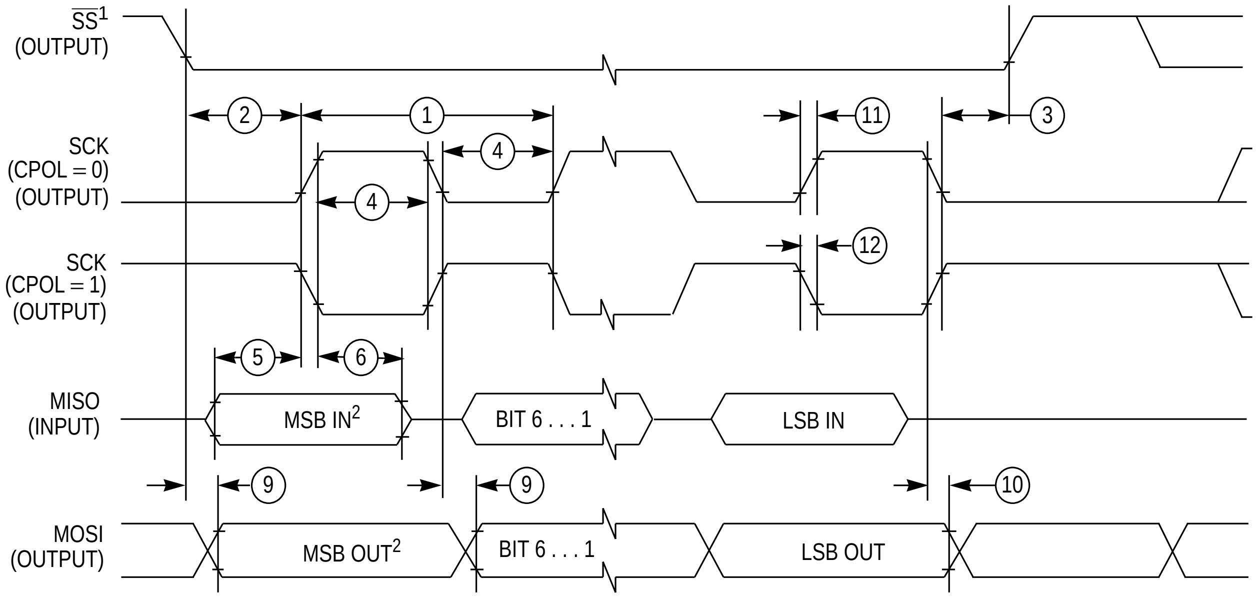
Conditions are shown in **Table A-4** unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	P	Self Clock Mode frequency	f_{SCM}	1		5.5	MHz
2	D	VCO locking range	f_{VCO}	8		50	MHz
3	D	Lock Detector transition from Acquisition to Tracking mode	$\|\Delta_{trk}\|$	3		4	%[1]
4	D	Lock Detection	$\|\Delta_{Lock}\|$	0		1.5	%[1]
5	D	Un-Lock Detection	$\|\Delta_{unl}\|$	0.5		2.5	%[1]
6	D	Lock Detector transition from Tracking to Acquisition mode	$\|\Delta_{unt}\|$	6		8	%[1]
7	C	PLLON Total Stabilization delay (Auto Mode) [2]	t_{stab}		0.5		ms
8	D	PLLON Acquisition mode stabilization delay [2]	t_{acq}		0.3		ms
9	D	PLLON Tracking mode stabilization delay [2]	t_{al}		0.2		ms
10	D	Fitting parameter VCO loop gain	K_1		-120		MHz/V
11	D	Fitting parameter VCO loop frequency	f_1		75		MHz
12	D	Charge pump current acquisition mode	$\| i_{ch} \|$		38.5		µA
13	D	Charge pump current tracking mode	$\| i_{ch} \|$		3.5		µA
14	C	Jitter fit parameter 1[2]	j_1			1.1	%
15	C	Jitter fit parameter 2[2]	j_2			0.13	%

NOTES:
1. % deviation from target frequency
2. f_{REF} = 4MHz, f_{BUS} = 25MHz equivalent f_{VCO} = 50MHz: REFDV = #$03, SYNR = #$018, Cs = 4.7nF, Cp = 470pF, Rs = 10KΩ.

A.7 SPI

A.7.1 Master Mode

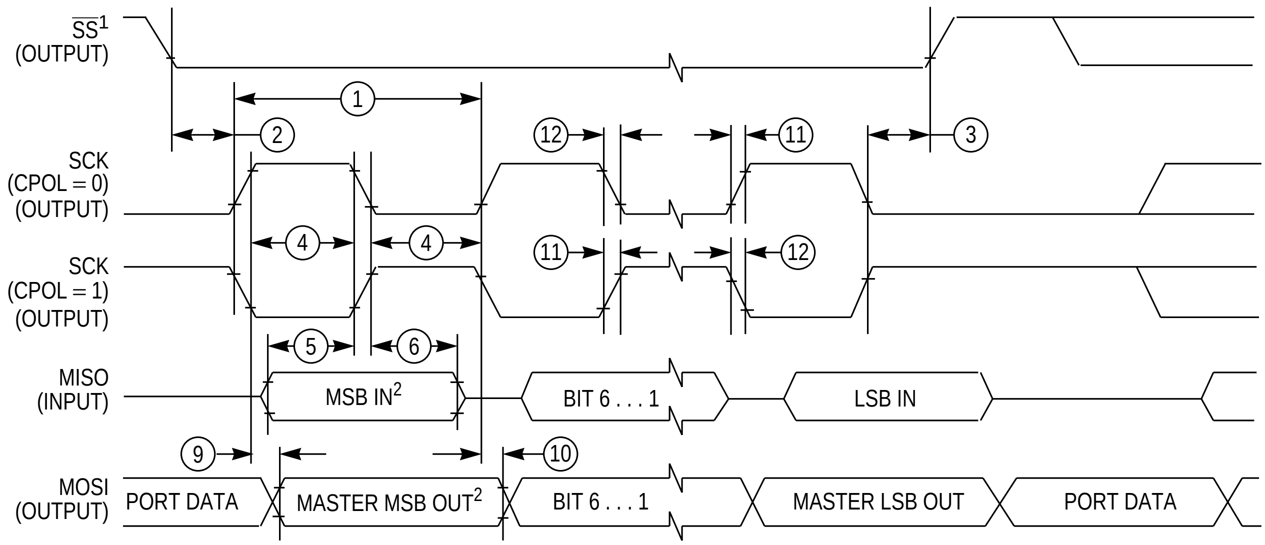
Figure A-5 and **Figure A-6** illustrate the master mode timing. Timing values are shown in **Table A-18**.



1. If configured as output.

2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure A-5 SPI Master Timing (CPHA = 0)



1. If configured as output
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure A-6 SPI Master Timing (CPHA =1)

Table A-18 SPI Master Mode Timing Characteristics[1]

Conditions are shown in **Table A-4** unless otherwise noted, C_{LOAD} = 200pF on all outputs							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	P	Operating Frequency	f_{op}	DC		1/4	f_{bus}
1	P	SCK Period $t_{sck} = 1./f_{op}$	t_{sck}	4		2048	t_{bus}
2	D	Enable Lead Time	t_{lead}	1/2		—	t_{sck}
3	D	Enable Lag Time	t_{lag}	1/2			t_{sck}
4	D	Clock (SCK) High or Low Time	t_{wsck}	t_{bus} – 30		1024 t_{bus}	ns
5	D	Data Setup Time (Inputs)	t_{su}	25			ns
6	D	Data Hold Time (Inputs)	t_{hi}	0			ns
9	D	Data Valid (after Enable Edge)	t_v			25	ns
10	D	Data Hold Time (Outputs)	t_{ho}	0			ns
11	D	Rise Time Inputs and Outputs	t_r			25	ns
12	D	Fall Time Inputs and Outputs	t_f			25	ns

NOTES:
1. The numbers 7, 8 in the column labeled “Num” are missing. This has been done on purpose to be consistent between the Master and the Slave timing shown in **Table A-19**.