



Welcome to [E-XFL.COM](https://www.e-xfl.com)

### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Obsolete
Core Processor	HCS12
Core Size	16-Bit
Speed	25MHz
Connectivity	CANbus, I <sup>2</sup> C, SCI, SPI
Peripherals	PWM, WDT
Number of I/O	59
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	2.35V ~ 5.25V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-QFP
Supplier Device Package	80-QFP (14x14)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s12dj256ccfu">https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s12dj256ccfu</a>

2.3.57	PS0 / RXD0 — Port S I/O Pin 0 . . . . .	67
2.3.58	PT[7:0] / IOC[7:0] — Port T I/O Pins [7:0] . . . . .	67
2.4	Power Supply Pins . . . . .	67
2.4.1	VDDX, VSSX — Power & Ground Pins for I/O Drivers . . . . .	68
2.4.2	VDDR, VSSR — Power & Ground Pins for I/O Drivers & for Internal Voltage Regulator 68	
2.4.3	VDD1, VDD2, VSS1, VSS2 — Core Power Pins . . . . .	68
2.4.4	VDDA, VSSA — Power Supply Pins for ATD and VREG . . . . .	68
2.4.5	VRH, VRL — ATD Reference Voltage Input Pins . . . . .	68
2.4.6	VDDPLL, VSSPLL — Power Supply Pins for PLL . . . . .	68
2.4.7	VREGEN — On Chip Voltage Regulator Enable . . . . .	69

## Section 3 System Clock Description

3.1	Overview. . . . .	71
-----	-------------------	----

## Section 4 Modes of Operation

4.1	Overview. . . . .	73
4.2	Chip Configuration Summary . . . . .	73
4.3	Security. . . . .	74
4.3.1	Securing the Microcontroller . . . . .	74
4.3.2	Operation of the Secured Microcontroller . . . . .	74
4.3.3	Unsecuring the Microcontroller . . . . .	75
4.4	Low Power Modes . . . . .	75
4.4.1	Stop . . . . .	75
4.4.2	Pseudo Stop. . . . .	75
4.4.3	Wait . . . . .	75
4.4.4	Run. . . . .	75

## Section 5 Resets and Interrupts

5.1	Overview. . . . .	77
5.2	Vectors . . . . .	77
5.2.1	Vector Table. . . . .	77
5.3	Effects of Reset . . . . .	78
5.3.1	I/O pins. . . . .	78
5.3.2	Memory . . . . .	79

## Section 6 HCS12 Core Block Description

## Preface

The Device User Guide provides information about the MC9S12DP256B device made up of standard HCS12 blocks and the HCS12 processor core.

**Table 0-1** and **Table 0-2** show the availability of peripheral modules on the various derivatives. For details about the compatibility within the MC9S12D-Family refer also to engineering bulletin EB386.

**Table 0-1 Drivative Differences MC9S12D256B**

Generic device	MC9S12DP256B	MC9S12DT256B	MC9S12DJ256B	MC9S12DG256B	MC9S12A256B
# of CANs	5	3	2	2	0
CAN0	✓	✓	✓	✓	
CAN1	✓	✓			
CAN2	✓				
CAN3	✓				
CAN4	✓	✓	✓	✓	
J1850/BDLC	✓		✓		
Package	112 LQFP	112 LQFP	112 LQFP/80 QFP	112 LQFP/80 QFP	112 LQFP/80 QFP
Mask set	0/1K79X	0/1K79X	0/1K79X	0/1K79X	0/1K79X
Temp Options	M, V, C	M, V, C	M, V, C	M, V, C	C
package Code	PV	PV	PV/FU	PV	PV/FU
Notes	An errata exists conntact Sales office	An errata exists conntact Sales office	An errata exists conntact Sales office	An errata exists conntact Sales office	An errata exists conntact Sales office

**Table 0-2 Derivative Differences MC9S12D256C**

Generic device	MC9S12DP256C	MC9S12DT256C	MC9S12DJ256C	MC9S12DG256C
# of CANs	5	3	2	2
CAN0	✓	✓	✓	✓
CAN1	✓	✓		
CAN2	✓			
CAN3	✓			
CAN4	✓	✓	✓	✓
J1850/BDLC	✓		✓	
Package	112 LQFP	112 LQFP	112 LQFP/80 QFP	112 LQFP/80 QFP
Mask set	2K79X	2K79X	2K79X	2K79X
Temp Options	M, V, C	M, V, C	M, V, C	M, V, C
package Code	PV	PV	PV/FU	PV
Notes	An errata exists contact Sales office	An errata exists contact Sales office	An errata exists contact Sales office	An errata exists contact Sales office

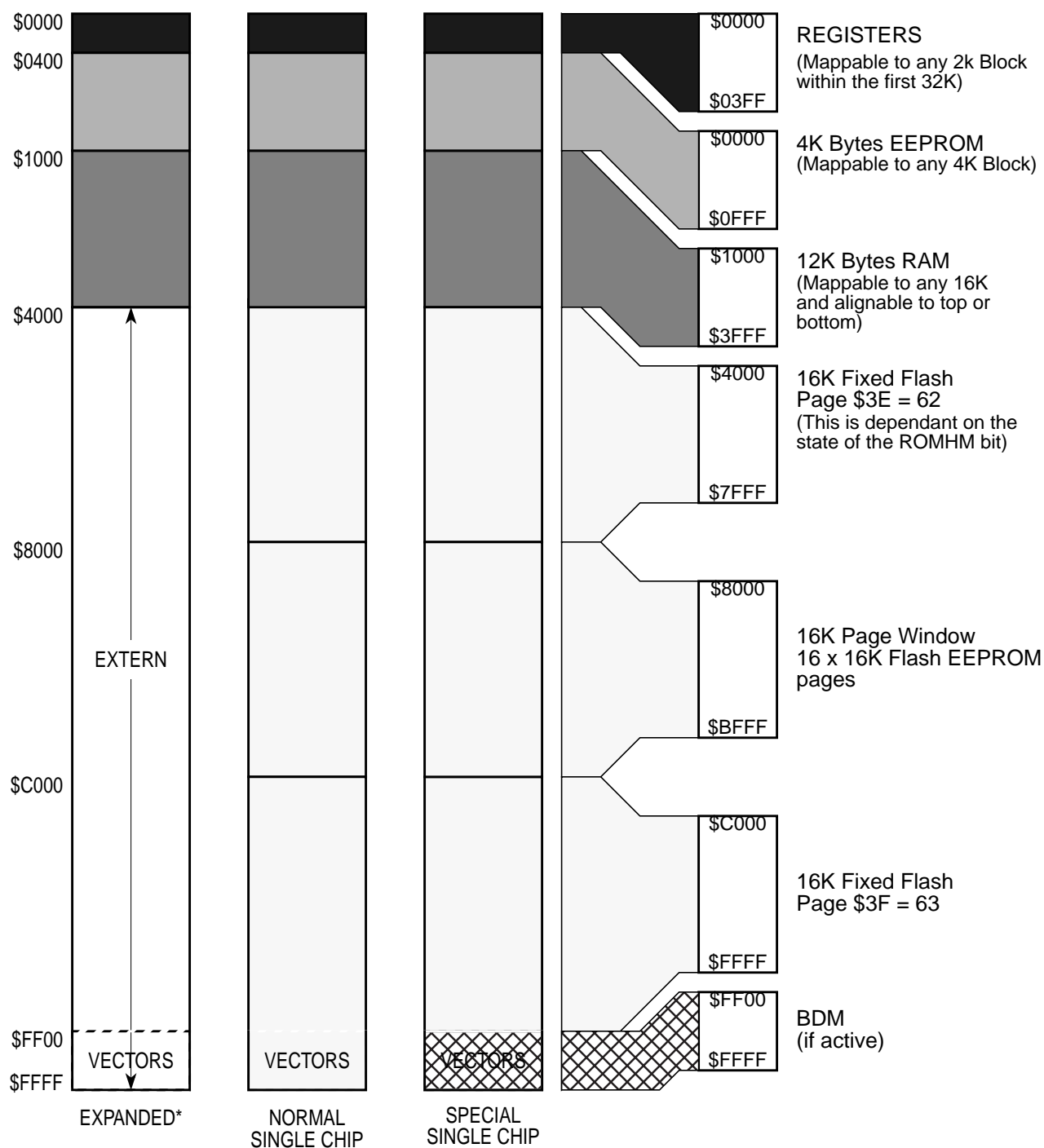
## 1.5 Device Memory Map

**Table 1-1** and **Figure 1-2** show the device memory map of the MC9S12DP256B after reset. Note that after reset the bottom 1k of the EEPROM (\$0000 - \$03FF) are hidden by the register space.

**Table 1-1 Device Memory Map**

Address	Module	Size (Bytes)
\$0000 - \$0017	CORE (Ports A, B, E, Modes, Inits, Test)	24
\$0018 - \$0019	Reserved	2
\$001A - \$001B	Device ID register (PARTID)	2
\$001C - \$001F	CORE (MEMSIZ, IRQ, HPRIO)	4
\$0020 - \$0027	Reserved	8
\$0028 - \$002F	CORE (Background Debug Mode)	8
\$0030 - \$0033	CORE (PPAGE, Port K)	4
\$0034 - \$003F	Clock and Reset Generator (PLL, RTI, COP)	12
\$0040 - \$007F	Enhanced Capture Timer 16-bit 8 channels	64
\$0080 - \$009F	Analog to Digital Converter 10-bit 8 channels (ATD0)	32
\$00A0 - \$00C7	Pulse Width Modulator 8-bit 8 channels (PWM)	40
\$00C8 - \$00CF	Serial Communications Interface 0 (SCI0)	8
\$00D0 - \$00D7	Serial Communications Interface 0 (SCI1)	8
\$00D8 - \$00DF	Serial Peripheral Interface (SPI0)	8
\$00E0 - \$00E7	Inter IC Bus	8
\$00E8 - \$00EF	Byte Data Link Controller (BDLC)	8
\$00F0 - \$00F7	Serial Peripheral Interface (SPI1)	8
\$00F8 - \$00FF	Serial Peripheral Interface (SPI2)	8
\$0100 - \$010F	Flash Control Register	16
\$0110 - \$011B	EEPROM Control Register	12
\$011C - \$011F	Reserved	4
\$0120 - \$013F	Analog to Digital Converter 10-bit 8 channels (ATD1)	32
\$0140 - \$017F	Motorola Scalable Can (CAN0)	64
\$0180 - \$01BF	Motorola Scalable Can (CAN1)	64
\$01C0 - \$01FF	Motorola Scalable Can (CAN2)	64
\$0200 - \$023F	Motorola Scalable Can (CAN3)	64
\$0240 - \$027F	Port Integration Module (PIM)	64
\$0280 - \$02BF	Motorola Scalable Can (CAN4)	64
\$02C0 - \$03FF	Reserved	320
\$0000 - \$0FFF	EEPROM array	4096
\$1000 - \$3FFF	RAM array	12288
\$4000 - \$7FFF	Fixed Flash EEPROM array incl. 0.5K, 1K, 2K or 4K Protected Sector at start	16384
\$8000 - \$BFFF	Flash EEPROM Page Window	16384

**Figure 1-2 MC9S12DP256B Memory Map**



\* Assuming that a '0' was driven onto port K bit 7 during MCU is reset into normal expanded wide or narrow mode.

**\$0010 - \$0014**

**MMC map 1 of 4 (Core User Guide)**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$0012	INITEE	Read:	EE15	EE14	EE13	EE12	0	0	0	EEON
		Write:								
\$0013	MISC	Read:	0	0	0	0	EXSTR1	EXSTR0	ROMHM	ROMON
		Write:								
\$0014	MTST0	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								

**\$0015 - \$0016**

**INT map 1 of 2 (Core User Guide)**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$0015	ITCR	Read:	0	0	0	WRINT	ADR3	ADR2	ADR1	ADR0
		Write:								
\$0016	ITEST	Read:	INTE	INTC	INTA	INT8	INT6	INT4	INT2	INT0
		Write:								

**\$0017 - \$0017**

**MMC map 2 of 4 (Core User Guide)**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$0017	MTST1	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								

**\$0018 - \$001B**

**Miscellaneous Peripherals (Device User Guide, Table 1-3)**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$0018	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
\$0019	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
\$001A	PARTIDH	Read:	ID15	ID14	ID13	ID12	ID11	ID10	ID9	ID8
		Write:								
\$001B	PARTIDL	Read:	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
		Write:								

**\$001C - \$001D**

**MMC map 3 of 4 (Core and Device User Guide, Table 1-4)**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$001C	MEMSIZ0	Read:	reg_sw0	0	eep_sw1	eep_sw0	0	ram_sw2	ram_sw1	ram_sw0
		Write:								
\$001D	MEMSIZ1	Read:	rom_sw1	rom_sw0	0	0	0	0	pag_sw1	pag_sw0
		Write:								



## Section 2 Signal Description

This section describes signals that connect off-chip. It includes a pinout diagram, a table of signal properties, and detailed discussion of signals. It is built from the signal description sections of the Block User Guides of the individual IP blocks on the device.

### 2.1 Device Pinout

The MC9S12DP256B/MC9S12DT256/MC9S12DJ256 and MC9S12DG256 is available in a 112-pin low profile quad flat pack (LQFP) and MC9S12DJ256 is also available in a 80-pin quad flat pack (QFP). Most pins perform two or more functions, as described in the Signal Descriptions. **Figure 2-1** and **Figure 2-3** show the pin assignments.



**2.3.23 PH5 / KWH5 / MOSI2 — Port H I/O Pin 5**

PH5 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as master output (during master mode) or slave input pin (during slave mode) MOSI of the Serial Peripheral Interface 2 (SPI2).

**2.3.24 PH4 / KWH4 / MISO2 — Port H I/O Pin 2**

PH4 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as master input (during master mode) or slave output (during slave mode) pin MISO of the Serial Peripheral Interface 2 (SPI2).

**2.3.25 PH3 / KWH3 /  $\overline{SS1}$  — Port H I/O Pin 3**

PH3 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as slave select pin  $\overline{SS}$  of the Serial Peripheral Interface 1 (SPI1).

**2.3.26 PH2 / KWH2 / SCK1 — Port H I/O Pin 2**

PH2 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as serial clock pin SCK of the Serial Peripheral Interface 1 (SPI1).

**2.3.27 PH1 / KWH1 / MOSI1 — Port H I/O Pin 1**

PH1 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as master output (during master mode) or slave input pin (during slave mode) MOSI of the Serial Peripheral Interface 1 (SPI1).

**2.3.28 PH0 / KWH0 / MISO1 — Port H I/O Pin 0**

PH0 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as master input (during master mode) or slave output (during slave mode) pin MISO of the Serial Peripheral Interface 1 (SPI1).

**2.3.29 PJ7 / KWJ7 / TXCAN4 / SCL — PORT J I/O Pin 7**

PJ7 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as the transmit pin TXCAN for the Motorola Scalable Controller Area Network controller 4 (CAN4) or the serial clock pin SCL of the IIC module.

**2.3.38 PM3 / TXCAN1 / TXCAN0 /  $\overline{SS}$ 0 — Port M I/O Pin 3**

PM3 is a general purpose input or output pin. It can be configured as the transmit pin TXCAN of the Motorola Scalable Controller Area Network controllers 1 or 0 (CAN1 or CAN0). It can be configured as the slave select pin  $\overline{SS}$  of the Serial Peripheral Interface 0 (SPI0).

**2.3.39 PM2 / RXCAN1 / RXCAN0 / MISO0 — Port M I/O Pin 2**

PM2 is a general purpose input or output pin. It can be configured as the receive pin RXCAN of the Motorola Scalable Controller Area Network controllers 1 or 0 (CAN1 or CAN0). It can be configured as the master input (during master mode) or slave output pin (during slave mode) MISO for the Serial Peripheral Interface 0 (SPI0).

**2.3.40 PM1 / TXCAN0 / TXB — Port M I/O Pin 1**

PM1 is a general purpose input or output pin. It can be configured as the transmit pin TXCAN of the Motorola Scalable Controller Area Network controller 0 (CAN0). It can be configured as the transmit pin TXB of the BDLC.

**2.3.41 PM0 / RXCAN0 / RXB — Port M I/O Pin 0**

PM0 is a general purpose input or output pin. It can be configured as the receive pin RXCAN of the Motorola Scalable Controller Area Network controller 0 (CAN0). It can be configured as the receive pin RXB of the BDLC.

**2.3.42 PP7 / KWP7 / PWM7 / SCK2 — Port P I/O Pin 7**

PP7 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as Pulse Width Modulator (PWM) channel 7 output. It can be configured as serial clock pin SCK of the Serial Peripheral Interface 2 (SPI2).

**2.3.43 PP6 / KWP6 / PWM6 /  $\overline{SS}$ 2 — Port P I/O Pin 6**

PP6 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as Pulse Width Modulator (PWM) channel 6 output. It can be configured as slave select pin  $\overline{SS}$  of the Serial Peripheral Interface 2 (SPI2).

**2.3.44 PP5 / KWP5 / PWM5 / MOSI2 — Port P I/O Pin 5**

PP5 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as Pulse Width Modulator (PWM) channel 5 output. It can be configured as master output (during master mode) or slave input pin (during slave mode) MOSI of the Serial Peripheral Interface 2 (SPI2).

## 2.4.1 VDDX,VSSX — Power & Ground Pins for I/O Drivers

External power and ground for I/O drivers. Because fast signal transitions place high, short-duration current demands on the power supply, use bypass capacitors with high-frequency characteristics and place them as close to the MCU as possible. Bypass requirements depend on how heavily the MCU pins are loaded.

## 2.4.2 VDDR, VSSR — Power & Ground Pins for I/O Drivers & for Internal Voltage Regulator

External power and ground for I/O drivers and input to the internal voltage regulator. Because fast signal transitions place high, short-duration current demands on the power supply, use bypass capacitors with high-frequency characteristics and place them as close to the MCU as possible. Bypass requirements depend on how heavily the MCU pins are loaded.

## 2.4.3 VDD1, VDD2, VSS1, VSS2 — Core Power Pins

Power is supplied to the MCU through VDD and VSS. Because fast signal transitions place high, short-duration current demands on the power supply, use bypass capacitors with high-frequency characteristics and place them as close to the MCU as possible. This 2.5V supply is derived from the internal voltage regulator. There is no static load on those pins allowed. The internal voltage regulator is turned off, if VREGEN is tied to ground.

**NOTE:** *No load allowed except for bypass capacitors.*

## 2.4.4 VDDA, VSSA — Power Supply Pins for ATD and VREG

VDDA, VSSA are the power supply and ground input pins for the voltage regulator and the analog to digital converter. It also provides the reference for the internal voltage regulator. This allows the supply voltage to the ATD and the reference voltage to be bypassed independently.

## 2.4.5 VRH, VRL — ATD Reference Voltage Input Pins

VRH and VRL are the reference voltage input pins for the analog to digital converter.

## 2.4.6 VDDPLL, VSSPLL — Power Supply Pins for PLL

Provides operating voltage and ground for the Oscillator and the Phased-Locked Loop. This allows the supply voltage to the Oscillator and PLL to be bypassed independently. This 2.5V voltage is generated by the internal voltage regulator.

**NOTE:** *No load allowed except for bypass capacitors.*

### 4.3.3 Unsecuring the Microcontroller

In order to unsecure the microcontroller, the internal FLASH and EEPROM must be erased. This can be done through an external program in expanded mode.

Once the user has erased the FLASH and EEPROM, the part can be reset into special single chip mode. This invokes a program that verifies the erasure of the internal FLASH and EEPROM. Once this program completes, the user can erase and program the FLASH security bits to the unsecured state. This is generally done through the BDM, but the user could also change to expanded mode (by writing the mode bits through the BDM) and jumping to an external program (again through BDM commands). Note that if the part goes through a reset before the security bits are reprogrammed to the unsecure state, the part will be secured again.

## 4.4 Low Power Modes

The microcontroller features three main low power modes. Consult the respective Block User Guide for information on the module behavior in Stop, Pseudo Stop, and Wait Mode. An important source of information about the clock system is the Clock and Reset Generator User Guide (CRG).

### 4.4.1 Stop

Executing the CPU STOP instruction stops all clocks and the oscillator thus putting the chip in fully static mode. Wake up from this mode can be done via reset or external interrupts.

### 4.4.2 Pseudo Stop

This mode is entered by executing the CPU STOP instruction. In this mode the oscillator is still running and the Real Time Interrupt (RTI) or Watchdog (COP) sub module can stay active. Other peripherals are turned off. This mode consumes more current than the full STOP mode, but the wake up time from this mode is significantly shorter.

### 4.4.3 Wait

This mode is entered by executing the CPU WAI instruction. In this mode the CPU will not execute instructions. The internal CPU signals (address and databus) will be fully static. All peripherals stay active. For further power consumption the peripherals can individually turn off their local clocks.

### 4.4.4 Run

Although this is not a low power mode, unused peripheral modules should not be enabled in order to save power.

## Section 5 Resets and Interrupts

### 5.1 Overview

Consult the Exception Processing section of the HCS12 Core User Guide for information on resets and interrupts.

### 5.2 Vectors

#### 5.2.1 Vector Table

**Table 5-1** lists interrupt sources and vectors in default order of priority.

**Table 5-1 Interrupt Vector Locations**

Vector Address	Interrupt Source	CCR Mask	Local Enable	HPRIO Value to Elevate
\$FFFE, \$FFFF	Reset	None	None	—
\$FFFC, \$FFFD	Clock Monitor fail reset	None	PLLCTL (CME, SCME)	—
\$FFFA, \$FFFB	COP failure reset	None	COP rate select	—
\$FFF8, \$FFF9	Unimplemented instruction trap	None	None	—
\$FFF6, \$FFF7	SWI	None	None	—
\$FFF4, \$FFF5	XIRQ	X-Bit	None	—
\$FFF2, \$FFF3	IRQ	I-Bit	IRQCR (IRQEN)	\$F2
\$FFF0, \$FFF1	Real Time Interrupt	I-Bit	CRGINT (RTIE)	\$F0
\$FFEE, \$FFEF	Enhanced Capture Timer channel 0	I-Bit	TIE (C0I)	\$EE
\$FFEC, \$FFED	Enhanced Capture Timer channel 1	I-Bit	TIE (C1I)	\$EC
\$FFEA, \$FFEB	Enhanced Capture Timer channel 2	I-Bit	TIE (C2I)	\$EA
\$FFE8, \$FFE9	Enhanced Capture Timer channel 3	I-Bit	TIE (C3I)	\$E8
\$FFE6, \$FFE7	Enhanced Capture Timer channel 4	I-Bit	TIE (C4I)	\$E6
\$FFE4, \$FFE5	Enhanced Capture Timer channel 5	I-Bit	TIE (C5I)	\$E4
\$FFE2, \$FFE3	Enhanced Capture Timer channel 6	I-Bit	TIE (C6I)	\$E2
\$FFE0, \$FFE1	Enhanced Capture Timer channel 7	I-Bit	TIE (C7I)	\$E0
\$FFDE, \$FFDF	Enhanced Capture Timer overflow	I-Bit	TSRC2 (TOF)	\$DE
\$FFDC, \$FFDD	Pulse accumulator A overflow	I-Bit	PACTL (PAOVI)	\$DC
\$FFDA, \$FFDB	Pulse accumulator input edge	I-Bit	PACTL (PAI)	\$DA
\$FFD8, \$FFD9	SPI0	I-Bit	SP0CR1 (SPIE, SPTIE)	\$D8
\$FFD6, \$FFD7	SCI0	I-Bit	SC0CR2 (TIE, TCIE, RIE, ILIE)	\$D6
\$FFD4, \$FFD5	SCI1	I-Bit	SC1CR2 (TIE, TCIE, RIE, ILIE)	\$D4
\$FFD2, \$FFD3	ATD0	I-Bit	ATD0CTL2 (ASCIE)	\$D2
\$FFD0, \$FFD1	ATD1	I-Bit	ATD1CTL2 (ASCIE)	\$D0
\$FFCE, \$FFCF	Port J	I-Bit	PTJIF (PTJIE)	\$CE
\$FFCC, \$FFCD	Port H	I-Bit	PTHIF (PTHIE)	\$CC
\$FFCA, \$FFCB	Modulus Down Counter underflow	I-Bit	MCCTL (MCZI)	\$CA

$$T_J = T_A + (P_D \cdot \Theta_{JA})$$

$T_J$  = Junction Temperature, [°C]

$T_A$  = Ambient Temperature, [°C]

$P_D$  = Total Chip Power Dissipation, [W]

$\Theta_{JA}$  = Package Thermal Resistance, [°C/W]

The total power dissipation can be calculated from:

$$P_D = P_{INT} + P_{IO}$$

$P_{INT}$  = Chip Internal Power Dissipation, [W]

Two cases with internal voltage regulator enabled and disabled must be considered:

1. Internal Voltage Regulator disabled

$$P_{INT} = I_{DD} \cdot V_{DD} + I_{DDPLL} \cdot V_{DDPLL} + I_{DDA} \cdot V_{DDA}$$

$$P_{IO} = \sum_i R_{DS(on)} \cdot I_{IO_i}^2$$

$P_{IO}$  is the sum of all output currents on I/O ports associated with VDDX and VDDR.

For  $R_{DS(on)}$  is valid:

$$R_{DS(on)} = \frac{V_{OL}}{I_{OL}}; \text{for outputs driven low}$$

respectively

$$R_{DS(on)} = \frac{V_{DD5} - V_{OH}}{I_{OH}}; \text{for outputs driven high}$$

2. Internal voltage regulator enabled

$$P_{INT} = I_{DDR} \cdot V_{DDR} + I_{DDA} \cdot V_{DDA}$$

$I_{DDR}$  is the current shown in **Table A-7** and not the overall current flowing into VDDR, which additionally contains the current flowing into the external loads with output high.

$$P_{IO} = \sum_i R_{DS(on)} \cdot I_{IO_i}^2$$

$P_{IO}$  is the sum of all output currents on I/O ports associated with VDDX and VDDR.

Table A-6 5V I/O Characteristics

Conditions are shown in Table A-4 unless otherwise noted							
Num	C	Rating	Symbol	Min	Typ	Max	Unit
1	P	Input High Voltage	$V_{IH}$	$0.65 \cdot V_{DD5}$	-	-	V
	T	Input High Voltage	$V_{IH}$	-	-	$V_{DD5} + 0.3$	V
2	P	Input Low Voltage	$V_{IL}$	-	-	$0.35 \cdot V_{DD5}$	V
	T	Input Low Voltage	$V_{IL}$	$V_{SS5} - 0.3$	-	-	V
3	C	Input Hysteresis	$V_{HYS}$		250		mV
4	P	Input Leakage Current (pins in high impedance input mode) <sup>1</sup> $V_{in} = V_{DD5}$ or $V_{SS5}$	$I_{in}$	-2.5	-	2.5	$\mu A$
5	P	Output High Voltage (pins in output mode) Partial Drive $I_{OH} = -2mA$ Full Drive $I_{OH} = -10mA$	$V_{OH}$	$V_{DD5} - 0.8$	-	-	V
6	P	Output Low Voltage (pins in output mode) Partial Drive $I_{OL} = +2mA$ Full Drive $I_{OL} = +10mA$	$V_{OL}$	-	-	0.8	V
7	P	Internal Pull Up Device Current, tested at $V_{IL}$ Max.	$I_{PUL}$	-	-	-130	$\mu A$
8	P	Internal Pull Up Device Current, tested at $V_{IH}$ Min.	$I_{PUH}$	-10	-	-	$\mu A$
9	P	Internal Pull Down Device Current, tested at $V_{IH}$ Min.	$I_{PDH}$	-	-	130	$\mu A$
10	P	Internal Pull Down Device Current, tested at $V_{IL}$ Max.	$I_{PDL}$	10	-	-	$\mu A$
11	D	Input Capacitance	$C_{in}$		6	-	pF
12	T	Injection current <sup>2</sup> Single Pin limit Total Device Limit. Sum of all injected currents	$I_{ICS}$ $I_{ICP}$	-2.5 -25	-	2.5 25	mA
13	P	Port H, J, P Interrupt Input Pulse filtered <sup>3</sup>	$t_{PULSE}$			3	$\mu s$
14	P	Port H, J, P Interrupt Input Pulse passed <sup>3</sup>	$t_{PULSE}$	10			$\mu s$

NOTES:

1. Maximum leakage current occurs at maximum operating temperature. Current decreases by approximately one-half for each 8 C to 12 C in the temperature range from 50 C to 125 C.
2. Refer to **Section A.1.4 Current Injection**, for more details
3. Parameter only applies in STOP or Pseudo STOP mode.

## A.2 ATD Characteristics

This section describes the characteristics of the analog to digital converter.

### A.2.1 ATD Operating Characteristics

The **Table A-8** shows conditions under which the ATD operates.

The following constraints exist to obtain full-scale, full range results:

$V_{SSA} \leq V_{RL} \leq V_{IN} \leq V_{RH} \leq V_{DDA}$ . This constraint exists since the sample buffer amplifier can not drive beyond the power supply levels that it ties to. If the input level goes outside of this range it will effectively be clipped.

**Table A-8 ATD Operating Characteristics**

Conditions are shown in <b>Table A-4</b> unless otherwise noted							
Num	C	Rating	Symbol	Min	Typ	Max	Unit
1	D	Reference Potential Low High	$V_{RL}$ $V_{RH}$	$V_{SSA}$ $V_{DDA}/2$		$V_{DDA}/2$ $V_{DDA}$	V V
2	C	Differential Reference Voltage <sup>1</sup>	$V_{RH}-V_{RL}$	4.50	5.00	5.25	V
3	D	ATD Clock Frequency	$f_{ATDCLK}$	0.5		2.0	MHz
4	D	ATD 10-Bit Conversion Period Clock Cycles <sup>2</sup> Conv, Time at 2.0MHz ATD Clock $f_{ATDCLK}$	$N_{CONV10}$ $T_{CONV10}$	14 7		28 14	Cycles $\mu s$
5	D	ATD 8-Bit Conversion Period Clock Cycles <sup>2</sup> Conv, Time at 2.0MHz ATD Clock $f_{ATDCLK}$	$N_{CONV8}$ $T_{CONV8}$	12 6		26 13	Cycles $\mu s$
6	D	Recovery Time ( $V_{DDA}=5.0$ Volts)	$t_{REC}$			20	$\mu s$
7	P	Reference Supply current 2 ATD blocks on	$I_{REF}$			0.750	mA
8	P	Reference Supply current 1 ATD block on	$I_{REF}$			0.375	mA

**NOTES:**

1. Full accuracy is not guaranteed when differential voltage is less than 4.50V
2. The minimum time assumes a final sample period of 2 ATD clocks cycles while the maximum time assumes a final sample period of 16 ATD clocks.

### A.2.2 Factors influencing accuracy

Three factors - source resistance, source capacitance and current injection - have an influence on the accuracy of the ATD.

#### A.2.2.1 Source Resistance:

Due to the input pin leakage current as specified in **Table A-6** in conjunction with the source resistance there will be a voltage drop from the signal source to the ATD input. The maximum source resistance  $R_S$



The loop bandwidth  $f_C$  should be chosen to fulfill the Gardner's stability criteria by at least a factor of 10, typical values are 50.  $\zeta = 0.9$  ensures a good transient response.

$$f_C < \frac{2 \cdot \zeta \cdot f_{\text{ref}}}{\pi \cdot \left( \zeta + \sqrt{1 + \zeta^2} \right)} \cdot \frac{1}{50} \rightarrow f_C < \frac{f_{\text{ref}}}{4 \cdot 50}; (\zeta = 0.9)$$

And finally the frequency relationship is defined as

$$n = \frac{f_{\text{VCO}}}{f_{\text{ref}}} = 2 \cdot (\text{synr} + 1)$$

With the above inputs the resistance can be calculated as:

$$R = \frac{2 \cdot \pi \cdot n \cdot f_C}{K_\Phi}$$

The capacitance  $C_s$  can now be calculated as:

$$C_s = \frac{2 \cdot \zeta^2}{\pi \cdot f_C \cdot R} \approx \frac{0.516}{f_C \cdot R}; (\zeta = 0.9)$$

The capacitance  $C_p$  should be chosen in the range of:

$$C_s/20 \leq C_p \leq C_s/10$$

The stabilization delays shown in **Table A-16** are dependant on PLL operational settings and external component selection (e.g. crystal, XFC filter).

### A.5.3.2 Jitter Information

The basic functionality of the PLL is shown in **Figure A-2**. With each transition of the clock  $f_{\text{cmp}}$ , the deviation from the reference clock  $f_{\text{ref}}$  is measured and input voltage to the VCO is adjusted accordingly. The adjustment is done continuously with no abrupt changes in the clock output frequency. Noise, voltage, temperature and other factors cause slight variations in the control loop resulting in a clock jitter. This jitter affects the real minimum and maximum clock periods as illustrated in **Figure A-3**.

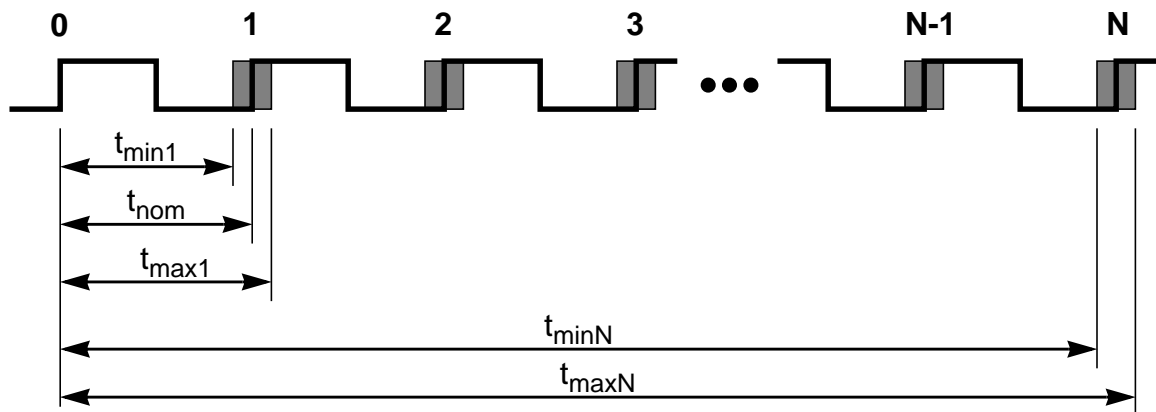


Figure A-3 Jitter Definitions

The relative deviation of  $t_{nom}$  is at its maximum for one clock period, and decreases towards zero for larger number of clock periods (N).

Defining the jitter as:

$$J(N) = \max\left(\left|1 - \frac{t_{max}(N)}{N \cdot t_{nom}}\right|, \left|1 - \frac{t_{min}(N)}{N \cdot t_{nom}}\right|\right)$$

For  $N < 100$ , the following equation is a good fit for the maximum jitter:

$$J(N) = \frac{j_1}{\sqrt{N}} + j_2$$

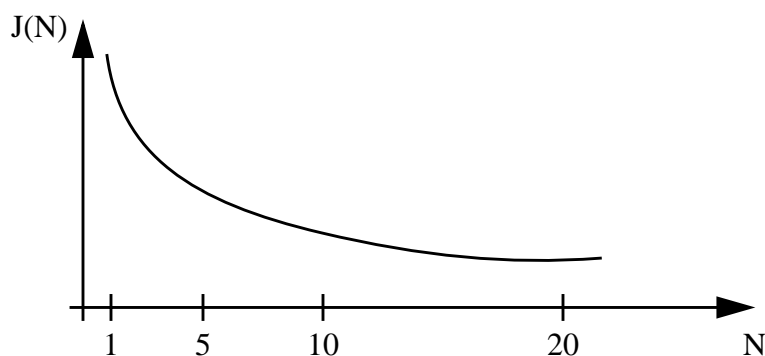


Figure A-4 Maximum bus clock jitter approximation

## A.6 MSCAN

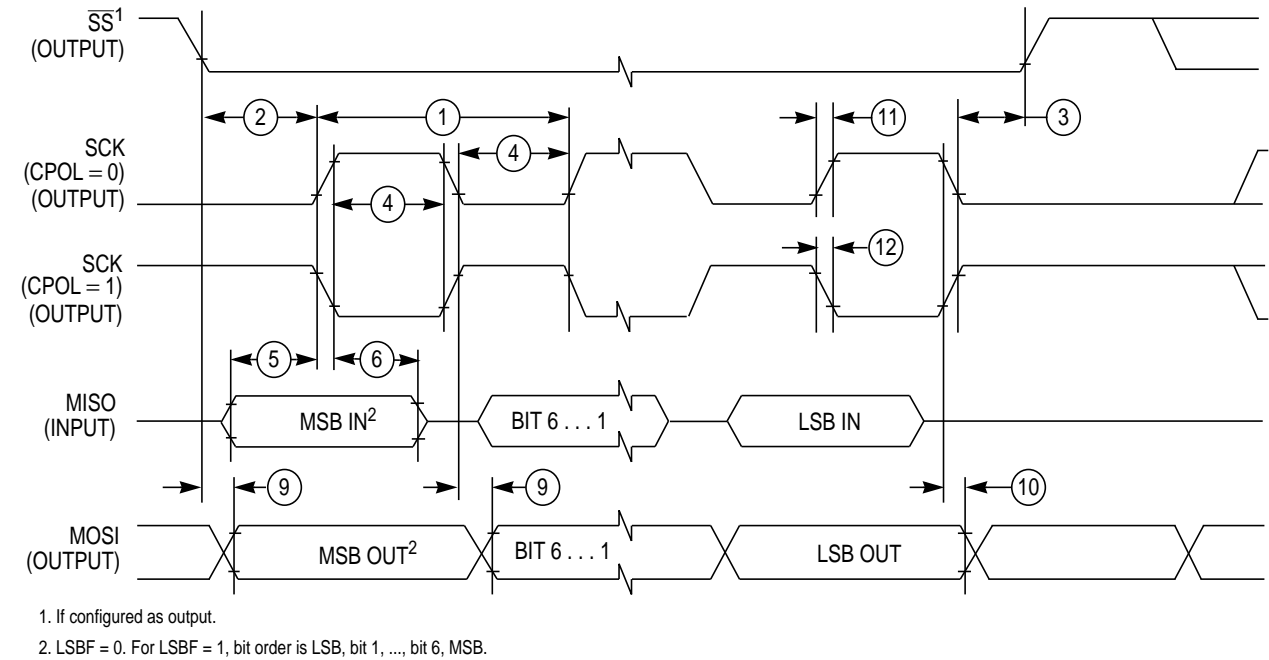
**Table A-17 MSCAN Wake-up Pulse Characteristics**

Conditions are shown in <b>Table A-4</b> unless otherwise noted							
Num	C	Rating	Symbol	Min	Typ	Max	Unit
1	P	MSCAN Wake-up dominant pulse filtered	$t_{WUP}$			2	$\mu s$
2	P	MSCAN Wake-up dominant pulse pass	$t_{WUP}$	5			$\mu s$

# A.7 SPI

## A.7.1 Master Mode

**Figure A-5** and **Figure A-6** illustrate the master mode timing. Timing values are shown in **Table A-18**.



**Figure A-5 SPI Master Timing (CPHA = 0)**

## A.8 External Bus Timing

A timing diagram of the external multiplexed-bus is illustrated in **Figure A-9** with the actual timing values shown on table **Table A-20**. All major bus signals are included in the diagram. While both a data write and data read cycle are shown, only one or the other would occur on a particular bus cycle.

### A.8.1 General Muxed Bus Timing

The expanded bus timings are highly dependent on the load conditions. The timing parameters shown assume a balanced load across all outputs.