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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HC08
Core Size	8-Bit
Speed	8MHz
Connectivity	I²C, IRSCI, SPI
Peripherals	LCD, LVD, POR, PWM
Number of I/O	40
Program Memory Size	24KB (24K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 6x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-QFP
Supplier Device Package	80-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc68hc908lk24cfq

Section 2. Memory Map

Section 3. Random-Access Memory (RAM)

Section 4. FLASH Memory (FLASH)

Section 5. Configuration Registers (CONFIG)

Section 19. External Interrupt (IRQ)

Section 20. Keyboard Interrupt Module (KBI)

Section 1. General Description

1.1 Contents

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$FE09	Reserved	Read: Write:	R	R	R	R	R	R	R	R
		Reset:								
$FE0A	Reserved	Read: Write:	R	R	R	R	R	R	R	R
		Reset:								
$FE0B	Reserved	Read: Write:	R	R	R	R	R	R	R	R
		Reset:								
$FE0C	Break Address Register High (BRKH)	Read: Write:	Bit 15	14	13	12	11	10	9	Bit 8
		Reset:	0	0	0	0	0	0	0	0
$FE0D	Break Address Register Low (BRKL)	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
		Reset:	0	0	0	0	0	0	0	0
$FE0E	Break Status and Control Register (BRKSCR)	Read: Write:	BRKE	BRKA	0	0	0	0	0	0
		Reset:	0	0	0	0	0	0	0	0
$FE0F	Low-Voltage Inhibit Status Register (LVISR)	Read: Write:	LVIOUT	LVIIE	LVIIF	0 LVIIACK	0	0	0	0
		Reset:	0	0	0	0	0	0	0	0
$FFCF	FLASH Block Protect Register (FLBPR)#	Read: Write:	BPR7	BPR6	BPR5	BPR4	BPR3	BPR2	BPR1	BPR0
		Reset:	Unaffected by reset; $FF when blank							

Non-volatile FLASH register; write by programming.

$FFFF	COP Control Register (COPCTL)	Read:	Low byte of reset vector
		Write:	Writing clears COP counter (any value)
		Reset:	Unaffected by reset

U = Unaffected X = Indeterminate = Unimplemented R = Reserved

Figure 2-2. Control, Status, and Data Registers (Sheet 13 of 13)

4.8.1 FLASH Block Protect Register

The FLASH block protect register (FLBPR) is implemented as a byte within the FLASH memory, and therefore can only be written during a programming sequence of the FLASH memory. The value in this register determines the starting location of the protected range within the FLASH memory.

Address: $FFCF

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	BPR7	BPR6	BPR5	BPR4	BPR3	BPR2	BPR1	BPR0
Reset:	Unaffected by reset; $FF when blank							

Non-volatile FLASH register; write by programming.

Figure 4-4. FLASH Block Protect Register (FLBPR)

BPR[7:0] — FLASH Block Protect Bits

BPR[7:0] represent bits [14:7] of a 16-bit memory address. Bits [15:14] are logic 1’s and bits [6:0] are logic 0’s.

16-bit memory address

Start address of FLASH block protect	1								0	0	0	0	0	0	0
		BPR[7:0]													

The resultant 16-bit address is used for specifying the start address of the FLASH memory for block protection. The FLASH is protected from this start address to the end of FLASH memory, at $FFFF. With this mechanism, the protect start address can be $XX00 or $XX80 (at page boundaries — 128 bytes) within the FLASH memory.

Examples of protect start address is shown in **Table 4-1**:

5.4 Configuration Register 1 (CONFIG1)

The CONFIG1 register can be written once after each reset.

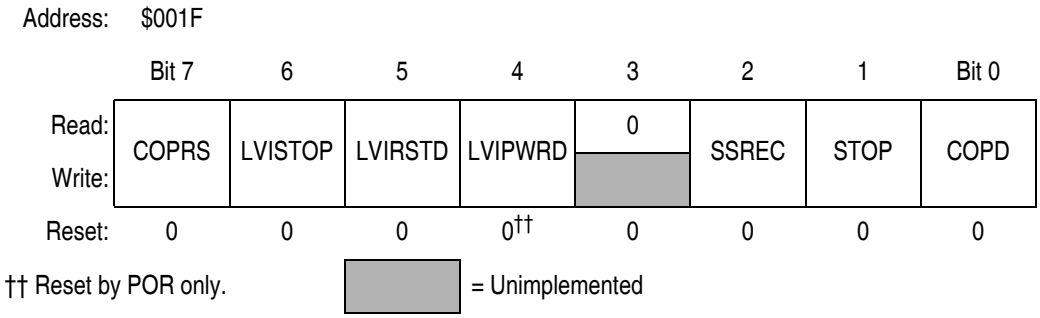

Figure 5-2. Configuration Register 1 (CONFIG1)

COPRS — COP Rate Select

COPRS selects the COP time-out period. Reset clears COPRS. (See **Section 21. Computer Operating Properly (COP)**.)

1 = COP time out period = $2^{13} – 2^4$ ICLK cycles
0 = COP time out period = $2^{18} – 2^4$ ICLK cycles

LVISTOP — LVI Enable in Stop Mode

When the LVIPWRD bit is clear, setting the LVISTOP bit enables the LVI to operate during stop mode. Reset clears LVISTOP. (See **Section 22. Low-Voltage Inhibit (LVI)**.)

1 = LVI enabled during stop mode
0 = LVI disabled during stop mode

LVIRSTD — LVI Reset Disable

LVIRSTD disables the reset signal from the LVI module. (See **Section 22. Low-Voltage Inhibit (LVI)**.)

1 = LVI module resets disabled
0 = LVI module resets enabled

LVIPWRD — LVI Power Disable Bit

LVIPWRD disables the LVI module. (See **Section 22. Low-Voltage Inhibit (LVI)**.)

1 = LVI module power disabled
0 = LVI module power enabled

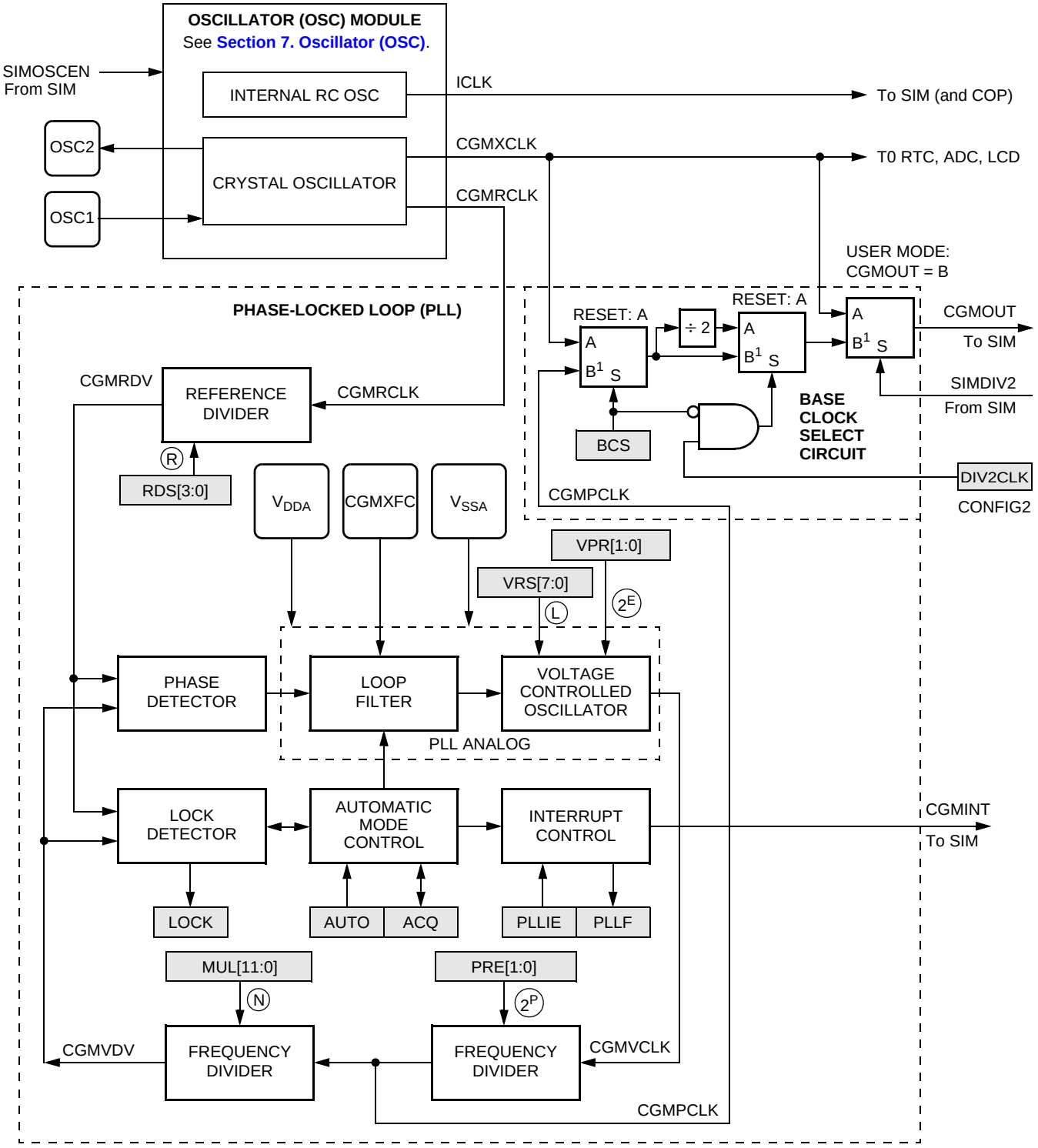

Figure 8-1. CGM Block Diagram

12.4 I/O Pins

Two RTC clock calibration pins are shared with standard port I/O pins.

Table 12-1. Pin Name Conventions

RTC Generic Pin Name	Full MCU Pin Name	Pin Selected for RTC Function by Bits in RTCCOMR ($0040)
CALIN	PTD0/$\overline{SS}$/CALIN	AUTOCAL
CALOUT	PTD3/SPSCK/CALOUT(1)	OUTF[1:0}

Notes:
1. Do not enable the SPI function if the pin is used for RTC calibration.

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$0040	RTC Calibration Control Register (RTCCOMR)	Read:	0	0	CAL	AUTOCAL	OUTF1	OUTF0	0	0
		Write:	R	R					RTCWE1	RTCWE0
		Reset:	0	0	0	0	0	0	0	0
$0041	RTC Calibration Data Register (RTCCDAT)	Read:	EOVL	0	E5	E4	E3	E2	E1	E0
		Write:								
		Reset:	U	0	U	U	U	U	U	U
$0042	RTC Control Register 1 (RTCCR1)	Read:	ALMIE	CHRIE	DAYIE	HRIE	MINIE	SECIE	TB1IE	TB2IE
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$0043	RTC Control Register 2 (RTCCR2)	Read:	COMEN	0	CHRE	RTCE	TBH	0	0	0
		Write:		CHRCLR						
		Reset:	U	0	0	0††	0	0	0	0
$0044	RTC Status Register (RTCSR)	Read:	ALMF	CHRF	DAYF	HRF	MINF	SECF	TB1F	TB2F
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$0045	Alarm Minute Register (ALMR)	Read:	0	0	AM5	AM4	AM3	AM2	AM1	AM0
		Write:								
		Reset:	0	0	U	U	U	U	U	U

†† Reset by POR only.

U = Unaffected = Unimplemented R = Reserved

Figure 12-1. RTC I/O Register Summary

12.5 Functional Description

The RTC module provides clock indications in seconds, minutes, and hours; calendar indications in day-of-week, day-of-month, month, and year; with automatic adjustment for month and leap year. Reading the clock and calendar registers return the current time and date. Writing to these registers set the time and date, and the counters will continue to count from the new settings.

The alarm interrupt is set for the hour and minute. When the hour and minute counters matches the time set in the alarm hour and minute registers, the alarm flag is set. The alarm can be configured to generate a CPU interrupt request.

A 1/100 seconds chronograph counter is provided for timing applications. This counter can be independently enabled or disabled, and cleared at any time.

RTC module interrupts include the alarm interrupt and seven periodic interrupts from the clock and chronograph counters.

A frequency compensation mechanism is built into this RTC module to allow adjustments made to the RTC clock when a less accurate 32.768 kHz crystal is used.

The 1-Hz clock that drives the clock and calendar could make use of the built-in compensation mechanism for crystal frequency error compensation so that the 1-Hz clock could be made more accurate than the frequency accuracy of the crystal that drive the module. The compensation value can be provided by application software or acquire automatically during calibration operation of the module.

Figure 12-2 shows the structure of the RTC module.

The mechanism uses the RTCWE[1:0] bits in the RTC calibration control register (RTCCOMR) in a state machine, which requires a bit-write sequence to disable the write-protection. A block diagram of the state machine is shown in **Figure 12-5**.

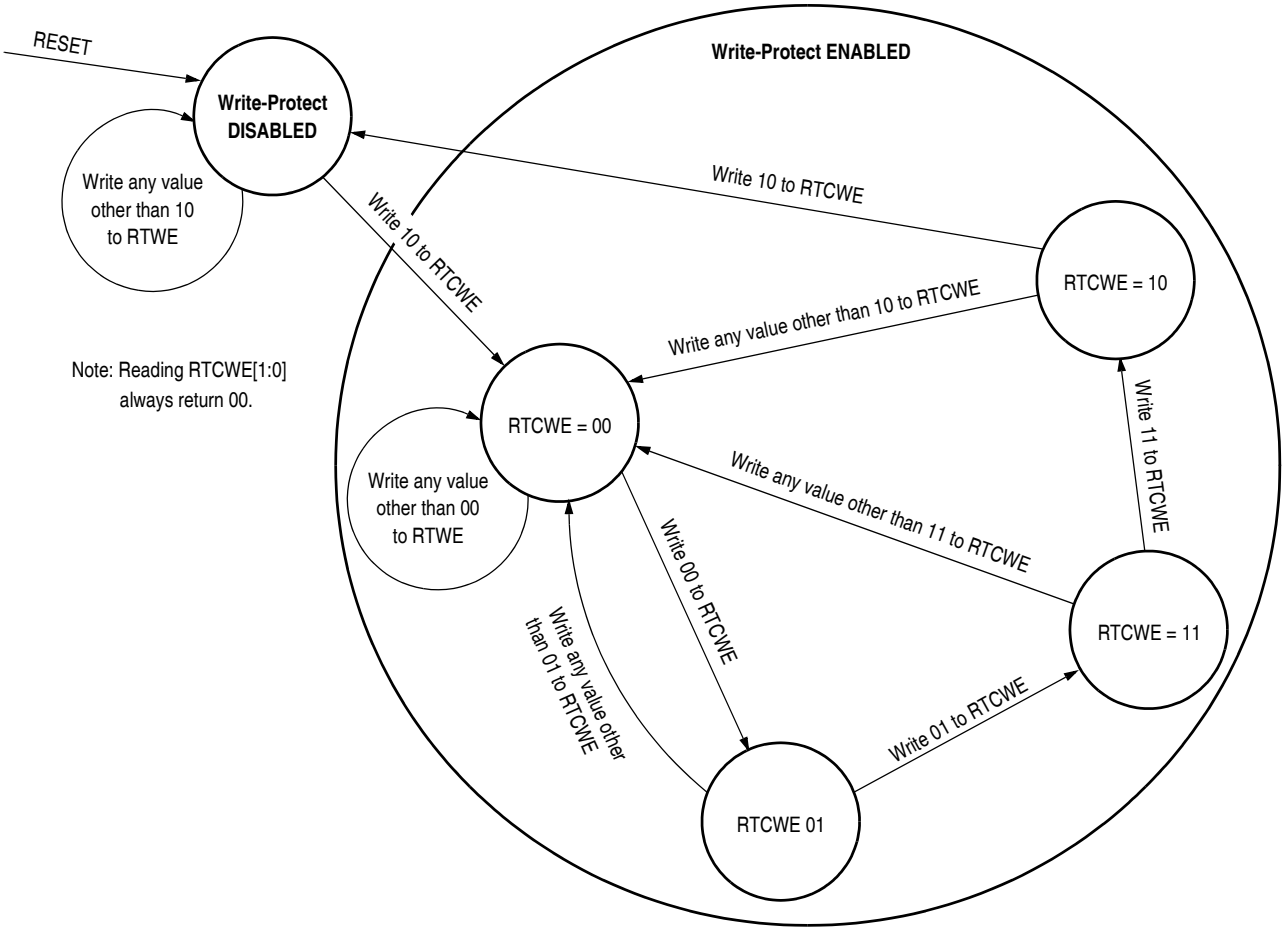

Figure 12-5. RTC Write Protect State Diagram

After a reset, the write-protect mechanism is disabled, allowing the user code to calibrate the RTC clock, set the time in the clock registers, and set the date in the calendar registers.

To enable write-protect after reset or write-protect is disabled execute the following code:

```
RTCWE1  EQU     1       ;RTCWE1 bit
RTCWE0  EQU     0       ;RTCWE0 bit
```

The maximum percent difference between the receiver count and the transmitter count of a fast 9-bit character with no errors is

$$\left|\frac{170 - 176}{170}\right| \times 100 = 3.53\%$$

13.7.3.6 Receiver Wakeup

So that the MCU can ignore transmissions intended only for other receivers in multiple-receiver systems, the receiver can be put into a standby state. Setting the receiver wakeup bit, RWU, in SCC2 puts the receiver into a standby state during which receiver interrupts are disabled.

Depending on the state of the WAKE bit in SCC1, either of two conditions on the RxD pin can bring the receiver out of the standby state:

- Address mark — An address mark is a logic 1 in the most significant bit position of a received character. When the WAKE bit is set, an address mark wakes the receiver from the standby state by clearing the RWU bit. The address mark also sets the SCI receiver full bit, SCRF. Software can then compare the character containing the address mark to the user-defined address of the receiver. If they are the same, the receiver remains awake and processes the characters that follow. If they are not the same, software can set the RWU bit and put the receiver back into the standby state.
- Idle input line condition — When the WAKE bit is clear, an idle character on the RxD pin wakes the receiver from the standby state by clearing the RWU bit. The idle character that wakes the receiver does not set the receiver idle bit, IDLE, or the SCI receiver full bit, SCRF. The idle line type bit, ILTY, determines whether the receiver begins counting logic 1s as idle character bits after the start bit or after the stop bit.

NOTE: *Clearing the WAKE bit after the RxD pin has been idle may cause the receiver to wake up immediately.*

13.11.6 SCI Data Register

The SCI data register is the buffer between the internal data bus and the receive and transmit shift registers. Reset has no effect on data in the SCI data register.

Address: $0018

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	R7	R6	R5	R4	R3	R2	R1	R0
Write:	T7	T6	T5	T4	T3	T2	T1	T0
Reset:	Unaffected by reset							

Figure 13-18. SCI Data Register (SCDR)

R7/T7–R0/T0 — Receive/Transmit Data Bits

Reading the SCDR accesses the read-only received data bits, R7–R0. Writing to the SCDR writes the data to be transmitted, T7–T0. Reset has no effect on the SCDR.

NOTE: *Do not use read/modify/write instructions on the SCI data register.*

16.5 Interrupts

When the AIEN bit is set, the ADC module is capable of generating a CPU interrupt after each ADC conversion. A CPU interrupt is generated if the COCO bit is at logic 0. The COCO bit is not used as a conversion complete flag when interrupts are enabled. The interrupt vector is defined in **Table 2-1 . Vector Addresses**.

16.6 Low-Power Modes

The STOP and WAIT instructions put the MCU in low power-consumption standby modes.

16.6.1 Wait Mode

The ADC continues normal operation in wait mode. Any enabled CPU interrupt request from the ADC can bring the MCU out of wait mode. If the ADC is not required to bring the MCU out of wait mode, power down the ADC by setting the ADCH[4:0] bits to logic 1's before executing the WAIT instruction.

16.6.2 Stop Mode

The ADC module is inactive after the execution of a STOP instruction. Any pending conversion is aborted. ADC conversions resume when the MCU exits stop mode. Allow one conversion cycle to stabilize the analog circuitry before attempting a new ADC conversion after exiting stop mode.

16.7 I/O Signals

The ADC module has ten channels, six channels are shared with port A and port B I/O pins; two channels are the ADC voltage reference inputs, V_{REFH} and V_{REFL}; one channel is the V_{LCD} input; and one channel is the 1.2V bandgap reference voltage.

In left justified mode the ADRH holds the eight most significant bits (MSBs), and the ADRL holds the two least significant bits (LSBs), of the 10-bit result. The ADRH and ADRL are updated each time a single channel ADC conversion completes. Reading ADRH latches the contents of ADRL. Until ADRL is read all subsequent ADC results will be lost. (See **Figure 16-7 . ADRH and ADRL in Left Justified Mode**.)

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$003D	ADC Data Register High (ADRH)	Read:	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2
		Write:	R	R	R	R	R	R	R	R
		Reset:	0	0	0	0	0	0	0	0
$003E	ADC Data Register Low (ADRL)	Read:	AD1	AD0	0	0	0	0	0	0
		Write:	R	R	R	R	R	R	R	R
		Reset:	0	0	0	0	0	0	0	0

Figure 16-7. ADRH and ADRL in Left Justified Mode

In left justified sign mode the ADRH holds the eight MSBs with the MSB complemented, and the ADRL holds the two least significant bits (LSBs), of the 10-bit result. The ADRH and ADRL are updated each time a single channel ADC conversion completes. Reading ADRH latches the contents of ADRL. Until ADRL is read all subsequent ADC results will be lost. (See **Figure 16-8 . ADRH and ADRL in Left Justified Sign Data Mode**.)

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$003D	ADC Data Register High (ADRH)	Read:	$\overline{AD9}$	AD8	AD7	AD6	AD5	AD4	AD3	AD2
		Write:	R	R	R	R	R	R	R	R
		Reset:	0	0	0	0	0	0	0	0
$003E	ADC Data Register Low (ADRL)	Read:	AD1	AD0	0	0	0	0	0	0
		Write:	R	R	R	R	R	R	R	R
		Reset:	0	0	0	0	0	0	0	0

Figure 16-8. ADRH and ADRL in Left Justified Sign Data Mode

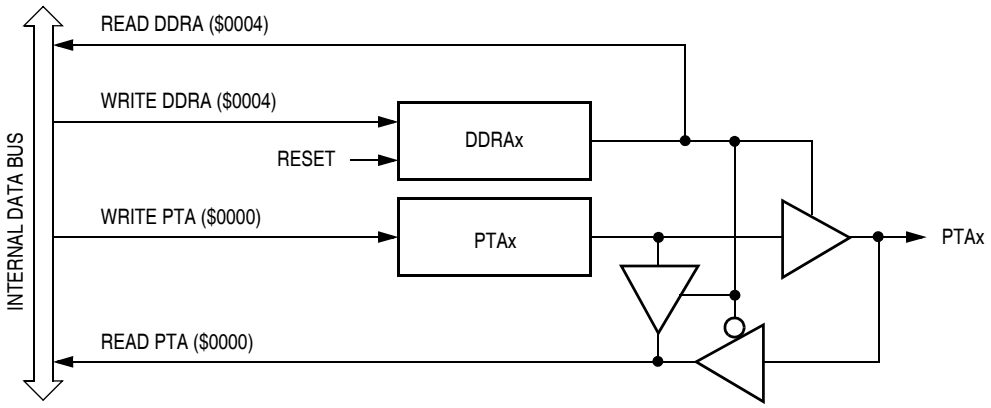

Figure 18-4. Port A I/O Circuit

When DDRAx is a logic 1, reading address $0000 reads the PTAx data latch. When DDRAx is a logic 0, reading address $0000 reads the voltage level on the pin. The data latch can always be written, regardless of the state of its data direction bit.

Table 18-2 summarizes the operation of the port A pins.

Table 18-2. Port A Pin Functions

DDRA Bit	PTA Bit	I/O Pin Mode	Accesses to DDRA	Accesses to PTA	
			Read/Write	Read	Write
0	X(1)	Input, Hi-Z(2)	DDRA[7:0]	Pin	PTA[7:0](3)
1	X	Output	DDRA[7:0]	PTA[7:0]	PTA[7:0]

Notes:
1. X = don't care.
2. Hi-Z = high impedance.
3. Writing affects data register, but does not affect input.

18.7.2 Data Direction Register E (DDRE)

Data direction register E determines whether each port E pin is an input or an output. Writing a logic 1 to a DDRE bit enables the output buffer for the corresponding port E pin; a logic 0 disables the output buffer.

Address: $0009

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	DDRE7	DDRE6	DDRE5	DDRE4	DDRE3	DDRE2	DDRE1	DDRE0
Reset:	0	0	0	0	0	0	0	0

Figure 18-17. Data Direction Register E (DDRE)

DDRE[7:0] — Data Direction Register E Bits

These read/write bits control port E data direction. Reset clears DDRE[7:0], configuring all port E pins as inputs.

1 = Corresponding port E pin configured as output
0 = Corresponding port E pin configured as input

NOTE: *Avoid glitches on port E pins by writing to the port E data register before changing data direction register E bits from 0 to 1.* ***Figure 18-18*** *shows the port E I/O logic.*

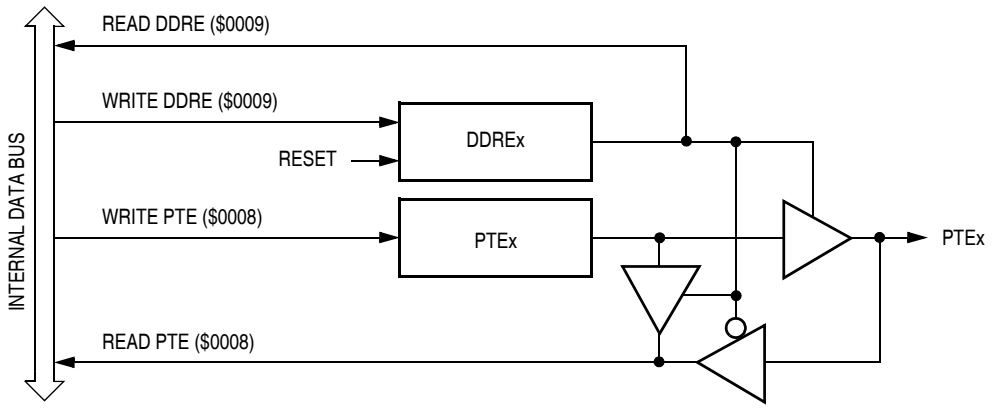

Figure 18-18. Port E I/O Circuit

Section 21. Computer Operating Properly (COP)

21.1 Contents

21.2 Introduction

The computer operating properly (COP) module contains a free-running counter that generates a reset if allowed to overflow. The COP module helps software recover from runaway code. Prevent a COP reset by clearing the COP counter periodically. The COP module can be disabled through the COPD bit in the configuration register 1 (CONFIG1).

21.5 COP Control Register

The COP control register is located at address $FFFF and overlaps the reset vector. Writing any value to $FFFF clears the COP counter and starts a new timeout period. Reading location $FFFF returns the low byte of the reset vector.

Address: $FFFF

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	Low byte of reset vector							
Write:	Clear COP counter							
Reset:	Unaffected by reset							

Figure 21-3. COP Control Register (COPCTL)

21.6 Interrupts

The COP does not generate CPU interrupt requests.

21.7 Monitor Mode

When monitor mode is entered with V_{TST} on the $\overline{IRQ}$ pin, the COP is disabled as long as V_{TST} remains on the $\overline{IRQ}$ pin or the $\overline{RST}$ pin. When monitor mode is entered by having blank reset vectors and not having V_{TST} on the $\overline{IRQ}$ pin, the COP is automatically disabled until a POR occurs.

21.8 Low-Power Modes

The WAIT and STOP instructions put the MCU in low power-consumption standby modes.

23.5.2 Stop Mode

A break interrupt causes exit from stop mode and sets the SBSW bit in the break status register.

23.6 Break Module Registers

These registers control and monitor operation of the break module:

- Break status and control register (BRKSCR)
- Break address register high (BRKH)
- Break address register low (BRKL)
- SIM break status register (SBSR)
- SIM break flag control register (SBFCR)

23.6.1 Break Status and Control Register

The break status and control register (BRKSCR) contains break module enable and status bits.

Address: $FE0E

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	BRKE	BRKA	0	0	0	0	0	0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 23-3. Break Status and Control Register (BRKSCR)

BRKE — Break Enable Bit

This read/write bit enables breaks on break address register matches. Clear BRKE by writing a logic 0 to bit 7. Reset clears the BRKE bit.

1 = Breaks enabled on 16-bit address match
0 = Breaks disabled on 16-bit address match

Section 24. Electrical Specifications

24.1 Contents

24.2 Introduction

This section contains electrical and timing specifications.