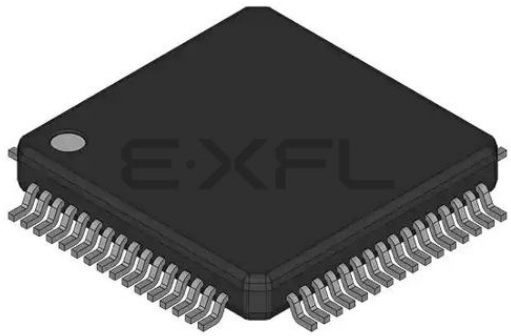

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	HC08
Core Size	8-Bit
Speed	8MHz
Connectivity	I²C, IRSCI, SPI
Peripherals	LCD, LVD, POR, PWM
Number of I/O	40
Program Memory Size	24KB (24K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 6x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-QFP
Supplier Device Package	64-QFP (14x14)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc68hc908lk24cfu

Section 14. Serial Peripheral Interface Module (SPI)

Section 25. Mechanical Specifications

Section 26. Ordering Information

Appendix A. MC68HC908LK24

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$0036	PLL Control Register (PTCL)	Read:	PLLIE	PLLF	PLLON	BCS	PRE1	PRE0	VPR1	VPR0
		Write:								
		Reset:	0	0	1	0	0	0	0	0
$0037	PLL Bandwidth Control Register (PBWC)	Read:	AUTO	LOCK	$\overline{ACQ}$	0	0	0	0	R
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$0038	PLL Multiplier Select Register High (PMSH)	Read:	0	0	0	0	MUL11	MUL10	MUL9	MUL8
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$0039	PLL Multiplier Select Register Low (PMSL)	Read:	MUL7	MUL6	MUL5	MUL4	MUL3	MUL2	MUL1	MUL0
		Write:								
		Reset:	0	1	0	0	0	0	0	0
$003A	PLL VCO Range Select Register (PMRS)	Read:	VRS7	VRS6	VRS5	VRS4	VRS3	VRS2	VRS1	VRS0
		Write:								
		Reset:	0	1	0	0	0	0	0	0
$003B	PLL Reference Divider Select Register (PMDS)	Read:	0	0	0	0	RDS3	RDS2	RDS1	RDS0
		Write:								
		Reset:	0	0	0	0	0	0	0	1

= Unimplemented R = Reserved

NOTES:
1. When AUTO = 0, PLLIE is forced clear and is read-only.
2. When AUTO = 0, PLLF and LOCK read as clear.
3. When AUTO = 1, $\overline{ACQ}$ is read-only.
4. When PLLON = 0 or VRS7:VRS0 = $0, BCS is forced clear and is read-only.
5. When PLLON = 1, the PLL programming register is read-only.
6. When BCS = 1, PLLON is forced set and is read-only.

Figure 8-2. CGM I/O Register Summary

8.5.6 CGM VCO Clock Output (CGMVCLK)

CGMVCLK is the clock output from the VCO.

8.5.7 CGM Base Clock Output (CGMOUT)

CGMOUT is the clock output of the CGM. This signal goes to the SIM, which generates the MCU clocks. CGMOUT is a 50 percent duty cycle clock running at twice the bus frequency. CGMOUT is software programmable to be equal to CGMXCLK, CGMXCLK divided by two, or CGMPCLK divided by two.

8.5.8 CGM CPU Interrupt (CGMINT)

CGMINT is the interrupt signal generated by the PLL lock detector.

8.6 CGM Registers

The following registers control and monitor operation of the CGM:

- PLL control register (PCTL)
  (See **8.6.1 PLL Control Register**.)
- PLL bandwidth control register (PBWC)
  (See **8.6.2 PLL Bandwidth Control Register**.)
- PLL multiplier select registers (PMSH and PMSL)
  (See **8.6.3 PLL Multiplier Select Registers**.)
- PLL VCO range select register (PMRS)
  (See **8.6.4 PLL VCO Range Select Register**.)
- PLL reference divider select register (PMDS)
  (See **8.6.5 PLL Reference Divider Select Register**.)

8.6.1 PLL Control Register

The PLL control register (PCTL) contains the interrupt enable and flag bits, the on/off switch, the base clock selector bit, the prescaler bits, and the VCO power-of-two range selector bits.

Address: $0036

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	PLLIE	PLLF	PLLON	BCS	PRE1	PRE0	VPR1	VPR0
Write:								
Reset:	0	0	1	0	0	0	0	0

= Unimplemented

Figure 8-4. PLL Control Register (PCTL)

PLLIE — PLL Interrupt Enable Bit

This read/write bit enables the PLL to generate an interrupt request when the LOCK bit toggles, setting the PLL flag, PLLF. When the AUTO bit in the PLL bandwidth control register (PBWC) is clear, PLLIE cannot be written and reads as logic 0. Reset clears the PLLIE bit.

1 = PLL interrupts enabled
0 = PLL interrupts disabled

PLLF — PLL Interrupt Flag Bit

This read-only bit is set whenever the LOCK bit toggles. PLLF generates an interrupt request if the PLLIE bit also is set. PLLF always reads as logic 0 when the AUTO bit in the PLL bandwidth control register (PBWC) is clear. Clear the PLLF bit by reading the PLL control register. Reset clears the PLLF bit.

1 = Change in lock condition
0 = No change in lock condition

NOTE: *Do not inadvertently clear the PLLF bit. Any read or read-modify-write operation on the PLL control register clears the PLLF bit.*

12.5 Functional Description

The RTC module provides clock indications in seconds, minutes, and hours; calendar indications in day-of-week, day-of-month, month, and year; with automatic adjustment for month and leap year. Reading the clock and calendar registers return the current time and date. Writing to these registers set the time and date, and the counters will continue to count from the new settings.

The alarm interrupt is set for the hour and minute. When the hour and minute counters matches the time set in the alarm hour and minute registers, the alarm flag is set. The alarm can be configured to generate a CPU interrupt request.

A 1/100 seconds chronograph counter is provided for timing applications. This counter can be independently enabled or disabled, and cleared at any time.

RTC module interrupts include the alarm interrupt and seven periodic interrupts from the clock and chronograph counters.

A frequency compensation mechanism is built into this RTC module to allow adjustments made to the RTC clock when a less accurate 32.768 kHz crystal is used.

The 1-Hz clock that drives the clock and calendar could make use of the built-in compensation mechanism for crystal frequency error compensation so that the 1-Hz clock could be made more accurate than the frequency accuracy of the crystal that drive the module. The compensation value can be provided by application software or acquire automatically during calibration operation of the module.

Figure 12-2 shows the structure of the RTC module.

12.10.3 RTC Control Register 1 (RTCCR1)

The RTC control register 1 (RTCCR1) contains the eight interrupt enable bits for RTC interrupt functions.

Address: $0042

Read: Write:	ALMIE	CHRIE	DAYIE	HRIE	MINIE	SECIE	TB1IE	TB2IE
Reset:	0	0	0	0	0	0	0	0

Figure 12-8. RTC Control Register 1 (RTCCR1)

ALMIE — Alarm Interrupt Enable

This read/write bit enables the alarm flag, ALMF, to generate CPU interrupt requests. Reset clears the ALMIE bit.

1 = ALMF enabled to generate CPU interrupt
0 = ALMF not enabled to generate CPU interrupt

CHRIE — Chronograph Interrupt Enable

This read/write bit enables the chronograph flag, CHRF, to generate CPU interrupt requests. Reset clears the CHRIE bit.

1 = CHRF enabled to generate CPU interrupt
0 = CHRF not enabled to generate CPU interrupt

DAYIE — Day Interrupt Enable

This read/write bit enables the day flag, DAYF, to generate CPU interrupt requests. Reset clears the DAYIE bit.

1 = DAYF enabled to generate CPU interrupt
0 = DAYF not enabled to generate CPU interrupt

HRIE — Hour Interrupt Enable

This read/write bit enables the hour flag, HRF, to generate CPU interrupt requests. Reset clears the HRIE bit.

1 = HRF enabled to generate CPU interrupt
0 = HRF not enabled to generate CPU interrupt

MINIE — Minute Interrupt Enable

This read/write bit enables the minute flag, MINF, to generate CPU interrupt requests. Reset clears the MINIE bit.

1 = MINF enabled to generate CPU interrupt
0 = MINF not enabled to generate CPU interrupt

13.7.2 Transmitter

Figure 13-7 shows the structure of the SCI transmitter.

The baud rate clock source for the SCI can be selected by the CKS bit, in the SCI baud rate register (see 13.11.7 SCI Baud Rate Register).

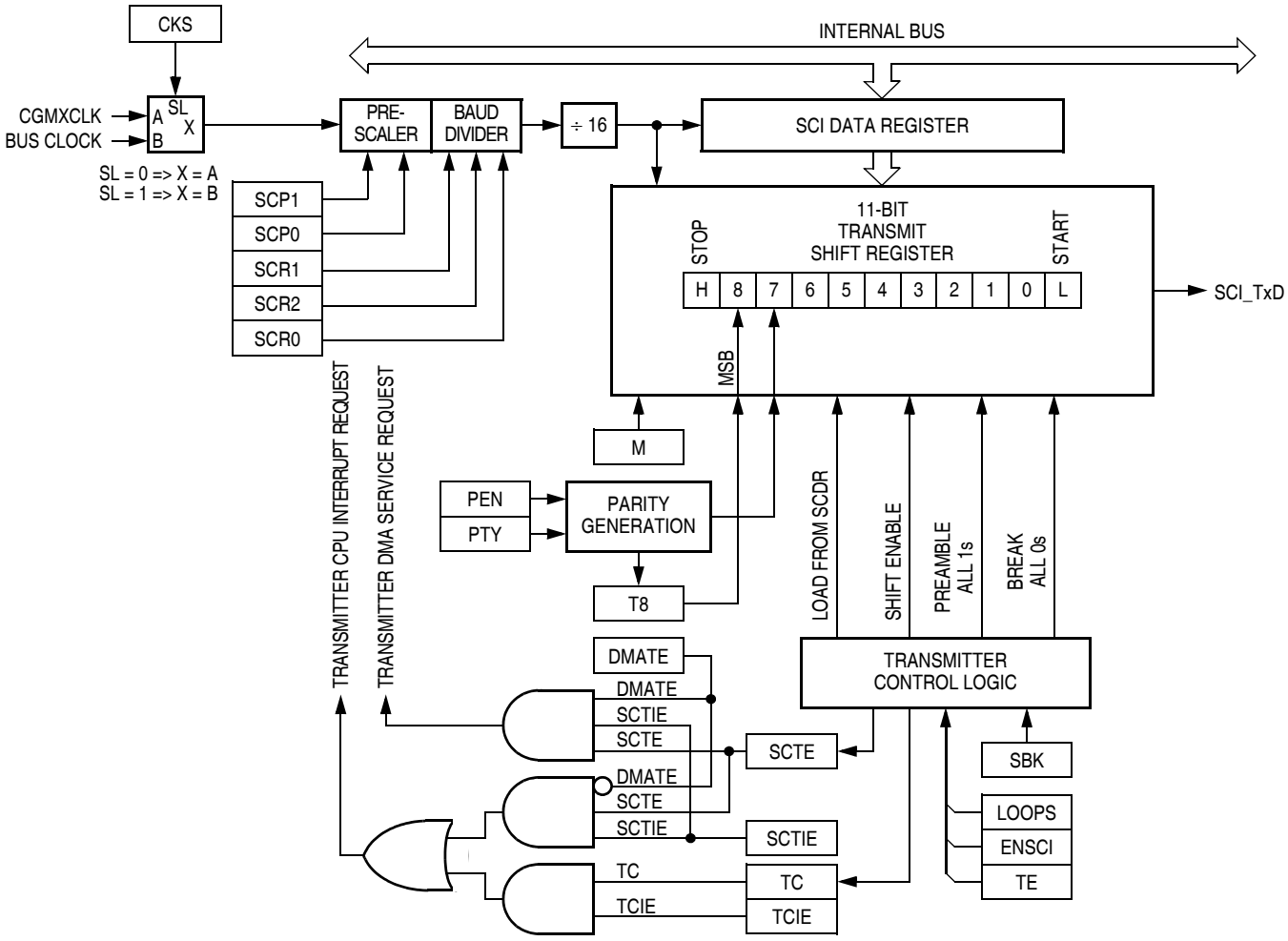

Figure 13-7. SCI Transmitter

The maximum percent difference between the receiver count and the transmitter count of a fast 9-bit character with no errors is

$$\left|\frac{170 - 176}{170}\right| \times 100 = 3.53\%$$

13.7.3.6 Receiver Wakeup

So that the MCU can ignore transmissions intended only for other receivers in multiple-receiver systems, the receiver can be put into a standby state. Setting the receiver wakeup bit, RWU, in SCC2 puts the receiver into a standby state during which receiver interrupts are disabled.

Depending on the state of the WAKE bit in SCC1, either of two conditions on the RxD pin can bring the receiver out of the standby state:

- Address mark — An address mark is a logic 1 in the most significant bit position of a received character. When the WAKE bit is set, an address mark wakes the receiver from the standby state by clearing the RWU bit. The address mark also sets the SCI receiver full bit, SCRF. Software can then compare the character containing the address mark to the user-defined address of the receiver. If they are the same, the receiver remains awake and processes the characters that follow. If they are not the same, software can set the RWU bit and put the receiver back into the standby state.
- Idle input line condition — When the WAKE bit is clear, an idle character on the RxD pin wakes the receiver from the standby state by clearing the RWU bit. The idle character that wakes the receiver does not set the receiver idle bit, IDLE, or the SCI receiver full bit, SCRF. The idle line type bit, ILTY, determines whether the receiver begins counting logic 1s as idle character bits after the start bit or after the stop bit.

NOTE: *Clearing the WAKE bit after the RxD pin has been idle may cause the receiver to wake up immediately.*

Table 13-5 shows a summary of I/O pin functions when the SCI is enabled.

Table 13-5. SCI Pin Functions (Standard and Infrared)

SCC1 [ENSCI]	SCIRCR [IREN]	SCC2 [TE]	SCC2 [RE]	TxD Pin	RxD Pin
1	0	0	0	Hi-Z(1)	Input ignored (terminate externally)
1	0	0	1	Hi-Z(1)	Input sampled, pin should idle high
1	0	1	0	Output SCI (idle high)	Input ignored (terminate externally)
1	0	1	1	Output SCI (idle high)	Input sampled, pin should idle high
1	1	0	0	Hi-Z(1)	Input ignored (terminate externally)
1	1	0	1	Hi-Z(1)	Input sampled, pin should idle high
1	1	1	0	Output IR SCI (idle high)	Input ignored (terminate externally)
1	1	1	1	Output IR SCI (idle high)	Input sampled, pin should idle high
0	X	X	X	Pins under port control (standard I/O port)	

Notes:
1. After completion of transmission in progress.

13.11 I/O Registers

The following I/O registers control and monitor SCI operation:

- SCI control register 1 (SCC1)
- SCI control register 2 (SCC2)
- SCI control register 3 (SCC3)
- SCI status register 1 (SCS1)
- SCI status register 2 (SCS2)
- SCI data register (SCDR)
- SCI baud rate register (SCBR)
- SCI infrared control register (SCIRCR)

When the master SPI starts a transmission, the data in the slave shift register begins shifting out on the MISO pin. The slave can load its shift register with a new byte for the next transmission by writing to its transmit data register. The slave must write to its transmit data register at least one bus cycle before the master starts the next transmission. Otherwise, the byte already in the slave shift register shifts out on the MISO pin. Data written to the slave shift register during a transmission remains in a buffer until the end of the transmission.

When the clock phase bit (CPHA) is set, the first edge of SPSCK starts a transmission. When CPHA is clear, the falling edge of $\overline{SS}$ starts a transmission. (See **14.6 Transmission Formats**.)

NOTE: *SPSCK must be in the proper idle state before the slave is enabled to prevent SPSCK from appearing as a clock edge.*

14.6 Transmission Formats

During an SPI transmission, data is simultaneously transmitted (shifted out serially) and received (shifted in serially). A serial clock synchronizes shifting and sampling on the two serial data lines. A slave select line allows selection of an individual slave SPI device; slave devices that are not selected do not interfere with SPI bus activities. On a master SPI device, the slave select line can optionally be used to indicate multiple-master bus contention.

14.6.1 Clock Phase and Polarity Controls

Software can select any of four combinations of serial clock (SPSCK) phase and polarity using two bits in the SPI control register (SPCR). The clock polarity is specified by the CPOL control bit, which selects an active high or low clock and has no significant effect on the transmission format.

14.14.2 SPI Status and Control Register

The SPI status and control register contains flags to signal these conditions:

- Receive data register full
- Failure to clear SPRF bit before next byte is received (overflow error)
- Inconsistent logic level on $\overline{SS}$ pin (mode fault error)
- Transmit data register empty

The SPI status and control register also contains bits that perform these functions:

- Enable error interrupts
- Enable mode fault error detection
- Select master SPI baud rate

Address: $0011

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	SPRF	ERRIE	OVRF	MODF	SPTE	MODFEN	SPR1	SPR0
Write:								
Reset:	0	0	0	0	1	0	0	0

= Unimplemented

Figure 14-14. SPI Status and Control Register (SPSCR)

SPRF — SPI Receiver Full Bit

This clearable, read-only flag is set each time a byte transfers from the shift register to the receive data register. SPRF generates a CPU interrupt request if the SPRIE bit in the SPI control register is set also.

During an SPRF CPU interrupt, the CPU clears SPRF by reading the SPI status and control register with SPRF set and then reading the SPI data register. Reset clears the SPRF bit.

1 = Receive data register full
0 = Receive data register not full

MMTXIF — Multi-Master Transmit Interrupt Flag

This flag is set when data in the data transmit register (MMDTR) is downloaded to the output circuit, and that new data can be written to the MMDTR. MMTXIF generates an interrupt request to CPU if the MMIEN bit in MMCR is also set. This bit is cleared by writing "0" to it or when the MMEN = 0.

1 = Data transfer completed
0 = Data transfer in progress

MMATCH — Multi-Master Address Match

This flag is set when the received data in the data receive register (MMDRR) is an calling address which matches with the address or its extended addresses (MMEXTAD=1) specified in the MMADR register.

1 = Received address matches MMADR
0 = Received address does not match

MMSRW — Multi-Master Slave Read/Write

This bit indicates the data direction when the module is in slave mode. It is updated after the calling address is received from a master device. MMSRW = 1 when the calling master is reading data from the module (slave transmit mode). MMSRW = 0 when the master is writing data to the module (receive mode).

1 = Slave mode transmit
0 = Slave mode receive

MMRXAK — Multi-Master Receive Acknowledge

When this bit is cleared, it indicates an acknowledge signal has been received after the completion of 8 data bits transmission on the bus. When MMRXAK is set, it indicates no acknowledge signal has been detected at the 9th clock; the module will release the SDA line for the master to generate "stop" or "repeated start" condition. Reset sets this bit.

1 = No acknowledge signal received at 9th clock bit
0 = Acknowledge signal received at 9th clock bit

16.8.3 ADC Clock Control Register

The ADC clock control register (ADCLK) selects the clock frequency for the ADC.

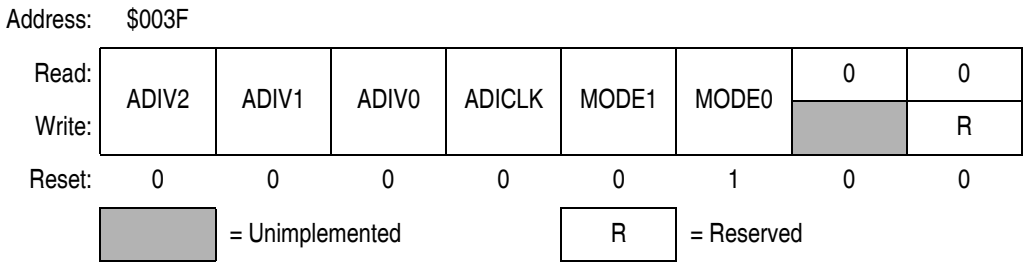

Figure 16-9. ADC Clock Control Register (ADCLK)

ADIV[2:0] — ADC Clock Prescaler Bits

ADIV2, ADIV1, and ADIV0 form a 3-bit field which selects the divide ratio used by the ADC to generate the internal ADC clock. Table 16-2 shows the available clock configurations. The ADC clock should be set to between 32kHz and 2MHz.

Table 16-2. ADC Clock Divide Ratio

ADIV2	ADIV1	ADIV0	ADC Clock Rate
0	0	0	ADC input clock ÷ 1
0	0	1	ADC input clock ÷ 2
0	1	0	ADC input clock ÷ 4
0	1	1	ADC input clock ÷ 8
1	X	X	ADC input clock ÷ 16

X = don’t care

ADICLK — ADC Input Clock Select Bit

ADICLK selects either bus clock or CGMXCLK as the input clock source to generate the internal ADC clock. Reset selects CGMXCLK as the ADC clock source.

17.2 Introduction

This section describes the liquid crystal display (LCD) driver module. The LCD driver module can drive a maximum of 33 frontplanes and 4 backplanes, depending on the LCD duty selected.

17.3 Features

Features of the LCD driver module include the following:

- Software programmable driver segment configurations:
  - 32 frontplanes × 4 backplanes (128 segments)
  - 33 frontplanes × 3 backplanes (99 segments)
  - 33 frontplanes × 1 backplane (33 segments)
- LCD bias voltages generated by internal resistor ladder
- Software programmable contrast control

17.4 Pin Name Conventions and I/O Register Addresses

Three dedicated I/O pins are for the backplanes, BP0–BP2; sixteen dedicated I/O pins are for the frontplanes, FP1–FP10 and FP27–FP32; and the sixteen frontplanes, FP11–FP26, are shared with port C and E pins. FP0 and BP3 shares the same pin and configured by the DUTY[1:0] bits in the LCD clock register.

The full names of the LCD output pins are shown in **Table 17-1**. The generic pin names appear in the text that follows.

Table 17-1. Pin Name Conventions

LCD Generic Pin Name	Full MCU Pin Name	Pin Selected for LCD Function by:
FP0/BP3	FP0/BP3	—
BP0–BP2	BP0–BP2	—
FP1–FP10	FP1–FP10	—
FP11–FP18	PTE0/FP11–PTE7/FP18	PEE in CONFIG2
FP19–FP26	PTC0/FP19–PTC7/FP26	PCEL:PCEH in CONFIG2
FP27–FP32	FP27–FP32	—

Section 18. Input/Output (I/O) Ports

18.1 Contents

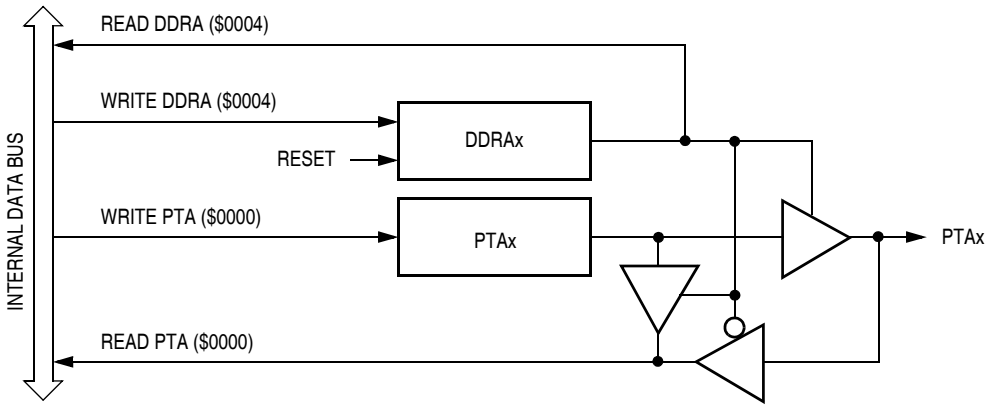

Figure 18-4. Port A I/O Circuit

When DDRAx is a logic 1, reading address $0000 reads the PTAx data latch. When DDRAx is a logic 0, reading address $0000 reads the voltage level on the pin. The data latch can always be written, regardless of the state of its data direction bit.

Table 18-2 summarizes the operation of the port A pins.

Table 18-2. Port A Pin Functions

DDRA Bit	PTA Bit	I/O Pin Mode	Accesses to DDRA	Accesses to PTA	
			Read/Write	Read	Write
0	X(1)	Input, Hi-Z(2)	DDRA[7:0]	Pin	PTA[7:0](3)
1	X	Output	DDRA[7:0]	PTA[7:0]	PTA[7:0]

Notes:
1. X = don't care.
2. Hi-Z = high impedance.
3. Writing affects data register, but does not affect input.

23.6.4 SIM Break Flag Control Register

The SIM break flag control register (SBFCR) contains a bit that enables software to clear status bits while the MCU is in a break state.

Address: $FE03

	Bit 7	6	5	4	3	2	1	Bit 0
Read: / Write:	BCFE	R	R	R	R	R	R	R
Reset:	0							

R = Reserved

Figure 23-7. SIM Break Flag Control Register (SBFCR)

BCFE — Break Clear Flag Enable Bit

This read/write bit enables software to clear status bits by accessing status registers while the MCU is in a break state. To clear status bits during the break state, the BCFE bit must be set.

1 = Status bits clearable during break

0 = Status bits not clearable during break

A.5 Electrical Specifications

Electrical specifications for the MC68HC908LJ24 apply to the MC68HC908LK24, except for the parameters indicated below.

A.5.1 5V DC Electrical Characteristics

Table A-1. 5V DC Electrical Characteristics

Characteristic[1]	Symbol	Min	Typ[2]	Max	Unit
V_{DD} supply current Stop, f_{OP} = 8 kHz[3] with OSC, RTC on	I_{DD}	—	5.5	7.5	µA
Low-voltage inhibit, trip rising voltage LVI reset disabled (LVIRSTD = 1) LVI reset enabled (LVIRSTD = 0)	V_{TRIPR}	3.7 3.62	— —	4.7 4.62	V V

Notes:
1. V_{DD} = 4.5 to 5.5 Vdc, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H, unless otherwise noted.
2. Typical values reflect average measurements at midpoint of voltage range, 25 °C only.
3. The 8kHz clock is from a 32kHz external square wave clock input at OSC1, for the driving the RTC. Due to loading effects, the I_{DD} values will be larger when a 32kHz crystal circuit is connected.

A.5.2 3.3V DC Electrical Characteristics

Table A-2. 3.3V DC Electrical Characteristics

Characteristic[1]	Symbol	Min	Typ[2]	Max	Unit
Low-voltage inhibit, trip rising voltage LVI disabled (LVIRSTD = 1) LVI enabled (LVIRSTD = 0)	V_{TRIPR}	2.2 2.12	— —	2.9 2.82	V V

Notes:
1. V_{DD} = 3.0 to 3.6 Vdc, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H, unless otherwise noted.
2. Typical values reflect average measurements at midpoint of voltage range, 25 °C only.