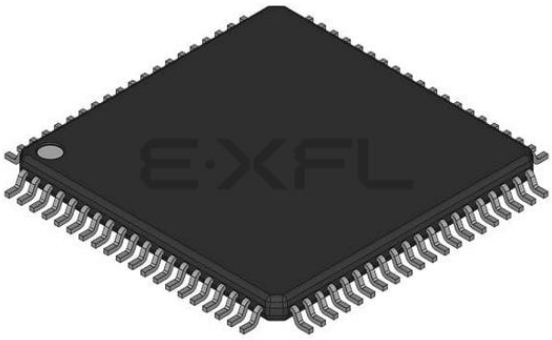

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HC08
Core Size	8-Bit
Speed	8MHz
Connectivity	I²C, IRSCI, SPI
Peripherals	LCD, LVD, POR, PWM
Number of I/O	48
Program Memory Size	24KB (24K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 6x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-QFP
Supplier Device Package	80-QFP (14x14)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc908lj24cfqe

1.2 Introduction

The MC68HC908LJ24 is a member of the low-cost, high-performance M68HC08 Family of 8-bit microcontroller units (MCUs). The M68HC08 Family is based on the customer-specified integrated circuit (CSIC) design strategy. All MCUs in the family use the enhanced M68HC08 central processor unit (CPU08) and are available with a variety of modules, memory sizes and types, and package types.

1.3 Features

Features of the MC68HC908LJ24 include the following:

- High-performance M68HC08 architecture
- Fully upward-compatible object code with M6805, M146805, and M68HC05 Families
  - 8-MHz at 5V operating voltage
  - 4-MHz at 3.3V operating voltage
- 32.768kHz crystal oscillator clock input with 32MHz internal PLL
- Optional continuous crystal oscillator operation in stop mode
- 24K-bytes user program FLASH memory with security[1] feature
- 768 bytes of on-chip RAM
- Up to 48 general-purpose input/output (I/O) pins:
  - High current 15mA sink capability on 30 pins
- Two 16-bit, 2-channel timer interface modules (TIM1 and TIM2) with selectable input capture, output compare, PWM capability on each channel, and external clock input option (T1CLK and T2CLK)
- Real time clock (RTC) with:
  - Clock, calendar, alarm, and chronograph functions
  - Selectable periodic interrupt requests for seconds, minutes, hours, days, 2-Hz, 4-Hz, 8-Hz, 16-Hz, and 128-Hz

1. No security feature is absolutely secure. However, Freescale strategy is to make reading or copying the FLASH difficult for unauthorized users.

Table 4-1. FLASH Block Protect Register to Physical Address

BPR[7:0]	Start Address of Protection Range[1]
$00 to $1F	The entire FLASH memory is **NOT** protected.[2]
$20	$9000 (1**001 0000 0**000 0000) The entire FLASH memory is protected.
$21	$9080 (1**001 0000 1**000 0000)
$22	$9100 (1**001 0001 0**000 0000)
$23	$9180 (1**001 0001 1**000 0000)
$24	$9200 (1**001 0010 0**000 0000)
and so on...	
$DE	$EF00 (1**110 1111 0**000 0000)
$DF	$EF80 (1**110 1111 1**000 0000)
$E0 to $FF	The entire FLASH memory is **NOT** protected.[2]

Notes:
1. The end address of the protected range is always $FFFF.
2. Except the 48-byte user vectors, which is always protected.

6.2 Introduction

The M68HC08 CPU (central processor unit) is an enhanced and fully object-code-compatible version of the M68HC05 CPU. The *CPU08 Reference Manual* (Freescale document order number CPU08RM/AD) contains a description of the CPU instruction set, addressing modes, and architecture.

6.3 Features

Feature of the CPU include:

- Object code fully upward-compatible with M68HC05 Family
- 16-bit stack pointer with stack manipulation instructions
- 16-Bit index register with X-register manipulation instructions
- 8-MHz CPU internal bus frequency
- 64-Kbyte program/data memory space
- 16 addressing modes
- Memory-to-memory data moves without using accumulator
- Fast 8-bit by 8-bit multiply and 16-bit by 8-bit divide instructions
- Enhanced binary-coded decimal (BCD) data handling
- Modular architecture with expandable internal bus definition for extension of addressing range beyond 64-Kbytes
- Low-power stop and wait modes

NOTE: *The location of the stack is arbitrary and may be relocated anywhere in RAM. Moving the SP out of page 0 ($0000 to $00FF) frees direct address (page 0) space. For correct operation, the stack pointer must point only to RAM locations.*

6.4.4 Program Counter

The program counter is a 16-bit register that contains the address of the next instruction or operand to be fetched.

Normally, the program counter automatically increments to the next sequential memory location every time an instruction or operand is fetched. Jump, branch, and interrupt operations load the program counter with an address other than that of the next sequential location.

During reset, the program counter is loaded with the reset vector address located at $FFFE and $FFFF. The vector address is the address of the first instruction to be executed after exiting the reset state.

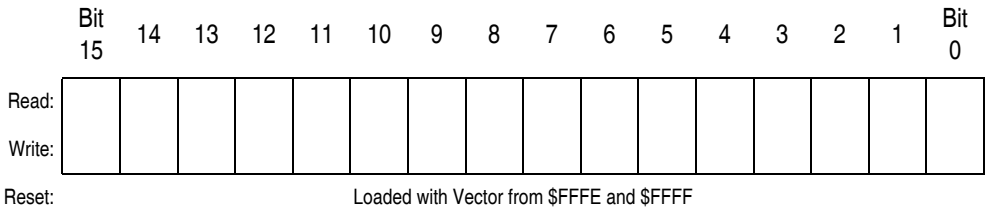
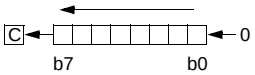
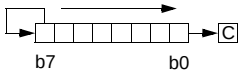


Figure 6-5. Program Counter (PC)

Table 6-1. Instruction Set Summary (Sheet 1 of 8)

Source Form	Operation	Description	Effect on CCR						Address Mode	Opcode	Operand	Cycles
			V	H	I	N	Z	C				
ADC #*opr* ADC *opr* ADC *opr* ADC *opr*,X ADC *opr*,X ADC ,X ADC *opr*,SP ADC *opr*,SP	Add with Carry	A ← (A) + (M) + (C)	↕	↕	–	↕	↕	↕	IMM DIR EXT IX2 IX1 IX SP1 SP2	A9 B9 C9 D9 E9 F9 9EE9 9ED9	ii dd hh ll ee ff ff ff ee ff	2 3 4 4 3 2 4 5
ADD #*opr* ADD *opr* ADD *opr* ADD *opr*,X ADD *opr*,X ADD ,X ADD *opr*,SP ADD *opr*,SP	Add without Carry	A ← (A) + (M)	↕	↕	–	↕	↕	↕	IMM DIR EXT IX2 IX1 IX SP1 SP2	AB BB CB DB EB FB 9EEB 9EDB	ii dd hh ll ee ff ff ff ee ff	2 3 4 4 3 2 4 5
AIS #*opr*	Add Immediate Value (Signed) to SP	SP ← (SP) + (16 « M)	–	–	–	–	–	–	IMM	A7	ii	2
AIX #*opr*	Add Immediate Value (Signed) to H:X	H:X ← (H:X) + (16 « M)	–	–	–	–	–	–	IMM	AF	ii	2
AND #*opr* AND *opr* AND *opr* AND *opr*,X AND *opr*,X AND ,X AND *opr*,SP AND *opr*,SP	Logical AND	A ← (A) & (M)	0	–	–	↕	↕	–	IMM DIR EXT IX2 IX1 IX SP1 SP2	A4 B4 C4 D4 E4 F4 9EE4 9ED4	ii dd hh ll ee ff ff ff ee ff	2 3 4 4 3 2 4 5
ASL *opr* ASLA ASLX ASL *opr*,X ASL ,X ASL *opr*,SP	Arithmetic Shift Left (Same as LSL)		↕	–	–	↕	↕	↕	DIR INH INH IX1 IX SP1	38 48 58 68 78 9E68	dd ff ff	4 1 1 4 3 5
ASR *opr* ASRA ASRX ASR *opr*,X ASR *opr*,X ASR *opr*,SP	Arithmetic Shift Right		↕	–	–	↕	↕	↕	DIR INH INH IX1 IX SP1	37 47 57 67 77 9E67	dd ff ff	4 1 1 4 3 5
BCC *rel*	Branch if Carry Bit Clear	PC ← (PC) + 2 + rel ? (C) = 0	–	–	–	–	–	–	REL	24	rr	3
BCLR *n*, *opr*	Clear Bit n in M	Mn ← 0	–	–	–	–	–	–	DIR (b0) DIR (b1) DIR (b2) DIR (b3) DIR (b4) DIR (b5) DIR (b6) DIR (b7)	11 13 15 17 19 1B 1D 1F	dd dd dd dd dd dd dd dd	4 4 4 4 4 4 4 4

The following conditions apply when in manual mode:

- $\overline{ACQ}$ is a writable control bit that controls the mode of the filter. Before turning on the PLL in manual mode, the $\overline{ACQ}$ bit must be clear.
- Before entering tracking mode ($\overline{ACQ}$ = 1), software must wait a given time, t_{ACQ} (See **8.9 Acquisition/Lock Time Specifications**.), after turning on the PLL by setting PLLON in the PLL control register (PCTL).
- Software must wait a given time, t_{AL}, after entering tracking mode before selecting the PLL as the clock source to CGMOUT (BCS = 1).
- The LOCK bit is disabled.
- CPU interrupts from the CGM are disabled.

8.4.6 Programming the PLL

The following procedure shows how to program the PLL.

NOTE: *The round function in the following equations means that the real number should be rounded to the nearest integer number.*

1. Choose the desired bus frequency, f_{BUSDES}.
2. Calculate the desired VCO frequency, $f_{VCLKDES}$.

$$f_{VCLKDES} = 2^P \times f_{CGMPCLK} = 2^P \times 4 \times f_{BUSDES}$$

   where P is the power of two multiplier, and can be 0, 1, 2, or 3
3. Choose a practical PLL reference frequency, f_{RCLK}, and the reference clock divider, R. Typically, the reference is 32.768 kHz and R = 1.

   Frequency errors to the PLL are corrected at a rate of f_{RCLK}/R. For stability and lock time reduction, this rate must be as fast as possible. The VCO frequency must be an integer multiple of this rate.

When the user dedicates a page of FLASH for data storage, and the size of the data array defined, each call of the EE_WRTIE routine will automatically transfer the data in the data array (in RAM) to the next blank block of locations in the FLASH page. Once a page is filled up, the EE_WRITE routine automatically erases the page, and starts reuse the page again. In the 128-byte page, an 8-byte control block is used by the routine to monitor the utilization of the page. In effect, only 120 bytes are used for data storage. (see **Figure 10-10**). The page control operations are transparent to the user.

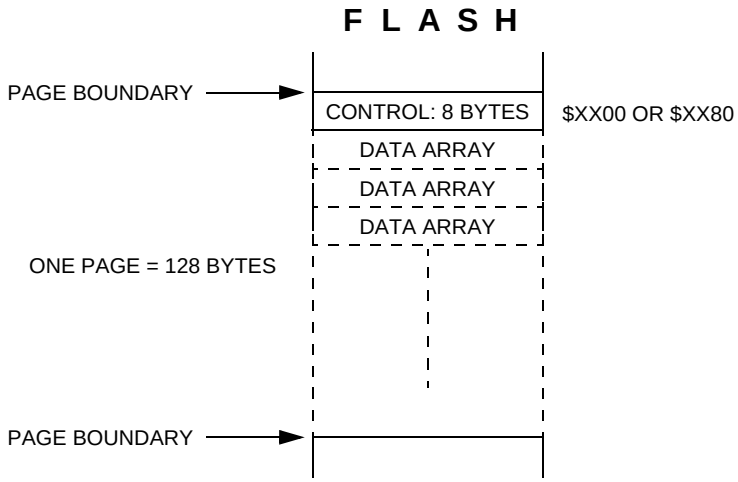


Figure 10-10. EE_WRITE FLASH Memory Usage

When using this routine to store a 2-byte data array, the FLASH page can be programmed 60 times before the an erase is required. In effect, the write/erase endurance is increased by 60 times. When a 15-byte data array is used, the write/erase endurance is increased by 8 times. Due to the FLASH page size limitation, the data array is limited from 2 bytes to 15 bytes.

The coding example below uses the $EF00–$EE7F page for data storage. The data array size is 15 bytes, and the bus speed is 4.9152 MHz. The coding assumes the data block is already loaded in RAM, with the address pointer, FILE_PTR, pointing to the first byte of the data block.

11.4 Pin Name Conventions

The text that follows describes both timers, TIM1 and TIM2. The TIM input/output (I/O) pin names are T[1,2]CH0 (timer channel 0). T[1,2]CH1 (timer channel 1), and T[1,2]CLK (external timer clock), where “1” is used to indicate TIM1 and “2” is used to indicate TIM2. The full names of the TIM I/O pins are listed in **Table 11-1**. The generic pin names appear in the text that follows.

Table 11-1. Pin Name Conventions

TIM Generic Pin Names:		T[1,2]CH0	T[1,2]CH1	T[1,2]CLK
Full TIM Pin Names:	TIM1	PTB2/T1CH0	PTB3/T1CH1	PTD4/KBI4/T1CLK
	TIM2	PTB4/T2CH0	PTB5/T2CH1	PTD5/KBI5/T2CLK

NOTE: *References to either timer 1 or timer 2 may be made in the following text by omitting the timer number. For example, TCH0 may refer generically to T1CH0 and T2CH0, and TCH1 may refer to T1CH1 and T2CH1.*

The T1CLK and T2CLK pins are also shared with KBI4 and KBI5 respectively. To avoid erratic behavior, these two pins should never be configured for use as TCLK and KBI inputs simultaneously.

11.5 Functional Description

Figure 11-1 shows the structure of the TIM. The central component of the TIM is the 16-bit TIM counter that can operate as a free-running counter or a modulo up-counter. The TIM counter provides the timing reference for the input capture and output compare functions. The TIM counter modulo registers, TMODH:TMODL, control the modulo value of the TIM counter. Software can read the TIM counter value at any time without affecting the counting sequence.

The two TIM channels (per timer) are programmable independently as input capture or output compare channels.

The value in the TIM counter modulo registers and the selected prescaler output determines the frequency of the PWM output. The frequency of an 8-bit PWM signal is variable in 256 increments. Writing $00FF (255) to the TIM counter modulo registers produces a PWM period of 256 times the internal bus clock period if the prescaler select value is $000. See **11.10.1 TIM Status and Control Register**.

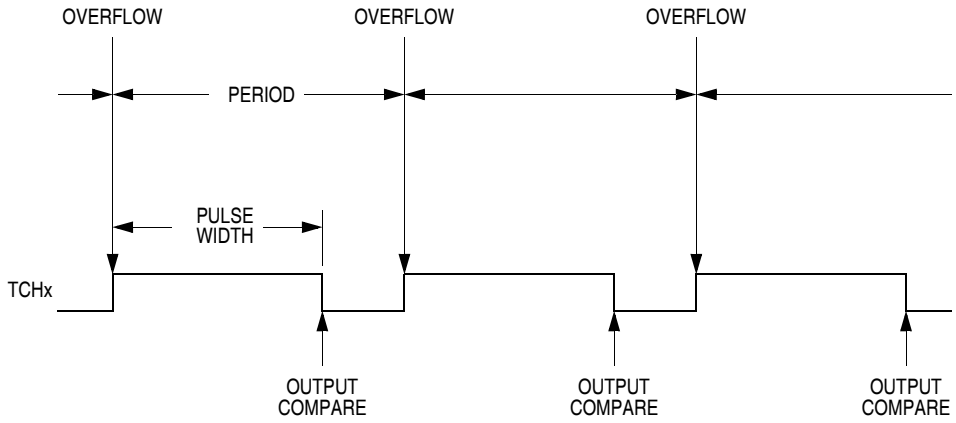


Figure 11-3. PWM Period and Pulse Width

The value in the TIM channel registers determines the pulse width of the PWM output. The pulse width of an 8-bit PWM signal is variable in 256 increments. Writing $0080 (128) to the TIM channel registers produces a duty cycle of 128/256 or 50%.

11.5.4.1 Unbuffered PWM Signal Generation

Any output compare channel can generate unbuffered PWM pulses as described in **11.5.4 Pulse Width Modulation (PWM)**. The pulses are unbuffered because changing the pulse width requires writing the new pulse width value over the old value currently in the TIM channel registers.

An unsynchronized write to the TIM channel registers to change a pulse width value could cause incorrect operation for up to two PWM periods. For example, writing a new value before the counter reaches the old value but after the counter reaches the new value prevents any compare during that PWM period. Also, using a TIM overflow interrupt routine to write a new, smaller pulse width value may cause the compare to be missed. The TIM may pass the new value before it is written.

In input capture mode (MSxB:MSxA = 0:0), reading the high byte of the TIM channel x registers (TCHxH) inhibits input captures until the low byte (TCHxL) is read.

In output compare mode (MSxB:MSxA ≠ 0:0), writing to the high byte of the TIM channel x registers (TCHxH) inhibits output compares until the low byte (TCHxL) is written.

Address: T1CH0H, $0026 and T2CH0H, $0031

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	Bit 15	14	13	12	11	10	9	Bit 8
Write:								
Reset:	Indeterminate after reset							

Figure 11-12. TIM Channel 0 Register High (TCH0H)

Address: T1CH0L, $0027 and T2CH0L $0032

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	Bit 7	6	5	4	3	2	1	Bit 0
Write:								
Reset:	Indeterminate after reset							

Figure 11-13. TIM Channel 0 Register Low (TCH0L)

Address: T1CH1H, $0029 and T2CH1H, $0034

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	Bit 15	14	13	12	11	10	9	Bit 8
Write:								
Reset:	Indeterminate after reset							

Figure 11-14. TIM Channel 1 Register High (TCH1H)

Address: T1CH1L, $002A and T2CH1L, $0035

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	Bit 7	6	5	4	3	2	1	Bit 0
Write:								
Reset:	Indeterminate after reset							

Figure 11-15. TIM Channel 1 Register Low (TCH1L)

OUTF[1:0] — Calibration Mode CALOUT Pin Output Selection

These two bits select the output option for the CALOUT pin. When CAL = 0, OUTF[1:0] is always 00.

Table 12-4. CALOUT Pin Output Option

OUTF[1:0]	CALOUT Pin Output
00	CALOUT pin is disconnected.
01	CALOUT pin outputs compensated 1-Hz.
10	CALOUT pin outputs CGMXCLK clock.
11	Reserved

RTCWE[1:0] — RTC Module Write Enable

These two write-only bits control the write-protect function of several RTC registers and bits. After a reset, write-protect is disabled, allowing full write access to RTC registers and bits. These two bits always read as 0.

To enable write-protect, perform the following sequence:

1. Write %10 to RTCWE[1:0] bits
2. Write %10 to RTCWE[1:0] bits

To disable write-protect, perform the following sequence:

1. Write %00 to RTCWE[1:0] bits
2. Write %01 to RTCWE[1:0] bits
3. Write %11 to RTCWE[1:0] bits
4. Write %10 to RTCWE[1:0] bits

To disable write-protect from an unsure protection state, first perform the enable write-protect sequence, followed by the disable write-protect sequence.

Table 13-5 shows a summary of I/O pin functions when the SCI is enabled.

Table 13-5. SCI Pin Functions (Standard and Infrared)

SCC1 [ENSCI]	SCIRCR [IREN]	SCC2 [TE]	SCC2 [RE]	TxD Pin	RxD Pin
1	0	0	0	Hi-Z(1)	Input ignored (terminate externally)
1	0	0	1	Hi-Z(1)	Input sampled, pin should idle high
1	0	1	0	Output SCI (idle high)	Input ignored (terminate externally)
1	0	1	1	Output SCI (idle high)	Input sampled, pin should idle high
1	1	0	0	Hi-Z(1)	Input ignored (terminate externally)
1	1	0	1	Hi-Z(1)	Input sampled, pin should idle high
1	1	1	0	Output IR SCI (idle high)	Input ignored (terminate externally)
1	1	1	1	Output IR SCI (idle high)	Input sampled, pin should idle high
0	X	X	X	Pins under port control (standard I/O port)	

Notes:
1. After completion of transmission in progress.

13.11 I/O Registers

The following I/O registers control and monitor SCI operation:

- SCI control register 1 (SCC1)
- SCI control register 2 (SCC2)
- SCI control register 3 (SCC3)
- SCI status register 1 (SCS1)
- SCI status register 2 (SCS2)
- SCI data register (SCDR)
- SCI baud rate register (SCBR)
- SCI infrared control register (SCIRCR)

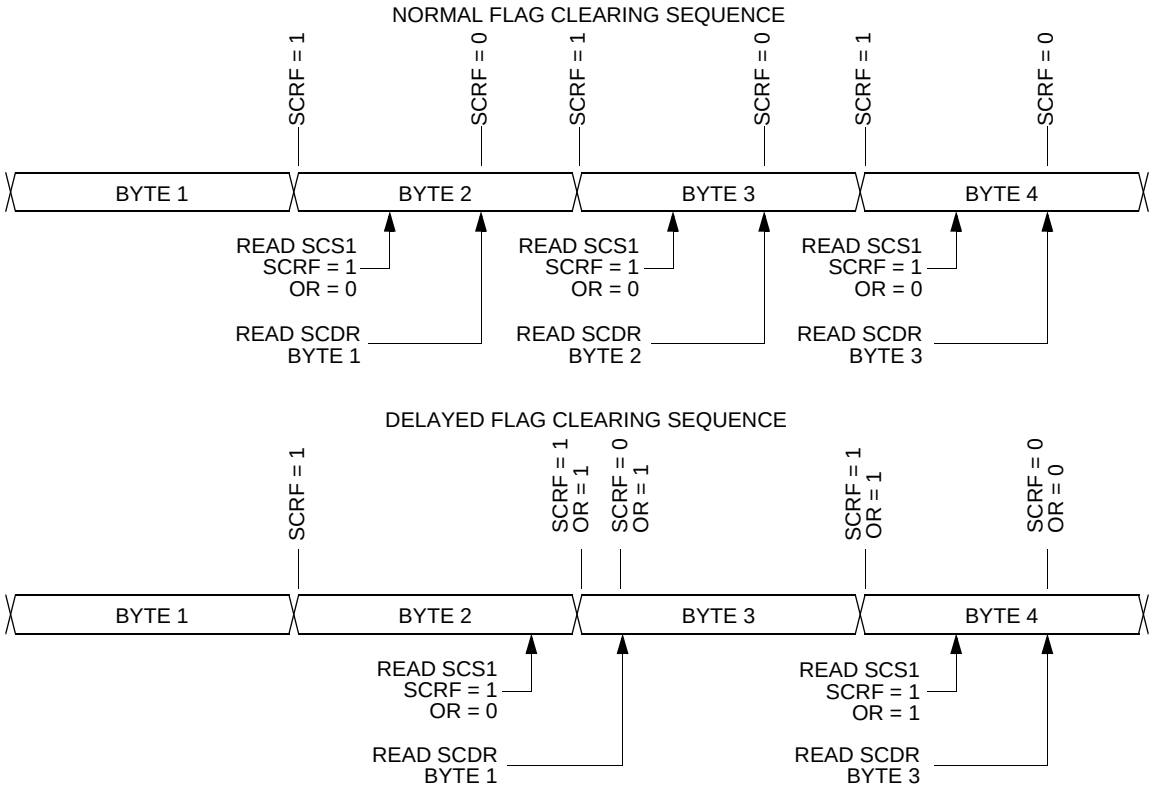


Figure 13-16. Flag Clearing Sequence

PE — Receiver Parity Error Bit

This clearable, read-only bit is set when the SCI detects a parity error in incoming data. PE generates an SCI error CPU interrupt request if the PEIE bit in SCC3 is also set. Clear the PE bit by reading SCS1 with PE set and then reading the SCDR. Reset clears the PE bit.

1 = Parity error detected

0 = No parity error detected

16.8 I/O Registers

These I/O registers control and monitor operation of the ADC:

- ADC status and control register, (ADSCR)
- ADC data register (ADRH:ADRL)
- ADC clock control register (ADCLK)

16.8.1 ADC Status and Control Register

This section describes the function of the ADC status and control register (ADSCR). Writing ADSCR aborts the current conversion and initiates a new conversion.

Address: $003C

Read:	COCO	AIEN	ADCO	ADCH4	ADCH3	ADCH2	ADCH1	ADCH0
Write:								
Reset:	0	0	0	1	1	1	1	1

= Unimplemented

Figure 16-4. ADC Status and Control Register (ADSCR)

COCO — Conversions Complete Bit

When the AIEN bit is a logic 0, the COCO is a read-only bit which is set each time a conversion is completed. This bit is cleared whenever the ADSCR is written, or whenever the ADC clock control register is written, or whenever the ADC data register low, ADRL, is read.

If the AIEN bit is logic 1, the COCO bit always read as logic 0, CPU to service the ADC interrupt will be generated at the end if an ADC conversion. Reset clears the COCO bit.

1 = Conversion completed (AIEN = 0)
0 = Conversion not completed (AIEN = 0)/CPU interrupt (AIEN=1)

AIEN — ADC Interrupt Enable Bit

When this bit is set, an interrupt is generated at the end of an ADC conversion. The interrupt signal is cleared when the data register, ADR0, is read or the ADSCR is written. Reset clears the AIEN bit.

1 = ADC interrupt enabled
0 = ADC interrupt disabled

Table 18-1. Port Control Register Bits Summary (Sheet 2 of 2)

Port	Bit	DDR	Module Control			Pin
			Module	Register	Control Bit	
D[1]	0	DDRD0	SPI RTC	SPCR ($0010)	SPE	PTD0/$\overline{SS}$/CALIN
				RTCCOMR ($0040)	CAL	
	1	DDRD1		SPCR ($0010)	SPE	PTD1/MISO
	2	DDRD2				PTD2/MOSI
	3	DDRD3		SPCR ($0010)	SPE	PTD3/SPSCK/CALOUT
				RTCCOMR ($0040)	CAL	
	4	DDRD4	KBI TIM	KBIER ($001C)	KBIE4	PTD4/KBI4/T1CLK
				T1SC ($0020)	PS[2:0]	
	5	DDRD5		KBIER ($001C)	KBIE5	PTD5/KBI5/T2CLK
				T2SC ($002B)	PS[2:0]	
	6	DDRD6	KBI MMIIC	KBIER ($001C)	KBIE6	PTD6/KBI6/SCL
				MMCR ($006C)	MMEN	
	7	DDRD7		KBIER ($001C)	KBIE7	PTD7/KBI7/SDA
				MMCR ($006C)	MMEN	
E	0	DDRE0	LCD	CONFIG2 ($001D)	PEE	PTE0/FP11
	1	DDRE1				PTE1/FP12
	2	DDRE2				PTE2/FP13
	3	DDRE3				PTE3/FP14
	4	DDRE4				PTE4/FP15
	5	DDRE5				PTE5/FP16
	6	DDRE6				PTE6/FP17
	7	DDRE7				PTE7/FP18
F	0	DDRF0	—	—	—	PTF0
	1	DDRF1				PTF1
	2	DDRF2				PTF2
	3	DDRF3				PTF3
	4	DDRF4				PTF4
	5	DDRF5				PTF5
	6	DDRF6				PTF6
	7	DDRF7				PTF7

Notes:
1. In addition to the standard I/O function on PTD0 and PTD3–PTD7 pins, these pins are shared with two other modules. For each of the pins, ONLY enable ONE module at any one time to avoid pin contention.

18.5 Port C

Port C is an 8-bit special function port that shares all of its port pins with the liquid crystal display (LCD) driver module.

Port pins PTC0–PTC7 can be configured for direct LED drive.

18.5.1 Port C Data Register (PTC)

The port C data register contains a data latch for each of the eight port C pins.

Address: $0002

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PTC7	PTC6	PTC5	PTC4	PTC3	PTC2	PTC1	PTC0
Reset:	Unaffected by reset							
Alternative Function:	FP26	FP25	FP24	FP23	FP22	FP21	FP20	FP19
Additional Function:	LED drive	LED drive	LED drive	LED drive	LED drive	LED drive	LED drive	LED drive

Figure 18-9. Port C Data Register (PTC)

PTC[7:0] — Port C Data Bits

These read/write bits are software programmable. Data direction of each port C pin is under the control of the corresponding bit in data direction register C. Reset has no effect on port C data.

FP[26:19] — LCD Driver Frontplanes 26–19

FP[26:19] are pins used for the frontplane output of the LCD driver module. The enable bits, PCEH and PCEL, in the CONFIG2 register, determine whether the PTC7/FP26–PTC4/FP23 and PTC3/FP22–PTC0/FP19 pins are LCD frontplane driver pins or general-purpose I/O pins. See **Section 17. Liquid Crystal Display (LCD) Driver**.

LED drive — Direct LED Drive Pins

PTC0–PTC7 pins can be configured for direct LED drive. See **18.5.3 Port C LED Control Register (LEDC)**.

21.8.1 Wait Mode

The COP remains active during wait mode. To prevent a COP reset during wait mode, periodically clear the COP counter in a CPU interrupt routine.

21.8.2 Stop Mode

Stop mode turns off the ICLK input to the COP and clears the COP prescaler. Service the COP immediately before entering or after exiting stop mode to ensure a full COP timeout period after entering or exiting stop mode.

To prevent inadvertently turning off the COP with a STOP instruction, a configuration option is available that disables the STOP instruction. When the STOP bit in the configuration register has the STOP instruction is disabled, execution of a STOP instruction results in an illegal opcode reset.

21.9 COP Module During Break Mode

The COP is disabled during a break interrupt when V_{TST} is present on the $\overline{RST}$ pin.

24.3 Absolute Maximum Ratings

Maximum ratings are the extreme limits to which the MCU can be exposed without permanently damaging it.

NOTE: *This device is not guaranteed to operate properly at the maximum ratings. Refer to* ***DC Electrical Characteristics*** *for guaranteed operating conditions.*

Table 24-1. Absolute Maximum Ratings

Characteristic[1]	Symbol	Value	Unit
Supply voltage	V_{DD}	–0.3 to +6.0	V
Input voltage All pins (except $\overline{IRQ}$) $\overline{IRQ}$ pin	V_{IN}	V_{SS} – 0.3 to V_{DD} + 0.3 V_{SS} – 0.3 to 8.5	V
Maximum current per pin excluding V_{DD} and V_{SS}	I	±25	mA
Maximum current out of V_{SS}	I_{MVSS}	100	mA
Maximum current into V_{DD}	I_{MVDD}	100	mA
Storage temperature	T_{STG}	–55 to +150	°C

Notes:
1. Voltages referenced to V_{SS}.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum-rated voltages to this high-impedance circuit. For proper operation, it is recommended that V_{IN} and V_{OUT} be constrained to the range $V_{SS} \le (V_{IN}$ or $V_{OUT}) \le V_{DD}$. Reliability of operation is enhanced if unused inputs are connected to an appropriate logic voltage level (for example, either V_{SS} or V_{DD}.)

24.4 Functional Operating Range

Table 24-2. Functional Operating Range

Characteristic	Symbol	Value	Unit
Operating temperature range	T_A	–40 to +85	°C
Operating voltage range	V_{DD}	3.3 ± 10% 5 ± 10%	V

24.5 Thermal Characteristics

Table 24-3. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal resistance 64-pin LQFP 64-pin QFP 80-pin LQFP 80-pin QFP	θ_{JA}	 72 67 85 75	°C/W
I/O pin power dissipation	$P_{I/O}$	User determined	W
Power dissipation(1)	P_D	$P_D = (I_{DD} \times V_{DD}) + P_{I/O} = K/(T_J + 273\ °C)$	W
Constant(2)	K	$P_D \times (T_A + 273\ °C) + P_D^2 \times \theta_{JA}$	W/°C
Average junction temperature	T_J	$T_A + (P_D \times \theta_{JA})$	°C

Notes:
1. Power dissipation is a function of temperature.
2. K constant unique to the device. K can be determined for a known T_A and measured P_D. With this value of K, P_D and T_J can be determined for any value of T_A.