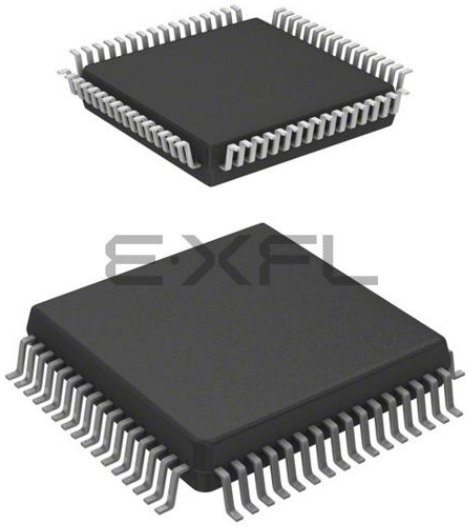

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	HC08
Core Size	8-Bit
Speed	8MHz
Connectivity	I²C, IRSCI, SPI
Peripherals	LCD, LVD, POR, PWM
Number of I/O	40
Program Memory Size	24KB (24K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 6x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-QFP
Supplier Device Package	64-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc908lj24cfue

5.4 Configuration Register 1 (CONFIG1)

The CONFIG1 register can be written once after each reset.

Address: $001F

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	COPRS	LVISTOP	LVIRSTD	LVIPWRD	0	SSREC	STOP	COPD
Write:								
Reset:	0	0	0	0††	0	0	0	0

†† Reset by POR only.

= Unimplemented

Figure 5-2. Configuration Register 1 (CONFIG1)

COPRS — COP Rate Select

COPRS selects the COP time-out period. Reset clears COPRS. (See **Section 21. Computer Operating Properly (COP)**.)

1 = COP time out period = $2^{13} – 2^4$ ICLK cycles
0 = COP time out period = $2^{18} – 2^4$ ICLK cycles

LVISTOP — LVI Enable in Stop Mode

When the LVIPWRD bit is clear, setting the LVISTOP bit enables the LVI to operate during stop mode. Reset clears LVISTOP. (See **Section 22. Low-Voltage Inhibit (LVI)**.)

1 = LVI enabled during stop mode
0 = LVI disabled during stop mode

LVIRSTD — LVI Reset Disable

LVIRSTD disables the reset signal from the LVI module. (See **Section 22. Low-Voltage Inhibit (LVI)**.)

1 = LVI module resets disabled
0 = LVI module resets enabled

LVIPWRD — LVI Power Disable Bit

LVIPWRD disables the LVI module. (See **Section 22. Low-Voltage Inhibit (LVI)**.)

1 = LVI module power disabled
0 = LVI module power enabled

Section 7. Oscillator (OSC)

7.1 Contents

7.2 Introduction

The oscillator module provides the reference clock for the clock generator module (CGM), the real time clock module (RTC), and other MCU sub-systems.

The oscillator module consist of two types of oscillator circuits:

- Internal RC oscillator
- 32.768kHz crystal (x-tal) oscillator

7.5.1 Crystal Amplifier Input Pin (OSC1)

OSC1 pin is an input to the crystal oscillator amplifier. Schmitt trigger and glitch filter are implemented on this pin to improve EMC performance. See **Section 24. Electrical Specifications** for detail specification of the glitch filter.

7.5.2 Crystal Amplifier Output Pin (OSC2)

OSC2 pin is the output of the crystal oscillator inverting amplifier.

7.5.3 Oscillator Enable Signal (SIMOSCEN)

The SIMOSCEN signal from the system integration module (SIM) enables/disables the x-tal oscillator circuit.

7.5.4 Internal RC Clock (ICLK)

The ICLK clock is the output from the internal RC oscillator. This clock drives the SIM and COP modules.

7.5.5 CGM Oscillator Clock (CGMXCLK)

The CGMXCLK clock is the output from the x-tal oscillator. This clock drives to CGM, real time clock module, analog-to-digital converter, liquid crystal display driver module, and other MCU sub-systems.

7.5.6 CGM Reference Clock (CGMRCLK)

This is buffered signal of CGMXCLK, it is used by the CGM as the phase-locked-loop (PLL) reference clock.

7.6 Low Power Modes

The WAIT and STOP instructions put the MCU in low-power consumption standby modes.

8.6.4 PLL VCO Range Select Register

The PLL VCO range select register (PMRS) contains the programming information required for the hardware configuration of the VCO.

Address: $003A

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	VRS7	VRS6	VRS5	VRS4	VRS3	VRS2	VRS1	VRS0
Reset:	0	1	0	0	0	0	0	0

Figure 8-8. PLL VCO Range Select Register (PMRS)

VRS[7:0] — VCO Range Select Bits

These read/write bits control the hardware center-of-range linear multiplier L which, in conjunction with E (See **8.4.3 PLL Circuits**, **8.4.6 Programming the PLL**, and **8.6.1 PLL Control Register**.), controls the hardware center-of-range frequency, f_{VRS}. VRS[7:0] cannot be written when the PLLON bit in the PCTL is set. (See **8.4.7 Special Programming Exceptions**.) A value of $00 in the VCO range select register disables the PLL and clears the BCS bit in the PLL control register (PCTL). (See **8.4.8 Base Clock Selector Circuit** and **8.4.7 Special Programming Exceptions**.). Reset initializes the register to $40 for a default range multiply value of 64.

NOTE: *The VCO range select bits have built-in protection such that they cannot be written when the PLL is on (PLLON = 1) and such that the VCO clock cannot be selected as the source of the base clock (BCS = 1) if the VCO range select bits are all clear.*

The PLL VCO range select register must be programmed correctly. Incorrect programming can result in failure of the PLL to achieve lock.

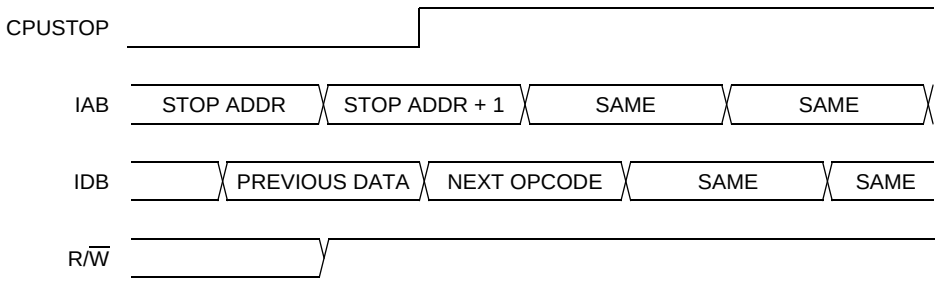
Section 9. System Integration Module (SIM)

9.1 Contents

A break interrupt during stop mode sets the SIM break stop/wait bit (SBSW) in the SIM break status register (SBSR).

The SIM counter is held in reset from the execution of the STOP instruction until the beginning of stop recovery. It is then used to time the recovery period. **Figure 9-18** shows stop mode entry timing.

NOTE: *To minimize stop current, all pins configured as inputs should be driven to a logic 1 or logic 0.*



NOTE: Previous data can be operand data or the STOP opcode, depending on the last instruction.

Figure 9-18. Stop Mode Entry Timing

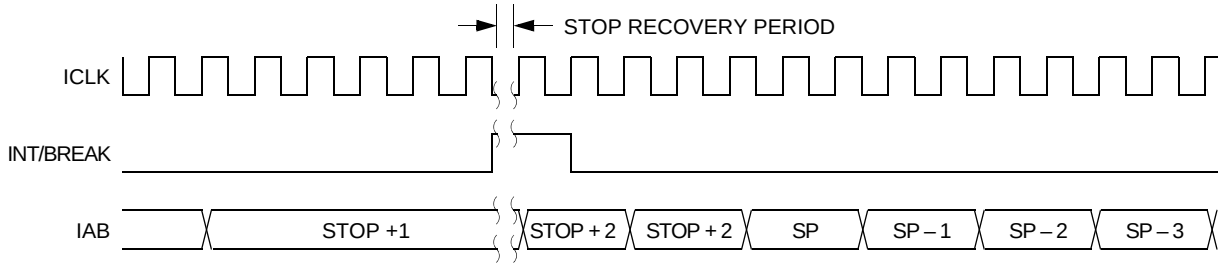


Figure 9-19. Stop Mode Recovery from Interrupt or Break

9.8 SIM Registers

The SIM has three memory-mapped registers:

- SIM Break Status Register (SBSR) — $FE00
- SIM Reset Status Register (SRSR) — $FE01
- SIM Break Flag Control Register (SBFCR) — $FE03

9.8.2 SIM Reset Status Register

This register contains six flags that show the source of the last reset provided all previous reset status bits have been cleared. Clear the SIM reset status register by reading it. A power-on reset sets the POR bit and clears all other bits in the register.

Address: $FE01

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	POR	PIN	COP	ILOP	ILAD	0	LVI	0
Write:								
Reset:	1	0	0	0	0	0	0	0

= Unimplemented

Figure 9-21. SIM Reset Status Register (SRSR)

POR — Power-On Reset Bit
1 = Last reset caused by POR circuit
0 = Read of SRSR

PIN — External Reset Bit
1 = Last reset caused by external reset pin ($\overline{\text{RST}}$)
0 = POR or read of SRSR

COP — Computer Operating Properly Reset Bit
1 = Last reset caused by COP counter
0 = POR or read of SRSR

ILOP — Illegal Opcode Reset Bit
1 = Last reset caused by an illegal opcode
0 = POR or read of SRSR

ILAD — Illegal Address Reset Bit (opcode fetches only)
1 = Last reset caused by an opcode fetch from an illegal address
0 = POR or read of SRSR

LVI — Low-Voltage Inhibit Reset Bit
1 = Last reset caused by the LVI circuit
0 = POR or read of SRSR

Section 10. Monitor ROM (MON)

10.1 Contents

Upon power-on reset, if the received bytes of the security code do not match the data at locations $FFF6–$FFFD, the host fails to bypass the security feature. The MCU remains in monitor mode, but reading a FLASH location returns an invalid value and trying to execute code from FLASH causes an illegal address reset. After receiving the eight security bytes from the host, the MCU transmits a break character, signifying that it is ready to receive a command.

NOTE: *The MCU does not transmit a break character until after the host sends the eight security bits.*

To determine whether the security code entered is correct, check to see if bit 6 of RAM address $40 is set. If it is, then the correct security code has been entered and FLASH can be accessed.

If the security sequence fails, the device should be reset by a power-on reset and brought up in monitor mode to attempt another entry. After failing the security sequence, the FLASH module can also be mass erased by executing an erase routine that was downloaded into internal RAM. The mass erase operation clears the security code locations so that all eight security bytes become $FF (blank).

NOTE: *With compensation enabled, the RTC clock and calendar register updates may not be synchronized to the timebase and chronograph clocks, since their clocks are derived from the uncompensated CGMXCLK.*

Hence, time intervals for timebase ticks may not align with the RTC clock and calendar register updates.

CHRCLR — Chronograph counter clear

Setting this write-only bit resets the chronograph counter and the chronograph data register (CHRR). Setting CHRCLR has no effect on any other registers. Counting resumes from $00. CHRCLR is cleared automatically after the chronograph counter is reset and always reads as logic 0. Reset clears the CHRCLR bit.

1 = Chronograph counter cleared
0 = No effect

CHRE — Chronograph Enable

This read/write bit enables the chronograph counter. When the chronograph counter is disabled (CHRE = 0), the value in the chronograph data register is held at the count value. Reset clears the CHRE bit.

1 = Chronograph counter enabled
0 = Chronograph counter disabled

RTCE — Real Time Clock Enable

This read/write bit enables the entire RTC module, allowing all RTC and chronograph operations. Disabling the RTC module does not affect the contents in the RTC registers. Reset clears the RTCE bit.

1 = RTC module enabled
0 = RTC module disabled

TBH — Timebase High Frequency Select

This read/write bit selects the timebase interrupt period for TB1 and TB2. Reset clears the TBH bit.

1 = TB1 interrupt is 0.125s; TB2 interrupt is 0.0625s
0 = TB1 interrupt is 0.5s; TB2 interrupt is 0.25s

12.10.5 RTC Status Register (RTCSR)

The RTC status register contains eight status flags. When a flag is set and the corresponding interrupt enable bit is also set, a CPU interrupt request is generated.

Address: $0044

	ALMF	CHRF	DAYF	HRF	MINF	SECF	TB1F	TB2F
Read:								
Write:								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 12-10. RTC Status Register (RTCSR)

ALMF — Alarm Flag

This clearable, read-only bit is set when the value in the RTC hour and minute counters matches the value in the alarm hour and alarm minute registers. When the ALMIE bit in RTCCR1 is set, ALMF generates a CPU interrupt request. In normal operation, clear the ALMF bit by reading RTCSR with ALMF set and then reading the alarm hour register (ALHR). Reset clears ALMF.

1 = RTC hour and minute counters matches the alarm hour and minute registers

0 = No matching between hour and minute counters and alarm hour and minute registers

CHRF — Chronograph Flag

This clearable, read-only bit is set on every tick of the chronograph counter (every counter count). The tick is on every 1/128 seconds (see **12.5.4 Chronograph Functions**). When the CHRIE bit in RTCCR1 is set, CHRF generates a CPU interrupt request. In normal operation, clear the CHRF bit by reading RTCSR with CHRF set and then reading the chronograph data register (CHRR). Reset clears CHRF.

1 = A chronograph counter tick has occurred

0 = No chronograph counter tick has occurred

13.7.2.3 Break Characters

Writing a logic 1 to the send break bit, SBK, in SCC2 loads the transmit shift register with a break character. A break character contains all logic 0s and has no start, stop, or parity bit. Break character length depends on the M bit in SCC1. As long as SBK is at logic 1, transmitter logic continuously loads break characters into the transmit shift register. After software clears the SBK bit, the shift register finishes transmitting the last break character and then transmits at least one logic 1. The automatic logic 1 at the end of a break character guarantees the recognition of the start bit of the next character.

The SCI recognizes a break character when a start bit is followed by eight or nine logic 0 data bits and a logic 0 where the stop bit should be.

Receiving a break character has the following effects on SCI registers:

- Sets the framing error bit (FE) in SCS1
- Sets the SCI receiver full bit (SCRF) in SCS1
- Clears the SCI data register (SCDR)
- Clears the R8 bit in SCC3
- Sets the break flag bit (BKF) in SCS2
- May set the overrun (OR), noise flag (NF), parity error (PE), or reception in progress flag (RPF) bits

13.7.2.4 Idle Characters

An idle character contains all logic 1s and has no start, stop, or parity bit. Idle character length depends on the M bit in SCC1. The preamble is a synchronizing idle character that begins every transmission.

If the TE bit is cleared during a transmission, the TxD pin becomes idle after completion of the transmission in progress. Clearing and then setting the TE bit during a transmission queues an idle character to be sent after the character currently being transmitted.

As the receiver samples an incoming character, it resynchronizes the RT clock on any valid falling edge within the character. Resynchronization within characters corrects misalignments between transmitter bit times and receiver bit times.

Slow Data Tolerance

Figure 13-10 shows how much a slow received character can be misaligned without causing a noise error or a framing error. The slow stop bit begins at RT8 instead of RT1 but arrives in time for the stop bit data samples at RT8, RT9, and RT10.

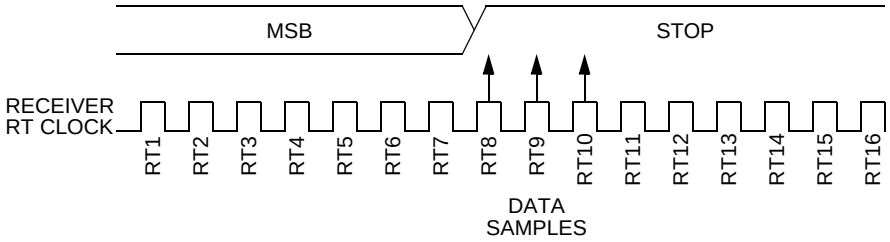


Figure 13-10. Slow Data

For an 8-bit character, data sampling of the stop bit takes the receiver 9 bit times × 16 RT cycles + 10 RT cycles = 154 RT cycles.

With the misaligned character shown in **Figure 13-10**, the receiver counts 154 RT cycles at the point when the count of the transmitting device is 9 bit times × 16 RT cycles + 3 RT cycles = 147 RT cycles.

The maximum percent difference between the receiver count and the transmitter count of a slow 8-bit character with no errors is

$$\left|\frac{154 - 147}{154}\right| \times 100 = 4.54\%$$

For a 9-bit character, data sampling of the stop bit takes the receiver 10 bit times × 16 RT cycles + 10 RT cycles = 170 RT cycles.

With the misaligned character shown in **Figure 13-10**, the receiver counts 170 RT cycles at the point when the count of the transmitting device is 10 bit times × 16 RT cycles + 3 RT cycles = 163 RT cycles.

14.2 Introduction

This section describes the serial peripheral interface (SPI) module, which allows full-duplex, synchronous, serial communications with peripheral devices.

14.3 Features

Features of the SPI module include the following:

- Full-duplex operation
- Master and slave modes
- Double-buffered operation with separate transmit and receive registers
- Four master mode frequencies (maximum = bus frequency ÷ 2)
- Maximum slave mode frequency = bus frequency
- Serial clock with programmable polarity and phase
- Two separately enabled interrupts:
  - SPRF (SPI receiver full)
  - SPTE (SPI transmitter empty)
- Mode fault error flag with CPU interrupt capability
- Overflow error flag with CPU interrupt capability
- Programmable wired-OR mode

The following sources in the SPI status and control register can generate CPU interrupt requests:

- SPI receiver full bit (SPRF) — The SPRF bit becomes set every time a byte transfers from the shift register to the receive data register. If the SPI receiver interrupt enable bit, SPRIE, is also set, SPRF generates an SPI receiver/error CPU interrupt request.
- SPI transmitter empty (SPTE) — The SPTE bit becomes set every time a byte transfers from the transmit data register to the shift register. If the SPI transmit interrupt enable bit, SPTIE, is also set, SPTE generates an SPTE CPU interrupt request.

14.10 Resetting the SPI

Any system reset completely resets the SPI. Partial resets occur whenever the SPI enable bit (SPE) is low. Whenever SPE is low, the following occurs:

- The SPTE flag is set.
- Any transmission currently in progress is aborted.
- The shift register is cleared.
- The SPI state counter is cleared, making it ready for a new complete transmission.
- All the SPI port logic is defaulted back to being general-purpose I/O.

These items are reset only by a system reset:

- All control bits in the SPCR register
- All control bits in the SPSCR register (MODFEN, ERRIE, SPR1, and SPR0)
- The status flags SPRF, OVRF, and MODF

By not resetting the control bits when SPE is low, the user can clear SPE between transmissions without having to set all control bits again when SPE is set back high for the next transmission.

If the calling master does not return an acknowledge bit (MMRXAK = 1), the module will release the SDA line for master to generate a "stop" or "repeated start" condition. The data in the MMDTR will not be transferred to the output circuit until the next calling from a master. The transmit buffer empty flag remains cleared (MMTXBE = 0).

In master mode, the data in MMDTR will be transferred to the output circuit when:

- the module receives an acknowledge bit (MMRXAK = 0), after setting master transmit mode (MMRW = 0), and the calling address has been transmitted; or
- the previous data in the output circuit has be transmitted and the receiving slave returns an acknowledge bit, indicated by a received acknowledge bit (MMRXAK = 0).

If the slave does not return an acknowledge bit (MMRXAK = 1), the master will generate a "stop" or "repeated start" condition. The data in the MMDTR will not be transferred to the output circuit. The transmit buffer empty flag remains cleared (MMTXBE = 0).

The sequence of events for slave transmit and master transmit are illustrated in **Figure 15-8**.

15.5.6 Multi-Master IIC Data Receive Register (MMDRR)

Address: $006F

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	MMRD7	MMRD6	MMRD5	MMRD4	MMRD3	MMRD2	MMRD1	MMRD0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 15-7. Multi-Master IIC Data Receive Register (MMDRR)

When the MMIIC module is enabled, MMEN = 1, data in this read-only register depends on whether module is in master or slave mode.

Section 21. Computer Operating Properly (COP)

21.1 Contents

21.2 Introduction

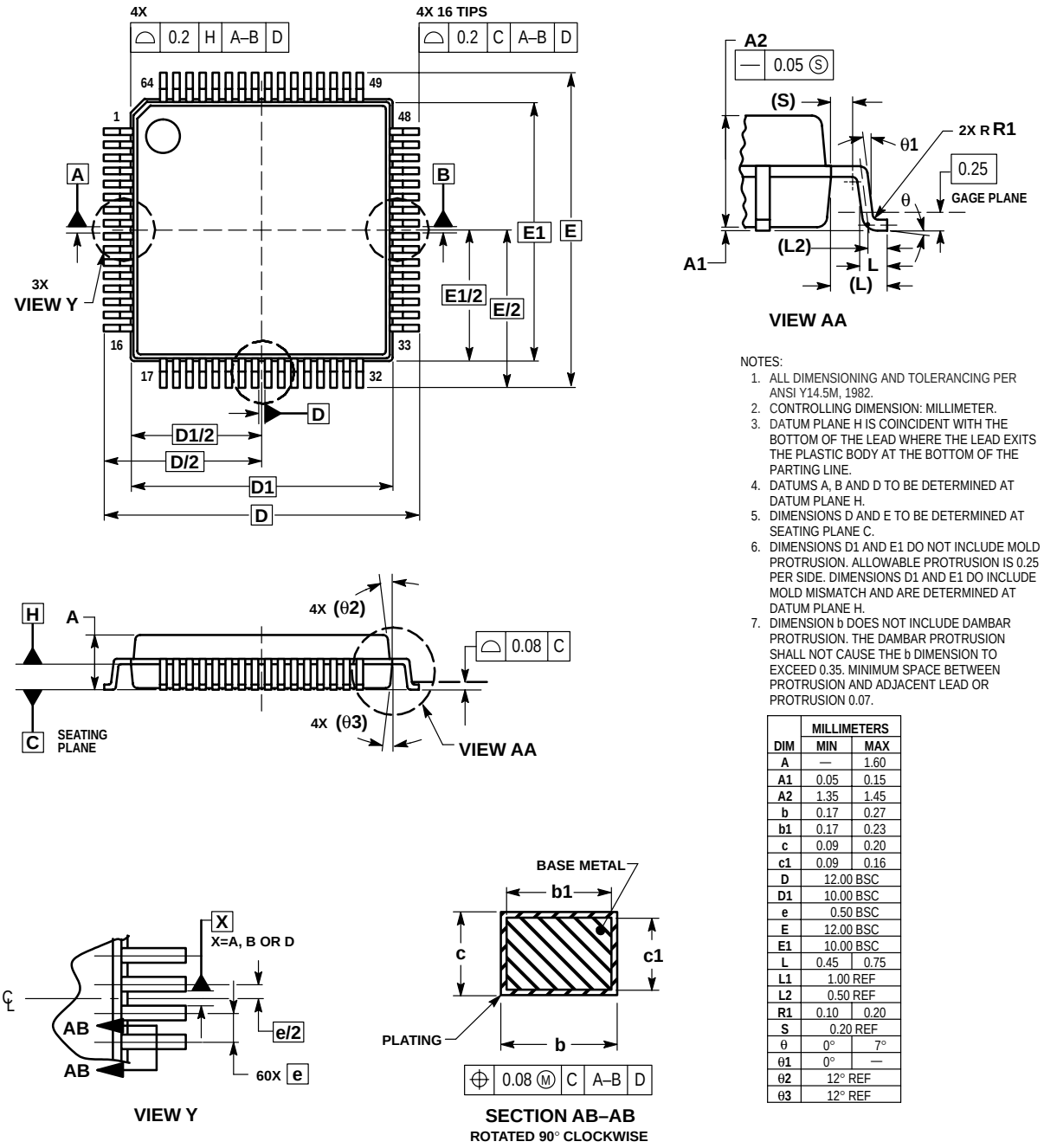
The computer operating properly (COP) module contains a free-running counter that generates a reset if allowed to overflow. The COP module helps software recover from runaway code. Prevent a COP reset by clearing the COP counter periodically. The COP module can be disabled through the COPD bit in the configuration register 1 (CONFIG1).

24.6 5V DC Electrical Characteristics

Table 24-4. 5V DC Electrical Characteristics

Characteristic[1]	Symbol	Min	Typ[2]	Max	Unit
Output high voltage (I_{LOAD} = –2.0 mA) All ports	V_{OH}	V_{DD}–0.8	—	—	V
Output low voltage (I_{LOAD} = 1.6mA) All ports (I_{LOAD} = 15.0 mA) PTB0–PTB5, PTC0–PTC7, PTE0–PTE7, PTF0–PTF7	V_{OL}	—	—	0.4	V
Input high voltage All ports, $\overline{RST}$, $\overline{IRQ}$, OSC1	V_{IH}	$0.7 \times V_{DD}$	—	V_{DD}	V
Input low voltage All ports, $\overline{RST}$, $\overline{IRQ}$, OSC1	V_{IL}	V_{SS}	—	$0.3 \times V_{DD}$	V
V_{DD} supply current					
Run[3], f_{OP} = 8 MHz					
with all modules on	I_{DD}	—	15	20	mA
with ADC on		—	13	18	mA
with ADC off		—	10.5	14	mA
Wait[4], f_{OP} = 8 MHz (all modules off)		—	5	8	mA
Stop, f_{OP} = 8 kHz[5]					
with OSC, RTC, LCD[6], LVI on		—	300	400	µA
with OSC, RTC, LCD[6] on		—	20	30	µA
with OSC, RTC on		—	7	12	µA
all modules off		—	—	1	µA
Digital I/O ports Hi-Z leakage current All ports, $\overline{RST}$	I_{IL}	—	—	± 10	µA
Input current $\overline{IRQ}$	I_{IN}	—	—	± 1	µA
Capacitance	C_{OUT}	—	—	12	pF
Ports (as input or output)	C_{IN}	—	—	8	
POR re-arm voltage[7]	V_{POR}	0	—	100	mV
POR rise-time ramp rate[8]	R_{POR}	0.035	—	—	V/ms
Monitor mode entry voltage (at $\overline{IRQ}$ pin)	V_{TST}	$1.5 \times V_{DD}$	—	8	V
Pullup resistors[9]					
PTA0–PTA3 and PTD4–PTD7 as KBI0–KBI7	R_{PU1}	21	30	39	kΩ
$\overline{RST}$, $\overline{IRQ}$	R_{PU2}	21	30	39	kΩ
Low-voltage inhibit, trip falling voltage	V_{TRIPF}	3.6	—	4.6	V
Low-voltage inhibit, trip rising voltage	V_{TRIPR}	3.7	—	4.7	V

25.3 64-Pin Low-Profile Quad Flat Pack (LQFP)



NOTES:
1. ALL DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
5. DIMENSIONS D AND E TO BE DETERMINED AT SEATING PLANE C.
6. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION SHALL NOT CAUSE THE b DIMENSION TO EXCEED 0.35. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07.

	MILLIMETERS	
DIM	MIN	MAX
A	—	1.60
A1	0.05	0.15
A2	1.35	1.45
b	0.17	0.27
b1	0.17	0.23
c	0.09	0.20
c1	0.09	0.16
D	12.00 BSC	
D1	10.00 BSC	
e	0.50 BSC	
E	12.00 BSC	
E1	10.00 BSC	
L	0.45	0.75
L1	1.00 REF	
L2	0.50 REF	
R1	0.10	0.20
S	0.20 REF	
θ	0°	7°
θ1	0°	—
θ2	12° REF	
θ3	12° REF	

Figure 25-1. 64-Pin Low-Profile Quad Flat Pack (Case No. 840F)