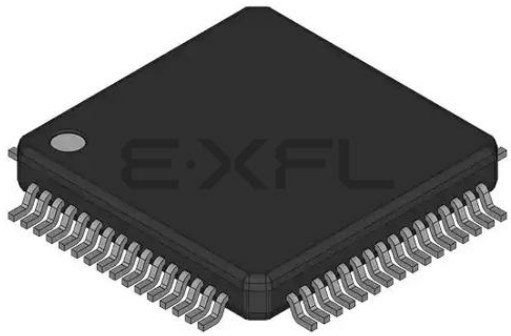

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	HC08
Core Size	8-Bit
Speed	8MHz
Connectivity	I²C, IRSCI, SPI
Peripherals	LCD, LVD, POR, PWM
Number of I/O	40
Program Memory Size	24KB (24K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 6x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-QFP
Supplier Device Package	64-QFP (14x14)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc908lj24cfuer

Table	Title	Page

1.2 Introduction

The MC68HC908LJ24 is a member of the low-cost, high-performance M68HC08 Family of 8-bit microcontroller units (MCUs). The M68HC08 Family is based on the customer-specified integrated circuit (CSIC) design strategy. All MCUs in the family use the enhanced M68HC08 central processor unit (CPU08) and are available with a variety of modules, memory sizes and types, and package types.

1.3 Features

Features of the MC68HC908LJ24 include the following:

- High-performance M68HC08 architecture
- Fully upward-compatible object code with M6805, M146805, and M68HC05 Families
  - 8-MHz at 5V operating voltage
  - 4-MHz at 3.3V operating voltage
- 32.768kHz crystal oscillator clock input with 32MHz internal PLL
- Optional continuous crystal oscillator operation in stop mode
- 24K-bytes user program FLASH memory with security[1] feature
- 768 bytes of on-chip RAM
- Up to 48 general-purpose input/output (I/O) pins:
  - High current 15mA sink capability on 30 pins
- Two 16-bit, 2-channel timer interface modules (TIM1 and TIM2) with selectable input capture, output compare, PWM capability on each channel, and external clock input option (T1CLK and T2CLK)
- Real time clock (RTC) with:
  - Clock, calendar, alarm, and chronograph functions
  - Selectable periodic interrupt requests for seconds, minutes, hours, days, 2-Hz, 4-Hz, 8-Hz, 16-Hz, and 128-Hz

1. No security feature is absolutely secure. However, Freescale strategy is to make reading or copying the FLASH difficult for unauthorized users.

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$0027	Timer 1 Channel 0 Register Low (T1CH0L)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
		Reset:	X	X	X	X	X	X	X	X
$0028	Timer 1 Channel 1 Status and Control Register (T1SC1)	Read:	CH1F	CH1IE	0	MS1A	ELS1B	ELS1A	TOV1	CH1MAX
		Write:	0							
		Reset:	0	0	0	0	0	0	0	0
$0029	Timer 1 Channel 1 Register High (T1CH1H)	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
		Reset:	X	X	X	X	X	X	X	X
$002A	Timer 1 Channel 1 Register Low (T1CH1L)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
		Reset:	X	X	X	X	X	X	X	X
$002B	Timer 2 Status and Control Register (T2SC)	Read:	TOF	TOIE	TSTOP	0	0	PS2	PS1	PS0
		Write:	0			TRST				
		Reset:	0	0	1	0	0	0	0	0
$002C	Timer 2 Counter Register High (T2CNTH)	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$002D	Timer 2 Counter Register Low (T2CNTL)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$002E	Timer 2 Counter Modulo Register High (T2MODH)	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
		Reset:	1	1	1	1	1	1	1	1
$002F	Timer 2 Counter Modulo Register Low (T2MODL)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
		Reset:	1	1	1	1	1	1	1	1
$0030	Timer 2 Channel 0 Status and Control Register (T2SC0)	Read:	CH0F	CH0IE	MS0B	MS0A	ELS0B	ELS0A	TOV0	CH0MAX
		Write:	0							
		Reset:	0	0	0	0	0	0	0	0

U = Unaffected X = Indeterminate = Unimplemented R = Reserved

Figure 2-2. Control, Status, and Data Registers (Sheet 5 of 13)

4.6 FLASH Mass Erase Operation

Use the following procedure to erase the entire FLASH memory:

1. Set both the ERASE bit and the MASS bit in the FLASH control register.
2. Read the FLASH block protect register.
3. Write any data to any FLASH address within the FLASH memory address range.
4. Wait for a time, t_{nvs} (10 µs).
5. Set the HVEN bit.
6. Wait for a time t_{merase} (4 ms).
7. Clear the ERASE bit.
8. Wait for a time, t_{nvh1} (100 µs).
9. Clear the HVEN bit.
10. After time, t_{rcv} (1 µs), the memory can be accessed again in read mode.

NOTE: *Programming and erasing of FLASH locations cannot be performed by code being executed from the FLASH memory; the code must be executed from RAM. While these operations must be performed in the order as shown, but other unrelated operations may occur between the steps.*

Table 6-1. Instruction Set Summary (Sheet 2 of 8)

Source Form	Operation	Description	Effect on CCR						Address Mode	Opcode	Operand	Cycles
			V	H	I	N	Z	C				
BCS *rel*	Branch if Carry Bit Set (Same as BLO)	PC ← (PC) + 2 + *rel* ? (C) = 1	–	–	–	–	–	–	REL	25	rr	3
BEQ *rel*	Branch if Equal	PC ← (PC) + 2 + *rel* ? (Z) = 1	–	–	–	–	–	–	REL	27	rr	3
BGE *opr*	Branch if Greater Than or Equal To (Signed Operands)	PC ← (PC) + 2 + *rel* ? (N ⊕ V) = 0	–	–	–	–	–	–	REL	90	rr	3
BGT *opr*	Branch if Greater Than (Signed Operands)	PC ← (PC) + 2 + *rel* ? (Z) | (N ⊕ V) = 0	–	–	–	–	–	–	REL	92	rr	3
BHCC *rel*	Branch if Half Carry Bit Clear	PC ← (PC) + 2 + *rel* ? (H) = 0	–	–	–	–	–	–	REL	28	rr	3
BHCS *rel*	Branch if Half Carry Bit Set	PC ← (PC) + 2 + *rel* ? (H) = 1	–	–	–	–	–	–	REL	29	rr	3
BHI *rel*	Branch if Higher	PC ← (PC) + 2 + *rel* ? (C) | (Z) = 0	–	–	–	–	–	–	REL	22	rr	3
BHS *rel*	Branch if Higher or Same (Same as BCC)	PC ← (PC) + 2 + *rel* ? (C) = 0	–	–	–	–	–	–	REL	24	rr	3
BIH *rel*	Branch if $\overline{\text{IRQ}}$ Pin High	PC ← (PC) + 2 + *rel* ? $\overline{\text{IRQ}}$ = 1	–	–	–	–	–	–	REL	2F	rr	3
BIL *rel*	Branch if $\overline{\text{IRQ}}$ Pin Low	PC ← (PC) + 2 + *rel* ? $\overline{\text{IRQ}}$ = 0	–	–	–	–	–	–	REL	2E	rr	3
BIT #*opr* BIT *opr* BIT *opr* BIT *opr*,X BIT *opr*,X BIT ,X BIT *opr*,SP BIT *opr*,SP	Bit Test	(A) & (M)	0	–	–	↕	↕	–	IMM DIR EXT IX2 IX1 IX SP1 SP2	A5 B5 C5 D5 E5 F5 9EE5 9ED5	ii dd hh ll ee ff ff ff ee ff	2 3 4 4 3 2 4 5
BLE *opr*	Branch if Less Than or Equal To (Signed Operands)	PC ← (PC) + 2 + *rel* ? (Z) | (N ⊕ V) = 1	–	–	–	–	–	–	REL	93	rr	3
BLO *rel*	Branch if Lower (Same as BCS)	PC ← (PC) + 2 + *rel* ? (C) = 1	–	–	–	–	–	–	REL	25	rr	3
BLS *rel*	Branch if Lower or Same	PC ← (PC) + 2 + *rel* ? (C) | (Z) = 1	–	–	–	–	–	–	REL	23	rr	3
BLT *opr*	Branch if Less Than (Signed Operands)	PC ← (PC) + 2 + *rel* ? (N ⊕ V) =1	–	–	–	–	–	–	REL	91	rr	3
BMC *rel*	Branch if Interrupt Mask Clear	PC ← (PC) + 2 + *rel* ? (I) = 0	–	–	–	–	–	–	REL	2C	rr	3
BMI *rel*	Branch if Minus	PC ← (PC) + 2 + *rel* ? (N) = 1	–	–	–	–	–	–	REL	2B	rr	3
BMS *rel*	Branch if Interrupt Mask Set	PC ← (PC) + 2 + *rel* ? (I) = 1	–	–	–	–	–	–	REL	2D	rr	3
BNE *rel*	Branch if Not Equal	PC ← (PC) + 2 + *rel* ? (Z) = 0	–	–	–	–	–	–	REL	26	rr	3
BPL *rel*	Branch if Plus	PC ← (PC) + 2 + *rel* ? (N) = 0	–	–	–	–	–	–	REL	2A	rr	3
BRA *rel*	Branch Always	PC ← (PC) + 2 + *rel*	–	–	–	–	–	–	REL	20	rr	3

9.3.3 Clocks in Stop Mode and Wait Mode

Upon exit from stop mode by an interrupt, break, or reset, the SIM allows ICLK to clock the SIM counter. The CPU and peripheral clocks do not become active until after the stop delay timeout. This timeout is selectable as 4096 or 32 ICLK cycles. (See **9.7.2 Stop Mode**.)

In wait mode, the CPU clocks are inactive. The SIM also produces two sets of clocks for other modules. Refer to the wait mode subsection of each module to see if the module is active or inactive in wait mode. Some modules can be programmed to be active in wait mode.

9.4 Reset and System Initialization

The MCU has these reset sources:

- Power-on reset module (POR)
- External reset pin ($\overline{\text{RST}}$)
- Computer operating properly module (COP)
- Low-voltage inhibit module (LVI)
- Illegal opcode
- Illegal address

All of these resets produce the vector $FFFE:$FFFF ($FEFE:$FEFF in monitor mode) and assert the internal reset signal (IRST). IRST causes all registers to be returned to their default values and all modules to be returned to their reset states.

An internal reset clears the SIM counter (see **9.5 SIM Counter**), but an external reset does not. Each of the resets sets a corresponding bit in the SIM reset status register (SRSR). (See **9.8 SIM Registers**.)

Table 10-3 lists external frequencies required to achieve a standard baud rate of 9600 BPS. Other standard baud rates can be accomplished using proportionally higher or lower frequency generators. If using a crystal as the clock source, be aware of the upper frequency limit that the internal clock module can handle.

Table 10-3. Monitor Baud Rate Selection

External Frequency	$\overline{\text{IRQ}}$	PTC1	Internal Frequency	Baud Rate (BPS)
4.9152 MHz	V_{TST}	0	2.4576 MHz	9600
9.8304 MHz	V_{TST}	1	2.4576 MHz	9600
9.8304 MHz	V_{DD}	X	2.4576 MHz	9600
32.768 kHz	V_{SS}	X	2.4576 MHz	9600

10.4.5 Commands

The monitor ROM firmware uses these commands:

- READ (read memory)
- WRITE (write memory)
- IREAD (indexed read)
- IWRITE (indexed write)
- READSP (read stack pointer)
- RUN (run user program)

The monitor ROM firmware echoes each received byte back to the PTA0 pin for error checking. An 11-bit delay at the end of each command allows the host to send a break character to cancel the command. A delay of two bit times occurs before each echo and before READ, IREAD, or READSP data is returned. The data returned by a read command appears after the echo of the last byte of the command.

NOTE: *Wait one bit time after each echo before sending the next byte.*

NOTE: *The EE_READ routine is unable to check for incorrect data blocks, such as the FLASH page boundary address and data size. It is the responsibility of the user to ensure the starting address indicated in the data block is at the FLASH page boundary and the data size is 2 to 15. If the FLASH page is programmed with a data array with a different size, the EE_READ call will be ignored.*

12.4 I/O Pins

Two RTC clock calibration pins are shared with standard port I/O pins.

Table 12-1. Pin Name Conventions

RTC Generic Pin Name	Full MCU Pin Name	Pin Selected for RTC Function by Bits in RTCCOMR ($0040)
CALIN	PTD0/$\overline{SS}$/CALIN	AUTOCAL
CALOUT	PTD3/SPSCK/CALOUT(1)	OUTF[1:0}

Notes:
1. Do not enable the SPI function if the pin is used for RTC calibration.

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$0040	RTC Calibration Control Register (RTCCOMR)	Read:	0	0	CAL	AUTOCAL	OUTF1	OUTF0	0	0
		Write:	R	R					RTCWE1	RTCWE0
		Reset:	0	0	0	0	0	0	0	0
$0041	RTC Calibration Data Register (RTCCDAT)	Read:	EOVL	0	E5	E4	E3	E2	E1	E0
		Write:								
		Reset:	U	0	U	U	U	U	U	U
$0042	RTC Control Register 1 (RTCCR1)	Read:	ALMIE	CHRIE	DAYIE	HRIE	MINIE	SECIE	TB1IE	TB2IE
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$0043	RTC Control Register 2 (RTCCR2)	Read:	COMEN	0	CHRE	RTCE	TBH	0	0	0
		Write:		CHRCLR						
		Reset:	U	0	0	0††	0	0	0	0
$0044	RTC Status Register (RTCSR)	Read:	ALMF	CHRF	DAYF	HRF	MINF	SECF	TB1F	TB2F
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$0045	Alarm Minute Register (ALMR)	Read:	0	0	AM5	AM4	AM3	AM2	AM1	AM0
		Write:								
		Reset:	0	0	U	U	U	U	U	U

†† Reset by POR only.

U = Unaffected = Unimplemented R = Reserved

Figure 12-1. RTC I/O Register Summary

SECIE — Second Interrupt Enable

This read/write bit enables the second flag, SECF, to generate CPU interrupt requests. Reset clears the SECIE bit.

1 = SECF enabled to generate CPU interrupt
0 = SECF not enabled to generate CPU interrupt

TB1IE — Timebase 1 Interrupt Enable

This read/write bit enables the timebase1 flag, TB1F, to generate CPU interrupt requests. Reset clears the TB1IE bit.

1 = TB1F enabled to generate CPU interrupt
0 = TB1F not enabled to generate CPU interrupt

TB2IE — Timebase 2 Interrupt Enable

This read/write bit enables the timebase2 flag, TB2F, to generate CPU interrupt requests. Reset clears the TB2IE bit.

1 = TB2F enabled to generate CPU interrupt
0 = TB2F not enabled to generate CPU interrupt

12.10.4 RTC Control Register 2 (RTCCR2)

The RTC control register 2 (RTCCR2) contains control and clock selection bits for RTC operation.

Address: $0043

Read:	COMEN*	0	CHRE	RTCE*	TBH	0	0	0
Write:		CHRCLR						
Reset:	U	0	0	0††	0	0	0	0

= Unimplemented

†† Reset by POR only.
* COMEN and RTCE bits are write-protected; unprotect by a write sequence to RTCWE[1:0] in RTCCOMR.

Figure 12-9. RTC Control Register 2 (RTCCR2)

COMEN — RTC Compensation Enable

This read/write bit enables the clock compensation mechanism for CGMXCLK frequency errors. Reset has no effect on COMEN bit.

1 = Compensation mechanism enabled
0 = Compensation mechanism not enabled

13.3 Features

Features of the SCI module include the following:

- Full duplex operation
- Standard mark/space non-return-to-zero (NRZ) format
- Programmable 8-bit or 9-bit character length
- Separately enabled transmitter and receiver
- Separate receiver and transmitter CPU interrupt requests
- Two receiver wakeup methods:
  - Idle line wakeup
  - Address mark wakeup
- Interrupt-driven operation with eight interrupt flags:
  - Transmitter empty
  - Transmission complete
  - Receiver full
  - Idle receiver input
  - Receiver overrun
  - Noise error
  - Framing error
  - Parity error
- Receiver framing error detection
- Hardware parity checking
- 1/16 bit-time noise detection

Features of the infrared (IR) sub-module include the following:

- IR sub-module enable/disable for infrared SCI or conventional SCI on TxD and RxD pins
- Software selectable infrared modulation/demodulation (3/16, 1/16 or 1/32 width pulses)

When an SPI is configured as a master, the $\overline{SS}$ input can be used in conjunction with the MODF flag to prevent multiple masters from driving MOSI and SPSCK. (See **14.8.2 Mode Fault Error**.) For the state of the $\overline{SS}$ pin to set the MODF flag, the MODFEN bit in the SPSCK register must be set. If the MODFEN bit is low for an SPI master, the $\overline{SS}$ pin can be used as a general-purpose I/O under the control of the data direction register of the shared I/O port. With MODFEN high, it is an input-only pin to the SPI regardless of the state of the data direction register of the shared I/O port.

The CPU can always read the state of the $\overline{SS}$ pin by configuring the appropriate pin as an input and reading the port data register. (See **Table 14-3**.)

Table 14-3. SPI Configuration

SPE	SPMSTR	MODFEN	SPI Configuration	State of $\overline{SS}$ Logic
0	X(1)	X	Not enabled	General-purpose I/O; $\overline{SS}$ ignored by SPI
1	0	X	Slave	Input-only to SPI
1	1	0	Master without MODF	General-purpose I/O; $\overline{SS}$ ignored by SPI
1	1	1	Master with MODF	Input-only to SPI

Note 1. X = Don’t care

14.13.5 CGND (Clock Ground)

CGND is the ground return for the serial clock pin, SPSCK, and the ground for the port output buffers. It is internally connected to V_{SS} as shown in **Table 14-1**.

Section 15. Multi-Master IIC Interface (MMIIC)

15.1 Contents

15.2 Introduction

This Multi-master IIC (MMIIC) Interface is designed for internal serial communication between the MCU and other IIC devices. A hardware circuit generates "start" and "stop" signal, while byte by byte data transfer is interrupt driven by the software algorithm. Therefore, it can greatly help the software in dealing with other devices to have higher system efficiency in a typical digital monitor system.

This module not only can be applied in internal communications, but can also be used as a typical command reception serial bus for factory setup and alignment purposes. It also provides the flexibility of hooking additional devices to an existing system for future expansion without adding extra hardware.

If the external clock (CGMXCLK) is equal to or greater than 1MHz, CGMXCLK can be used as the clock source for the ADC. If CGMXCLK is less than 1MHz, use the PLL-generated bus clock as the clock source. As long as the internal ADC clock is at f_{ADIC}, correct operation can be guaranteed.

1 = Internal bus clock
0 = External clock, CGMXCLK

$$f_{ADIC} = \frac{\text{CGMXCLK or bus frequency}}{\text{ADIV[2:0]}}$$

MODE1 and MODE0 — Modes of Result Justification

MODE1 and MODE0 selects between four modes of operation. The manner in which the ADC conversion results will be placed in the ADC data registers is controlled by these modes of operation. Reset returns right-justified mode.

Table 16-3. ADC Mode Select

MODE1	MODE0	ADC Clock Rate
0	0	8-bit truncated mode
0	1	Right justified mode
1	0	Left justified mode
1	1	Left justified sign data mode

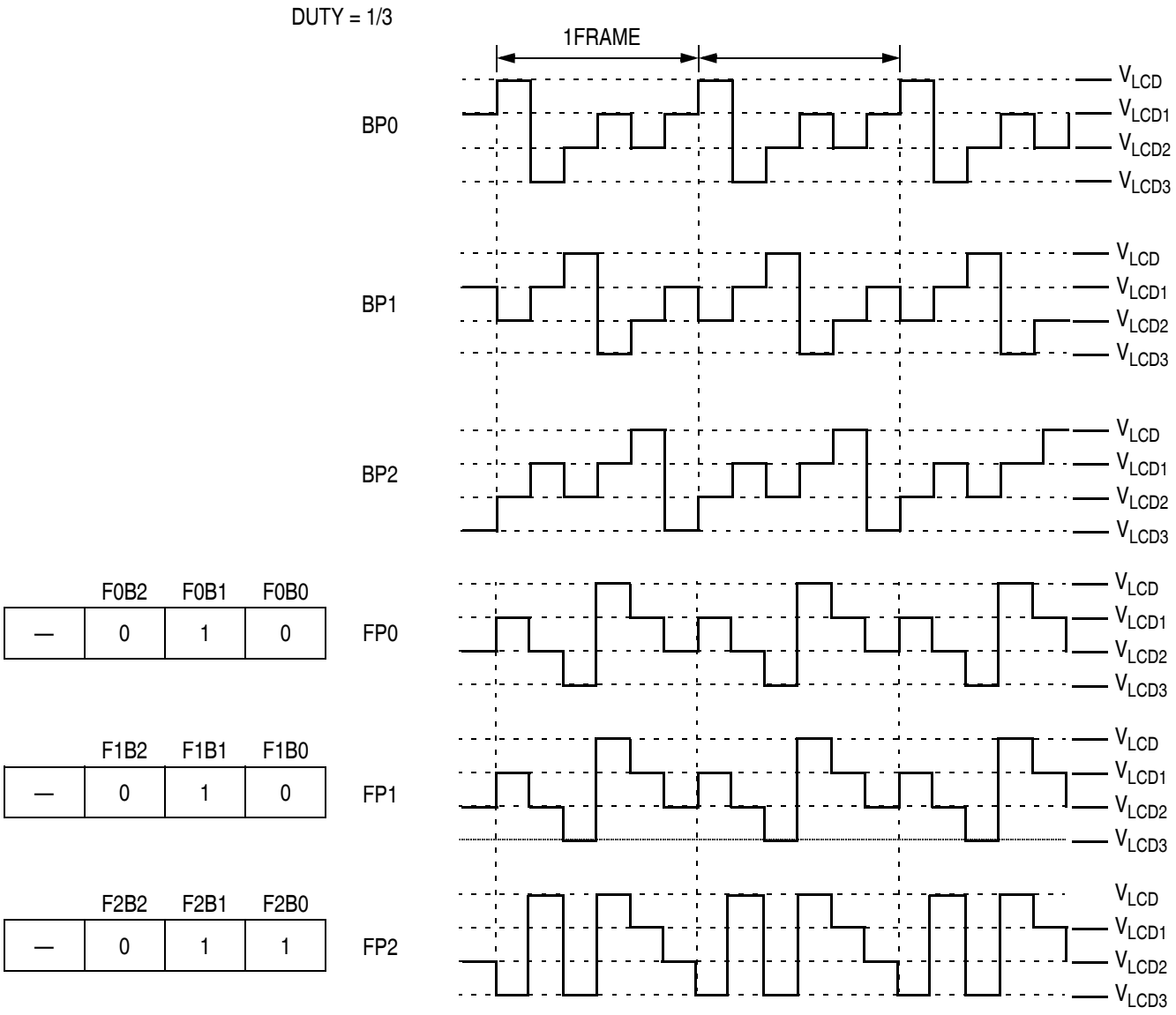


Figure 17-13. BP0–BP2 and FP0–FP2 Output Waveforms for 7-Segment Display Example

19.4.1 $\overline{\text{IRQ}}$ Pin

A logic 0 on the $\overline{\text{IRQ}}$ pin can latch an interrupt request into the IRQ latch. A vector fetch, software clear, or reset clears the IRQ latch.

If the MODE bit is set, the $\overline{\text{IRQ}}$ pin is both falling-edge-sensitive and low-level-sensitive. With MODE set, both of the following actions must occur to clear IRQ:

- Vector fetch or software clear — A vector fetch generates an interrupt acknowledge signal to clear the latch. Software may generate the interrupt acknowledge signal by writing a logic 1 to the ACK bit in the interrupt status and control register (INTSCR). The ACK bit is useful in applications that poll the $\overline{\text{IRQ}}$ pin and require software to clear the IRQ latch. Writing to the ACK bit prior to leaving an interrupt service routine can also prevent spurious interrupts due to noise. Setting ACK does not affect subsequent transitions on the $\overline{\text{IRQ}}$ pin. A falling edge that occurs after writing to the ACK bit latches another interrupt request. If the IRQ mask bit, IMASK, is clear, the CPU loads the program counter with the vector address at locations $FFFA and $FFFB.
- Return of the $\overline{\text{IRQ}}$ pin to logic 1 — As long as the $\overline{\text{IRQ}}$ pin is at logic 0, IRQ remains active.

The vector fetch or software clear and the return of the $\overline{\text{IRQ}}$ pin to logic 1 may occur in any order. The interrupt request remains pending as long as the $\overline{\text{IRQ}}$ pin is at logic 0. A reset will clear the latch and the MODE control bit, thereby clearing the interrupt even if the pin stays low.

If the MODE bit is clear, the $\overline{\text{IRQ}}$ pin is falling-edge-sensitive only. With MODE clear, a vector fetch or software clear immediately clears the IRQ latch.

The IRQF bit in the INTSCR register can be used to check for pending interrupts. The IRQF bit is not affected by the IMASK bit, which makes it useful in applications where polling is preferred.

Use the BIH of BIL instruction to read the logic level on the $\overline{\text{IRQ}}$ pin.

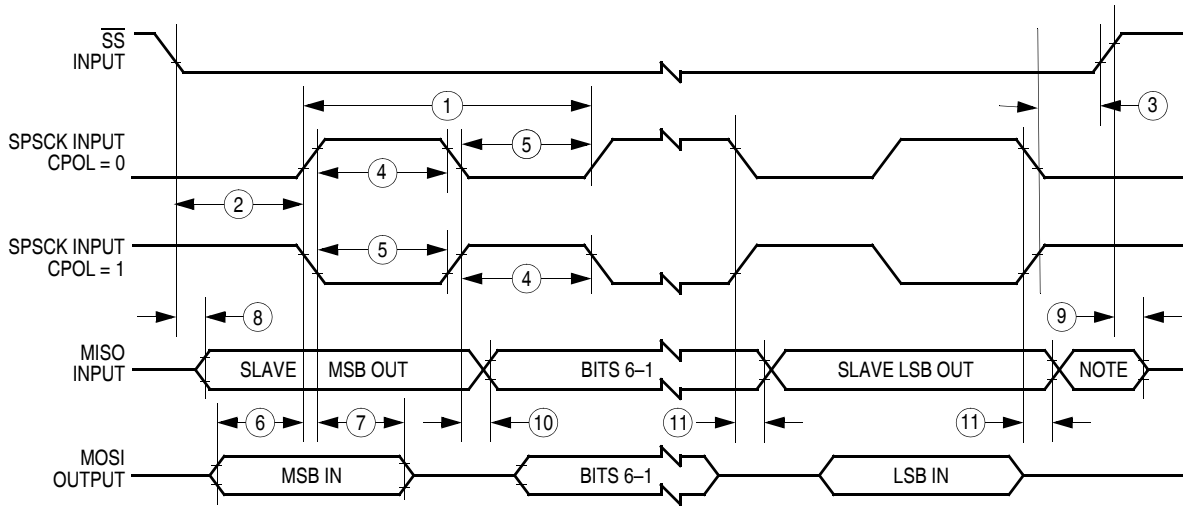
NOTE: *When using the level-sensitive interrupt trigger, avoid false interrupts by masking interrupt requests in the interrupt routine.*

Section 24. Electrical Specifications

24.1 Contents

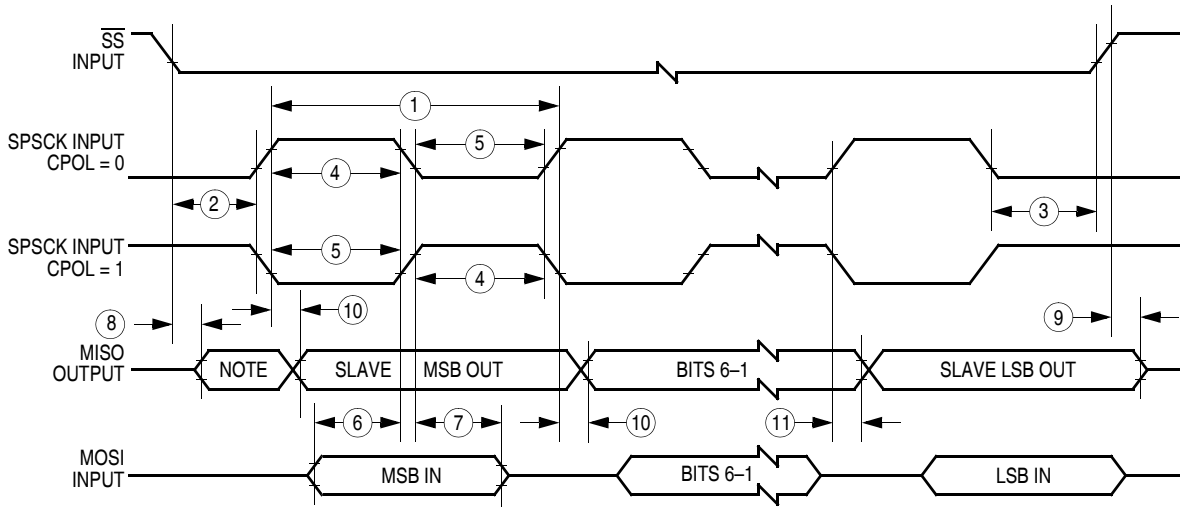
24.2 Introduction

This section contains electrical and timing specifications.



Note: Not defined but normally MSB of character just received

a) SPI Slave Timing (CPHA = 0)



Note: Not defined but normally LSB of character previously transmitted

b) SPI Slave Timing (CPHA = 1)

Figure 24-3. SPI Slave Timing

Section 26. Ordering Information

26.1 Contents

26.2 Introduction

This section contains ordering numbers for the MC68HC908LJ24.

26.3 MC Order Numbers

Table 26-1. MC Order Numbers

MC Order Number	Package	Operating Temperature Range
MC68HC908LJ24CPB	64-pin LQFP	–40 to +85 °C
MC68HC908LJ24CFU	64-pin QFP	–40 to +85 °C
MC68HC908LJ24CPK	80-pin LQFP	–40 to +85 °C
MC68HC908LJ24CFQ	80-pin QFP	–40 to +85 °C