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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HC08
Core Size	8-Bit
Speed	8MHz
Connectivity	I²C, IRSCI, SPI
Peripherals	LCD, LVD, POR, PWM
Number of I/O	40
Program Memory Size	24KB (24K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 6x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc908lj24cpbe

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$FE08	FLASH Control Register (FLCR)	Read:	0	0	0	0	HVEN	MASS	ERASE	PGM
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$FFCF	FLASH Block Protect Register (FLBPR)#	Read:	BPR7	BPR6	BPR5	BPR4	BPR3	BPR2	BPR1	BPR0
		Write:								
		Reset:	Unaffected by reset; $FF when blank							

Non-volatile FLASH register; write by programming.

= Unimplemented

Figure 4-1. FLASH I/O Register Summary

4.3 Functional Description

The FLASH memory consists of an array of 24,576 bytes for user memory plus a block of 48 bytes for user interrupt vectors. *An erased bit reads as logic 1 and a programmed bit reads as a logic 0*. The FLASH memory page size is defined as 128 bytes, and is the minimum size that can be erased in a page erase operation. Program and erase operations are facilitated through control bits in FLASH control register (FLCR). The address ranges for the FLASH memory are:

- $9000–$EFFF; user memory, 24,576 bytes
- $FFD0–$FFFF; user interrupt vectors, 48 bytes

Programming tools are available from Freescale. Contact your local Freescale representative for more information.

NOTE: *A security feature prevents viewing of the FLASH contents.*[1]

1. No security feature is absolutely secure. However, Freescale's strategy is to make reading or copying the FLASH difficult for unauthorized users.

Section 6. Central Processor Unit (CPU)

6.1 Contents

The reference clock for the CGM, real time clock module (RTC) and other MCU sub-systems is driven by the crystal oscillator. The COP module is always driven by internal RC clock.

The internal RC oscillator runs continuously after a POR or reset and is always available in run and wait modes. In stop mode, it can be disabled by setting the STOP_IRCDIS bit in CONFIG2 register.
Figure 7-1. shows the block diagram of the oscillator module.

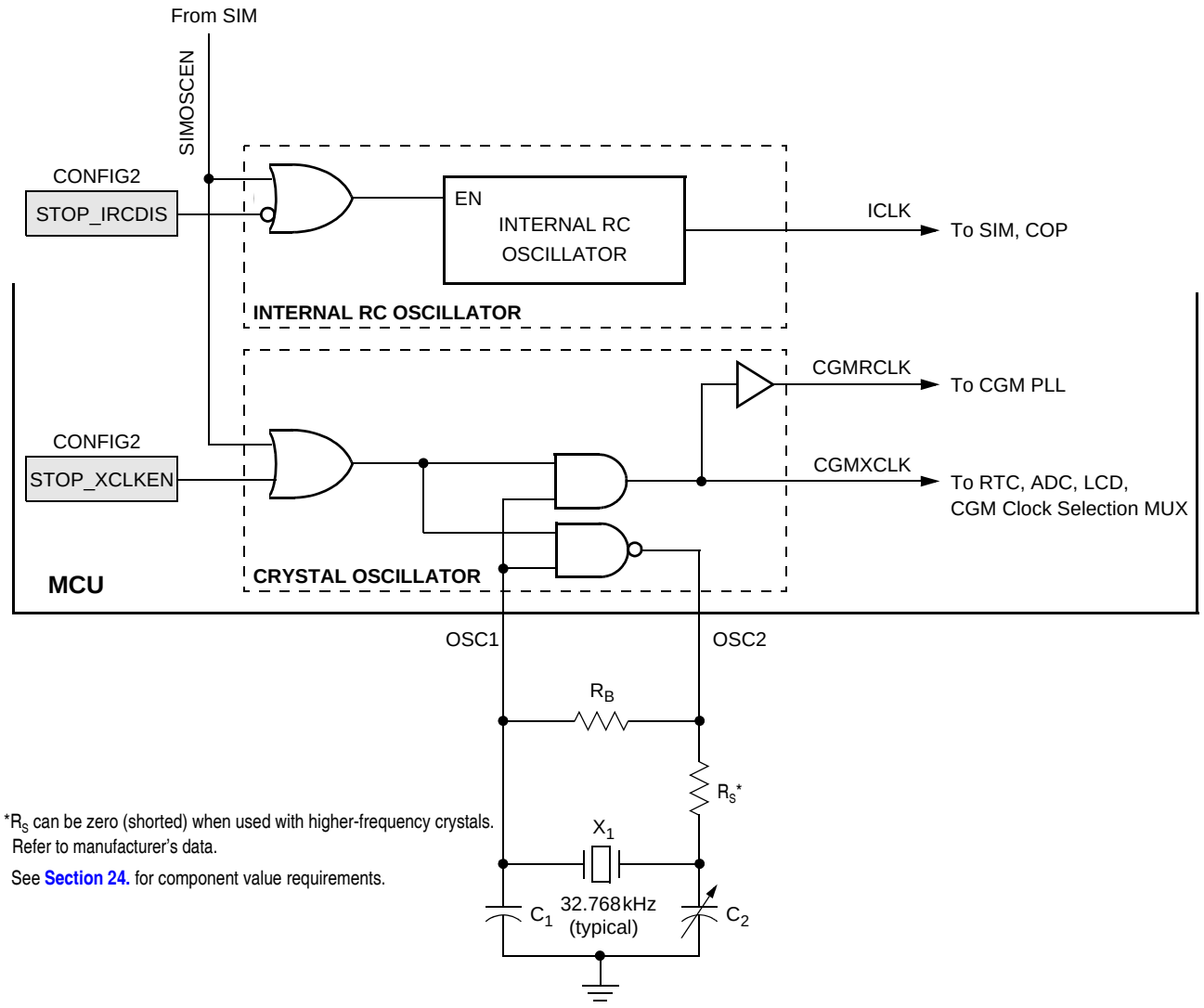


Figure 7-1. Oscillator Module Block Diagram

8.9.3 Choosing a Filter

As described in **8.9.2 Parametric Influences on Reaction Time**, the external filter network is critical to the stability and reaction time of the PLL. The PLL is also dependent on reference frequency and supply voltage.

Either of the filter networks in **Figure 8-10** is recommended when using a 32.768kHz reference clock (CGMRCLK). **Figure 8-10 (a)** is used for applications requiring better stability. **Figure 8-10 (b)** is used in low-cost applications where stability is not critical.

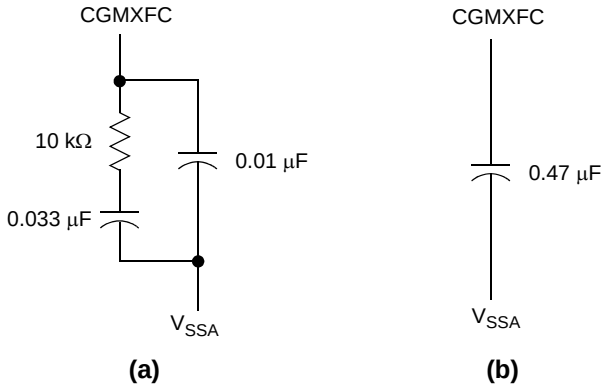
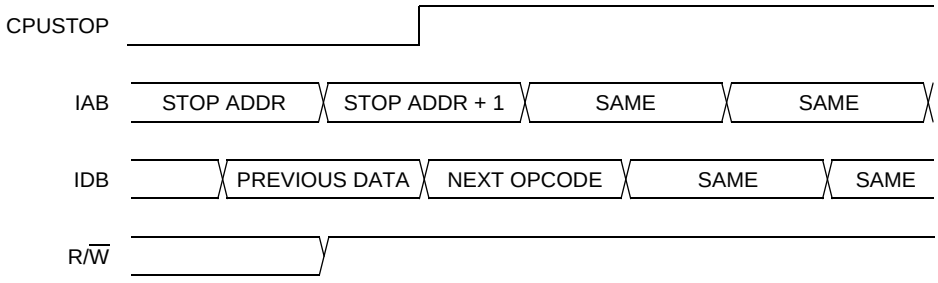


Figure 8-10. PLL Filter

A break interrupt during stop mode sets the SIM break stop/wait bit (SBSW) in the SIM break status register (SBSR).

The SIM counter is held in reset from the execution of the STOP instruction until the beginning of stop recovery. It is then used to time the recovery period. **Figure 9-18** shows stop mode entry timing.

NOTE: *To minimize stop current, all pins configured as inputs should be driven to a logic 1 or logic 0.*



NOTE: Previous data can be operand data or the STOP opcode, depending on the last instruction.

Figure 9-18. Stop Mode Entry Timing

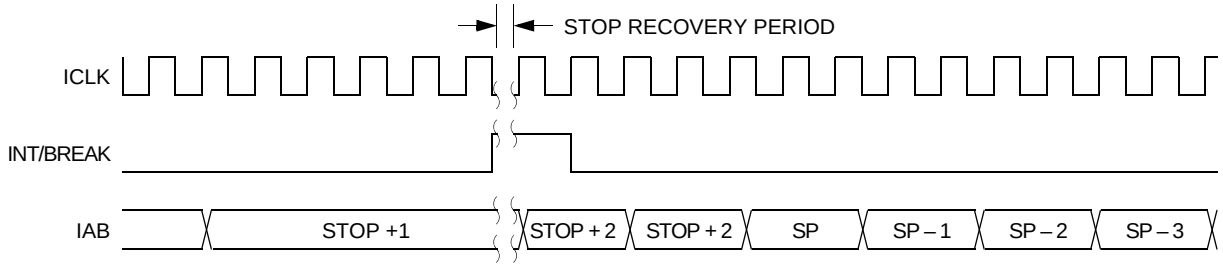


Figure 9-19. Stop Mode Recovery from Interrupt or Break

9.8 SIM Registers

The SIM has three memory-mapped registers:

- SIM Break Status Register (SBSR) — $FE00
- SIM Reset Status Register (SRSR) — $FE01
- SIM Break Flag Control Register (SBFCR) — $FE03

10.4.2 Data Format

Communication with the monitor ROM is in standard non-return-to-zero (NRZ) mark/space data format. Transmit and receive baud rates must be identical.

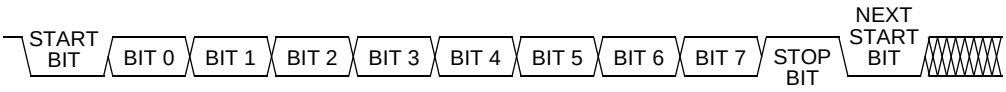


Figure 10-3. Monitor Data Format

10.4.3 Break Signal

A start bit (logic 0) followed by nine logic 0 bits is a break signal. When the monitor receives a break signal, it drives the PTA0 pin high for the duration of two bits and then echoes back the break signal.

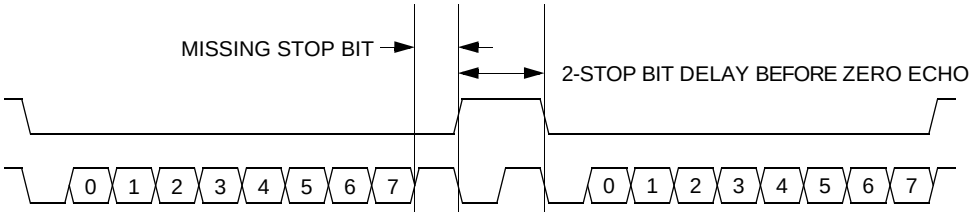


Figure 10-4. Break Transaction

10.4.4 Baud Rate

The communication baud rate is controlled by the crystal frequency and the state of the PTC1 pin (when $\overline{IRQ}$ is set to V_{TST}) upon entry into monitor mode. When PTC1 is high, the divide by ratio is 1024. If the PTC1 pin is at logic 0 upon entry into monitor mode, the divide by ratio is 512.

If monitor mode was entered with V_{DD} on $\overline{IRQ}$, then the divide by ratio is set at 1024, regardless of PTC1. If monitor mode was entered with V_{SS} on $\overline{IRQ}$, then the internal PLL steps up the external frequency, presumed to be 32.768 kHz, to 2.4576 MHz. These latter two conditions for monitor mode entry require that the reset vector is blank.

12.5 Functional Description

The RTC module provides clock indications in seconds, minutes, and hours; calendar indications in day-of-week, day-of-month, month, and year; with automatic adjustment for month and leap year. Reading the clock and calendar registers return the current time and date. Writing to these registers set the time and date, and the counters will continue to count from the new settings.

The alarm interrupt is set for the hour and minute. When the hour and minute counters matches the time set in the alarm hour and minute registers, the alarm flag is set. The alarm can be configured to generate a CPU interrupt request.

A 1/100 seconds chronograph counter is provided for timing applications. This counter can be independently enabled or disabled, and cleared at any time.

RTC module interrupts include the alarm interrupt and seven periodic interrupts from the clock and chronograph counters.

A frequency compensation mechanism is built into this RTC module to allow adjustments made to the RTC clock when a less accurate 32.768 kHz crystal is used.

The 1-Hz clock that drives the clock and calendar could make use of the built-in compensation mechanism for crystal frequency error compensation so that the 1-Hz clock could be made more accurate than the frequency accuracy of the crystal that drive the module. The compensation value can be provided by application software or acquire automatically during calibration operation of the module.

Figure 12-2 shows the structure of the RTC module.

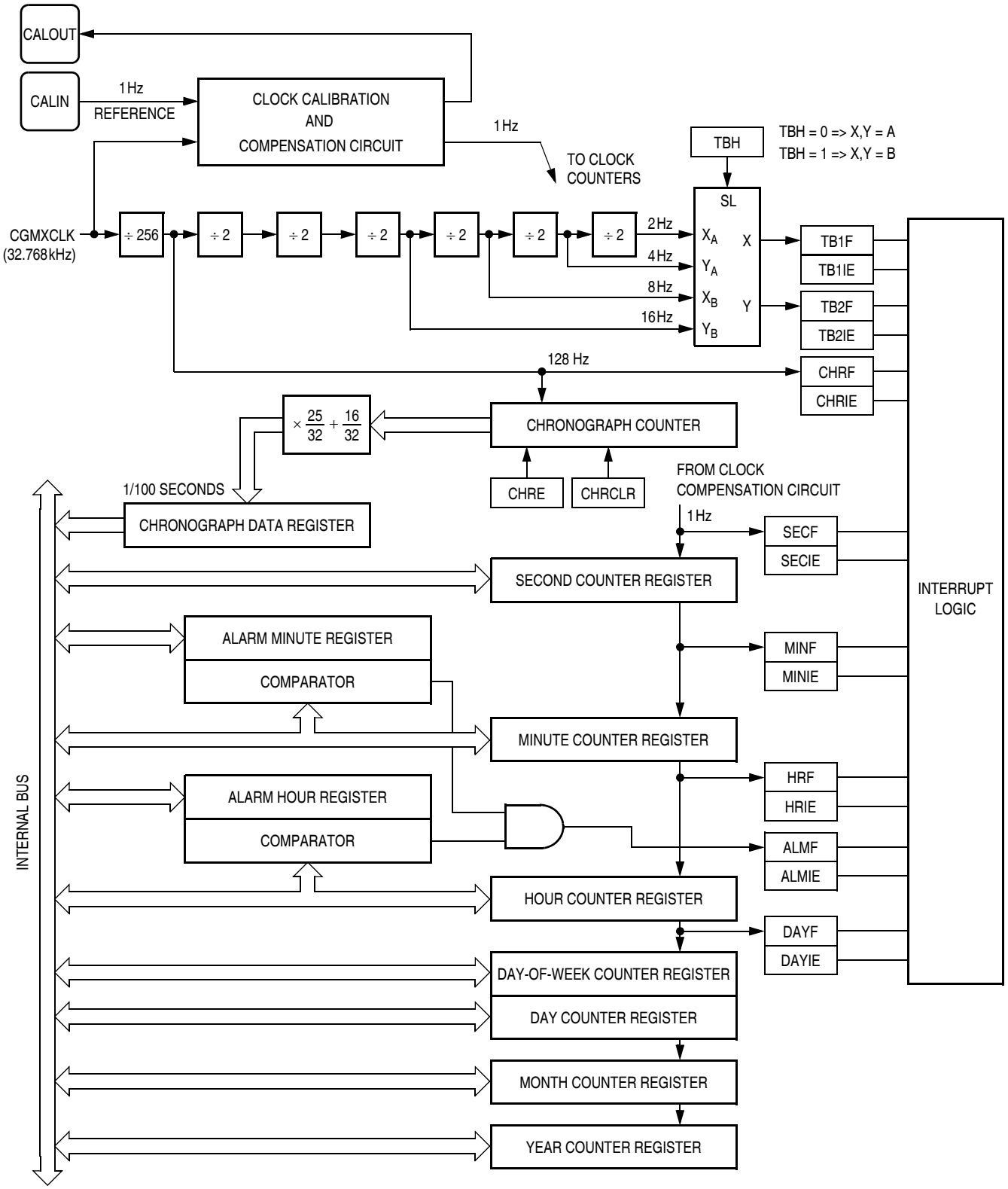


Figure 12-2. RTC Block Diagram

The infrared sub-module receives two clock sources from the SCI module: SCI_R16XCLK and SCI_R32XCLK. Both reference clocks are used to generate the narrow pulses during data transmission.
The SCI_R16XCLK and SCI_R32XCLK are internal clocks with frequencies that are 16 and 32 times the baud rate respectively. Both SCI_R16XCLK and SCI_R32XCLK clocks are used for transmitting data. The SCI_R16XCLK clock is used only for receiving data.

NOTE: *For proper SCI function (transmit or receive), the bus clock MUST be programmed to at least 32 times that of the selected baud rate.*
When the infrared sub-module is disabled, signals on the TxD and RxD pins pass through unchanged to the SCI module.

13.6 Infrared Functional Description

Figure 13-3 shows the structure of the infrared sub-module.

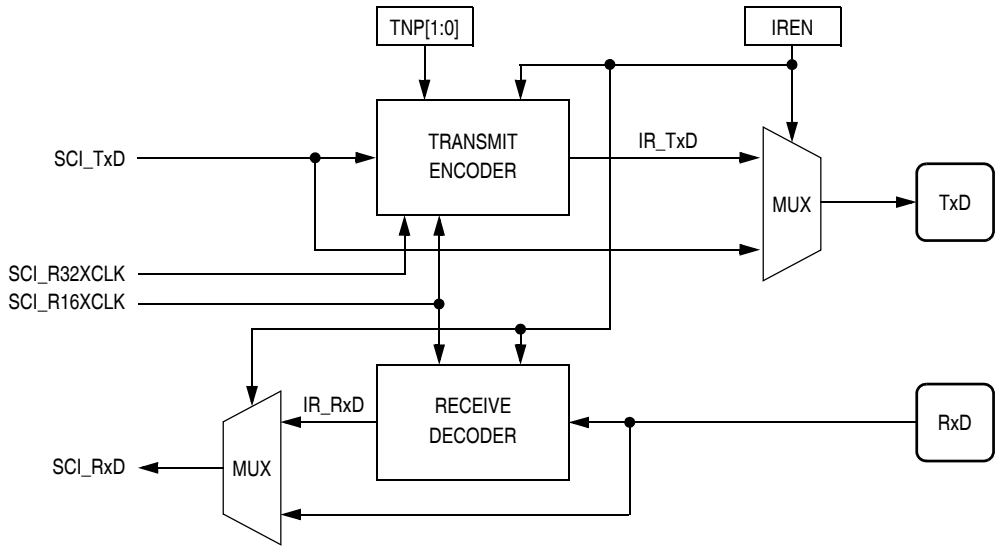


Figure 13-3. Infrared Sub-Module Diagram

The infrared sub-module provides the capability of transmitting narrow pulses to an infrared LED and receiving narrow pulses and transforming them to serial bits, which are sent to the SCI module. The infrared sub-module receives two clocks from the SCI. One of these two clocks is selected as the base clock to generate the 3/16, 1/16, or 1/32 bit width narrow pulses during transmission.

The SPR1 and SPR0 bits control the baud rate generator and determine the speed of the shift register. (See **14.14.2 SPI Status and Control Register**.) Through the SPSCK pin, the baud rate generator of the master also controls the shift register of the slave peripheral.

As the byte shifts out on the MOSI pin of the master, another byte shifts in from the slave on the master's MISO pin. The transmission ends when the receiver full bit, SPRF, becomes set. At the same time that SPRF becomes set, the byte from the slave transfers to the receive data register. In normal operation, SPRF signals the end of a transmission. Software clears SPRF by reading the SPI status and control register with SPRF set and then reading the SPI data register. Writing to the SPI data register clears the SPTE bit.

14.5.2 Slave Mode

The SPI operates in slave mode when the SPMSTR bit is clear. In slave mode, the SPSCK pin is the input for the serial clock from the master MCU. Before a data transmission occurs, the $\overline{SS}$ pin of the slave SPI must be at logic 0. $\overline{SS}$ must remain low until the transmission is complete. (See **14.8.2 Mode Fault Error**.)

In a slave SPI module, data enters the shift register under the control of the serial clock from the master SPI module. After a byte enters the shift register of a slave SPI, it transfers to the receive data register, and the SPRF bit is set. To prevent an overflow condition, slave software then must read the receive data register before another full byte enters the shift register.

The maximum frequency of the SPSCK for an SPI configured as a slave is the bus clock speed (which is twice as fast as the fastest master SPSCK clock that can be generated). The frequency of the SPSCK for an SPI configured as a slave does not have to correspond to any SPI baud rate. The baud rate only controls the speed of the SPSCK generated by an SPI configured as a master. Therefore, the frequency of the SPSCK for an SPI configured as a slave can be any frequency less than or equal to the bus speed.

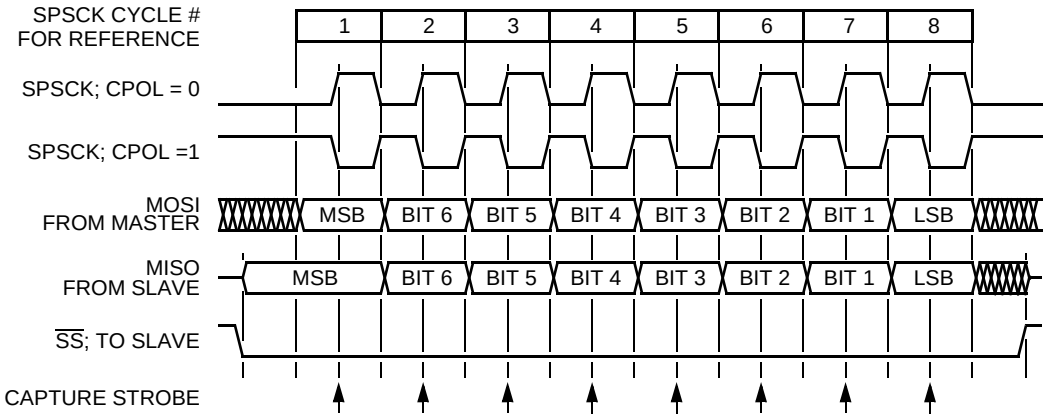


Figure 14-4. Transmission Format (CPHA = 0)

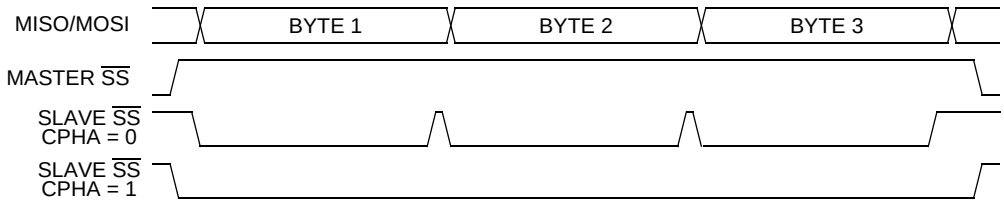


Figure 14-5. CPHA/SS Timing

When CPHA = 0 for a slave, the falling edge of SS indicates the beginning of the transmission. This causes the SPI to leave its idle state and begin driving the MISO pin with the MSB of its data. Once the transmission begins, no new data is allowed into the shift register from the transmit data register. Therefore, the SPI data register of the slave must be loaded with transmit data before the falling edge of SS. Any data written after the falling edge is stored in the transmit data register and transferred to the shift register after the current transmission.

14.7 Queuing Transmission Data

The double-buffered transmit data register allows a data byte to be queued and transmitted. For an SPI configured as a master, a queued data byte is transmitted immediately after the previous transmission has completed. The SPI transmitter empty flag (SPTE) indicates when the transmit data buffer is ready to accept new data. Write to the transmit data register only when the SPTE bit is high. **Figure 14-8** shows the timing associated with doing back-to-back transmissions with the SPI (SPSCK has CPHA: CPOL = 1:0).

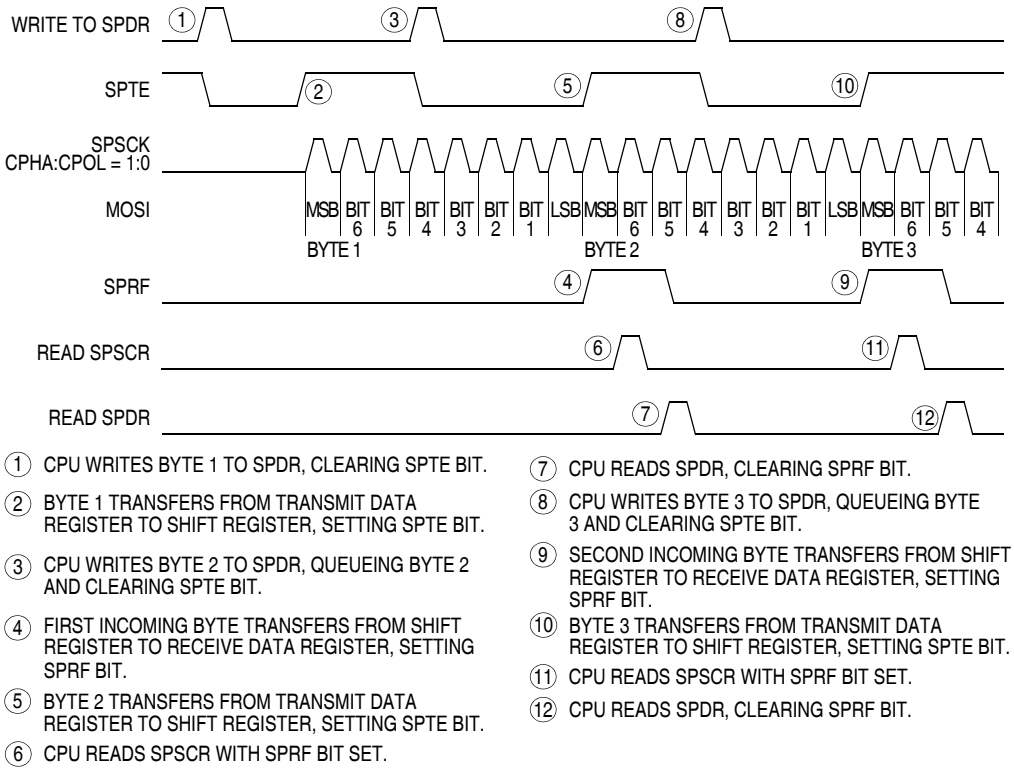


Figure 14-8. SPRF/SPTE CPU Interrupt Timing

The transmit data buffer allows back-to-back transmissions without the slave precisely timing its writes between transmissions as in a system with a single data buffer. Also, if no new data is written to the data buffer, the last value contained in the shift register is the next data word to be transmitted.

By not resetting the SPRF, OVRF, and MODF flags, the user can still service these interrupts after the SPI has been disabled. The user can disable the SPI by writing 0 to the SPE bit. The SPI can also be disabled by a mode fault occurring in an SPI that was configured as a master with the MODFEN bit set.

14.11 Low-Power Modes

The WAIT and STOP instructions put the MCU in low power-consumption standby modes.

14.11.1 Wait Mode

The SPI module remains active after the execution of a WAIT instruction. In wait mode the SPI module registers are not accessible by the CPU. Any enabled CPU interrupt request from the SPI module can bring the MCU out of wait mode.

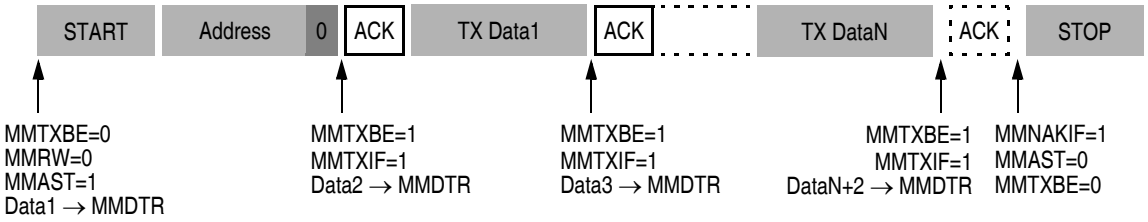
If SPI module functions are not required during wait mode, reduce power consumption by disabling the SPI module before executing the WAIT instruction.

To exit wait mode when an overflow condition occurs, enable the OVRF bit to generate CPU interrupt requests by setting the error interrupt enable bit (ERRIE). (See **14.9 Interrupts**.)

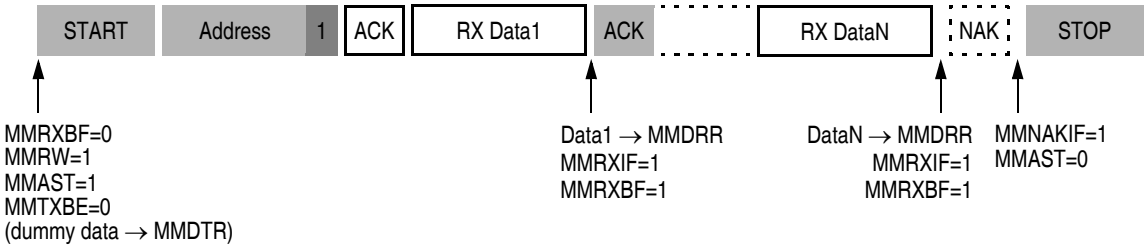
14.11.2 Stop Mode

The SPI module is inactive after the execution of a STOP instruction. The STOP instruction does not affect register conditions. SPI operation resumes after an external interrupt. If stop mode is exited by reset, any transfer in progress is aborted, and the SPI is reset.

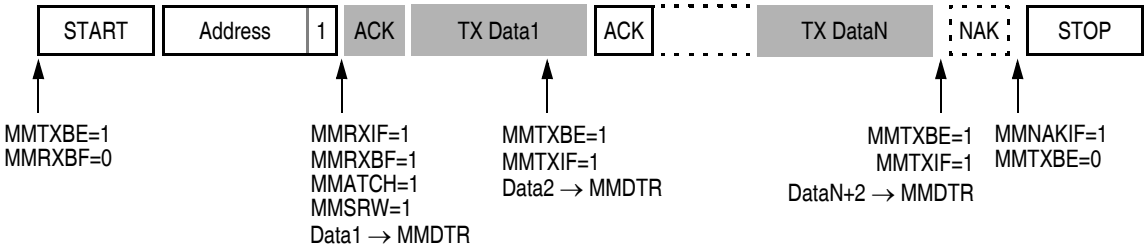
(a) Master Transmit Mode



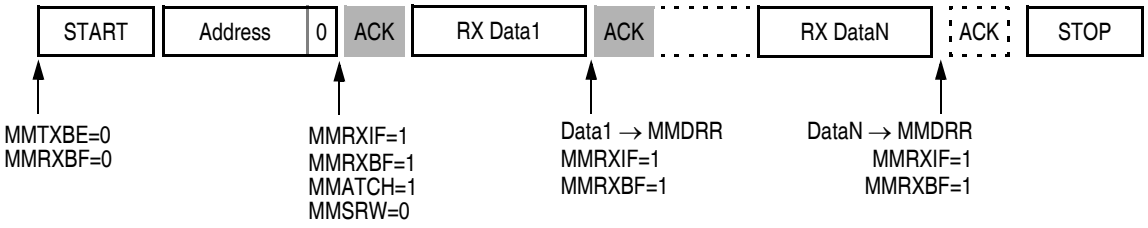
(b) Master Receive Mode



(c) Slave Transmit Mode



(d) Slave Receive Mode



Shaded data packets indicate transmissions by the MCU

Figure 15-8. Data Transfer Sequences for Master/Slave Transmit/Receive Modes

16.8.3 ADC Clock Control Register

The ADC clock control register (ADCLK) selects the clock frequency for the ADC.

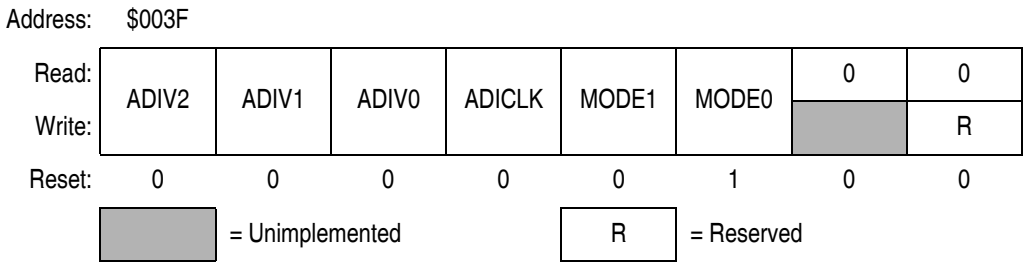


Figure 16-9. ADC Clock Control Register (ADCLK)

ADIV[2:0] — ADC Clock Prescaler Bits

ADIV2, ADIV1, and ADIV0 form a 3-bit field which selects the divide ratio used by the ADC to generate the internal ADC clock. Table 16-2 shows the available clock configurations. The ADC clock should be set to between 32kHz and 2MHz.

Table 16-2. ADC Clock Divide Ratio

ADIV2	ADIV1	ADIV0	ADC Clock Rate
0	0	0	ADC input clock ÷ 1
0	0	1	ADC input clock ÷ 2
0	1	0	ADC input clock ÷ 4
0	1	1	ADC input clock ÷ 8
1	X	X	ADC input clock ÷ 16

X = don’t care

ADICLK — ADC Input Clock Select Bit

ADICLK selects either bus clock or CGMXCLK as the input clock source to generate the internal ADC clock. Reset selects CGMXCLK as the ADC clock source.

17.5 Functional Description

Figure 17-2 shows a block diagram of the LCD driver module, and Figure 17-3 shows a simplified schematic of the LCD system.

The LCD driver module uses a 1/3 biasing method. The LCD power is supplied by the V_{LCD} pin. Voltages V_{LCD1}, V_{LCD2}, and V_{LCD3} are generated by an internal resistor ladder.

The LCD data registers, LDAT1–LDAT17, control the LCD segments' ON/OFF, with each data register controlling two frontplanes. When a logic 1 is written to a FxBx bit in the data register, the corresponding frontplane-backplane segment will turn ON. When a logic 0 is written, the the segment will turn OFF.

When the LCD driver module is disabled (LCDE = 0), the LCD display will be OFF, all backplane and frontplane drivers have the same potential as V_{DD}. The resistor ladder is disconnected from V_{DD} to reduce power consumption.

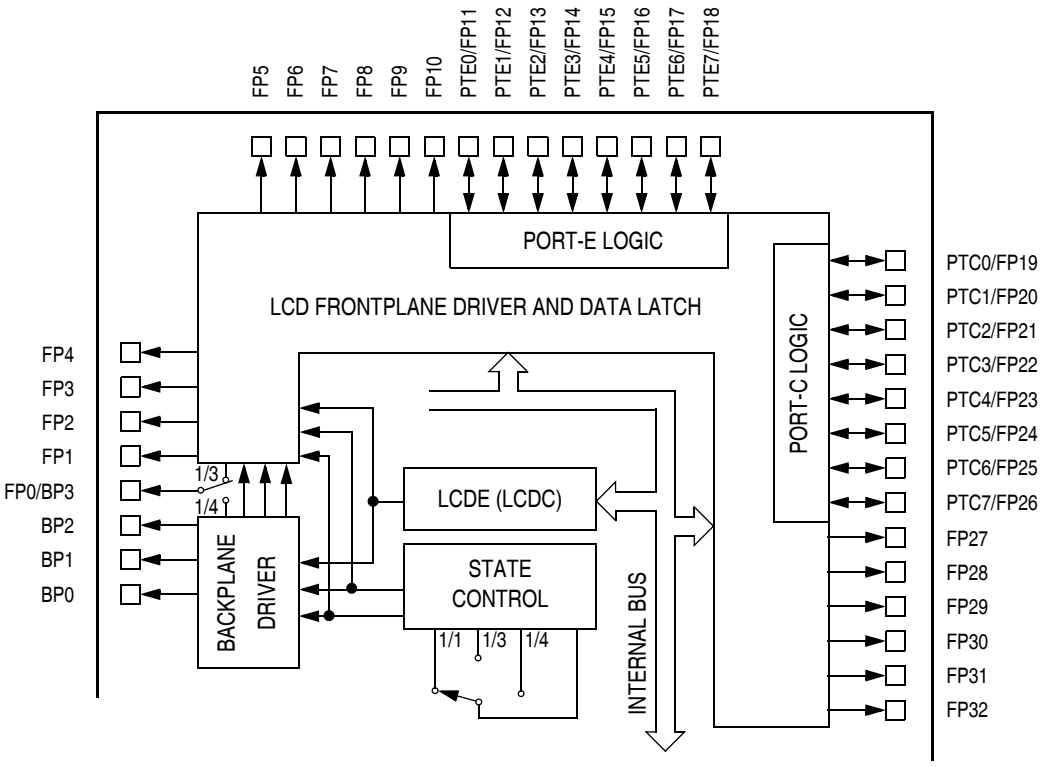


Figure 17-2. LCD Block Diagram

22.4.1 Polled LVI Operation

In applications that can operate at V_{DD} levels below the V_{TRIPF} level, software can monitor V_{DD} by polling the LVIOUT bit, or by setting the LVI interrupt enable bit, LVIIE, to enable interrupt requests. In the configuration register 1 (CONFIG1), the LVIPWRD bit must be at logic 0 to enable the LVI module, and the LVIRSTD bit must be at logic 1 to disable LVI resets.

The LVI interrupt flag, LVIIF, is set whenever the LVIOUT bit changes state (toggles). When LVIF is set, a CPU interrupt request is generated if the LVIIE is also set. In the LVI interrupt service subroutine, LVIIF bit can be cleared by writing a logic 1 to the LVI interrupt acknowledge bit, LVIIACK.

22.4.2 Forced Reset Operation

In applications that require V_{DD} to remain above the V_{TRIPF} level, enabling LVI resets allows the LVI module to reset the MCU when V_{DD} falls below the V_{TRIPF} level. In the configuration register 1 (CONFIG1), the LVIPWRD and LVIRSTD bits must be at logic 0 to enable the LVI module and to enable LVI resets.

If LVIIE is set to enable LVI interrupts when LVIRSTD is cleared, LVI reset has a higher priority over LVI interrupt. In this case, when V_{DD} falls below the V_{TRIPF} level, an LVI reset will occur, and the LVIIE bit will be cleared.

22.4.3 Voltage Hysteresis Protection

Once the LVI has triggered (by having V_{DD} fall below V_{TRIPF}), the LVI will maintain a reset condition until V_{DD} rises above the rising trip point voltage, V_{TRIPR}. This prevents a condition in which the MCU is continually entering and exiting reset if V_{DD} is approximately equal to V_{TRIPF}. V_{TRIPR} is greater than V_{TRIPF} by the hysteresis voltage, V_{HYS}.

A.5 Electrical Specifications

Electrical specifications for the MC68HC908LJ24 apply to the MC68HC908LK24, except for the parameters indicated below.

A.5.1 5V DC Electrical Characteristics

Table A-1. 5V DC Electrical Characteristics

Characteristic[1]	Symbol	Min	Typ[2]	Max	Unit
V_{DD} supply current Stop, f_{OP} = 8 kHz[3] with OSC, RTC on	I_{DD}	—	5.5	7.5	µA
Low-voltage inhibit, trip rising voltage LVI reset disabled (LVIRSTD = 1) LVI reset enabled (LVIRSTD = 0)	V_{TRIPR}	3.7 3.62	— —	4.7 4.62	V V

Notes:
1. V_{DD} = 4.5 to 5.5 Vdc, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H, unless otherwise noted.
2. Typical values reflect average measurements at midpoint of voltage range, 25 °C only.
3. The 8kHz clock is from a 32kHz external square wave clock input at OSC1, for the driving the RTC. Due to loading effects, the I_{DD} values will be larger when a 32kHz crystal circuit is connected.

A.5.2 3.3V DC Electrical Characteristics

Table A-2. 3.3V DC Electrical Characteristics

Characteristic[1]	Symbol	Min	Typ[2]	Max	Unit
Low-voltage inhibit, trip rising voltage LVI disabled (LVIRSTD = 1) LVI enabled (LVIRSTD = 0)	V_{TRIPR}	2.2 2.12	— —	2.9 2.82	V V

Notes:
1. V_{DD} = 3.0 to 3.6 Vdc, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H, unless otherwise noted.
2. Typical values reflect average measurements at midpoint of voltage range, 25 °C only.