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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HC08
Core Size	8-Bit
Speed	8MHz
Connectivity	I²C, IRSCI, SPI
Peripherals	LCD, LVD, POR, PWM
Number of I/O	40
Program Memory Size	24KB (24K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 6x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc908lj24cpber

1.6.9 ADC Voltage Low Reference Pin (V_{REFL})

V_{REFL} is the voltage input pin for the ADC voltage low reference. See 16.7.5 ADC Voltage Re ference Low Pin (V_{REFL}).

1.6.10 Port A Input/Output (I/O) Pins (PTA7–PTA0)

PTA7–PTA0 are special function, bidirectional port pins. See 18.3 Port A .
PTA7/ADC3–PTA4/ADC0 are shared with ADC, and
PTA3/KBI3–PTA0/KBI0 are shared with the KBI module.

1.6.11 Port B I/O Pins (PTB7–PTB0)

PTB7–PTB0 are special function, bidirectional port pins, with high current sink capability on PTB5–PTB0. See 18.4 Port B .
PTB1/RxD–PTB0/TxD are shared with the SCI module,
PTB5/T2CH1–PTB4/T2CH0 are shared with the TIM2,
PTB3/T1CH1–PTB2/T1CH0 are shared with the TIM1,
PTB7/ADC5–PTB6/ADC4 are shared with the ADC.

1.6.12 Port C I/O Pins (PTC7–PTC0)

PTC7–PTC0 are special function, bidirectional port pins, with high current sink capability. See 18.5 Port C .
PTC7/FP26–PTC0/FP19 are shared with the LCD frontplane drivers.

1.6.13 Port D I/O Pins (PTD7–PTD0)

PTD7–PTD0 are special function, bidirectional port pins.
PTD7/KBI7/SDA–PTD6/KBI6/SCL are shared with the KBI and IIC modules. See 18.6 Port D .
PTD5/KBI5/T2CLK–PTD4/KBI4/T1CLK are shared with the KBI, TIM1, and TIM2 modules.
PTD3/SPSCK/CALOUT–PTD0/$\overline{SS}$/CALIN are shared with the SPI and RTC modules.

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$004E	Chronograph Data Register (CHRR)	Read:	0	CHR6	CHR5	CHR4	CHR3	CHR2	CHR1	CHR0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$004F	LCD Clock Register (LCDCLK)	Read:	0	FCCTL1	FCCTL0	DUTY1	DUTY0	LCLK2	LCLK1	LCLK0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$0050	Reserved	Read:	R	R	R	R	R	R	R	R
		Write:								
		Reset:								
$0051	LCD Control Register (LCDCR)	Read:	LCDE	0	FC	LC	LCCON3	LCCON2	LCCON1	LCCON0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$0052	LCD Data Register 1 (LDAT1)	Read:	F1B3	F1B2	F1B1	F1B0	F0B3	F0B2	F0B1	F0B0
		Write:								
		Reset:	U	U	U	U	U	U	U	U
$0053	LCD Data Register 2 (LDAT2)	Read:	F3B3	F3B2	F3B1	F3B0	F2B3	F2B2	F2B1	F2B0
		Write:								
		Reset:	U	U	U	U	U	U	U	U
$0054	LCD Data Register 3 (LDAT3)	Read:	F5B3	F5B2	F5B1	F5B0	F4B3	F4B2	F4B1	F4B0
		Write:								
		Reset:	U	U	U	U	U	U	U	U
$0055	LCD Data Register 4 (LDAT4)	Read:	F7B3	F7B2	F7B1	F7B0	F6B3	F6B2	F6B1	F6B0
		Write:								
		Reset:	U	U	U	U	U	U	U	U
$0056	LCD Data Register 5 (LDAT5)	Read:	F9B3	F9B2	F9B1	F9B0	F8B3	F8B2	F8B1	F8B0
		Write:								
		Reset:	U	U	U	U	U	U	U	U
$0057	LCD Data Register 6 (LDAT6)	Read:	F11B3	F11B2	F11B1	F11B0	F10B3	F10B2	F10B1	F10B0
		Write:								
		Reset:	U	U	U	U	U	U	U	U

U = Unaffected X = Indeterminat = Unimplemented R = Reserved

Figure 2-2. Control, Status, and Data Registers (Sheet 9 of 13)

The operating range of the VCO is programmable for a wide range of frequencies and for maximum immunity to external noise, including supply and CGMXFC noise. The VCO frequency is bound to a range from roughly one-half to twice the center-of-range frequency, f_{VRS}. Modulating the voltage on the CGMXFC pin changes the frequency within this range. By design, f_{VRS} is equal to the nominal center-of-range frequency, f_{NOM}, (38.4 kHz) times a linear factor, L, and a power-of-two factor, E, or (L u2^{E})f_{NOM}.

CGMRCLK is the PLL reference clock, a buffered version of CGMXCLK. CGMRCLK runs at a frequency, f_{RCLK}, and is fed to the PLL through a programmable modulo reference divider, which divides f_{RCLK} by a factor, R. The divider's output is the final reference clock, CGMRDV, running at a frequency, $f_{RDV} = f_{RCLK}/R$. With an external crystal (30kHz–100kHz), always set R = 1 for specified performance. With an external high-frequency clock source, use R to divide the external frequency to between 30kHz and 100kHz.

The VCO's output clock, CGMVCLK, running at a frequency, f_{VCLK}, is fed back through a programmable pre-scaler divider and a programmable modulo divider. The pre-scaler divides the VCO clock by a power-of-two factor P (the CGMPCLK) and the modulo divider reduces the VCO clock by a factor, N. The dividers' output is the VCO feedback clock, CGMVDV, running at a frequency, $f_{VDV} = f_{VCLK}/(N$ u2$^{P})$. (See 8.4.6 Programming the PLL for more information.)

The phase detector then compares the VCO feedback clock, CGMVDV, with the final reference clock, CGMRDV. A correction pulse is generated based on the phase difference between the two signals. The loop filter then slightly alters the DC voltage on the external capacitor connected to CGMXFC based on the width and direction of the correction pulse. The filter can make fast or slow corrections depending on its mode, described in 8.4.4 Acquisiti on and Tracking Modes . The value of the external capacitor and the reference frequency determines the speed of the corrections and the stability of the PLL.

The lock detector compares the frequencies of the VCO feedback clock, CGMVDV, and the final reference clock, CGMRDV. Therefore, the speed of the lock detector is directly proportional to the final reference frequency, f_{RDV}. The circuit determines the mode of the PLL and the lock condition based on this comparison.

The relationship between the VCO frequency, f_{VCLK}, and the reference frequency, f_{RCLK}, is

$$f_{VCLK} = \frac{2^P N}{R} f_{RCLK}$$

where N is the integer range multiplier, between 1 and 4095.

In cases where desired bus frequency has some tolerance, choose f_{RCLK} to a value determined either by other module requirements (such as modules which are clocked by CGMXCLK), cost requirements, or ideally, as high as the specified range allows. See Section 24. Electr ical Specifications . Choose the reference divider, R = 1.

When the tolerance on the bus frequency is tight, choose f_{RCLK} to an integer divisor of f_{BUSDES}, and R = 1. If f_{RCLK} cannot meet this requirement, use the following equation to solve for R with practical choices of f_{RCLK}, and choose the f_{RCLK} that gives the lowest R.

$$R = \text{round}\left[R_{MAX} \times \left(\frac{f_{VCLKDES}}{f_{RCLK}} - \text{integer}\left(\frac{f_{VCLKDES}}{f_{RCLK}}\right)\right)\right] \quad (1)$$

4. Calculate N:

$$N = \text{round}\left(\frac{R \times f_{VCLKDES}}{f_{RCLK} \times 2^P}\right) \quad (1)$$

5. Calculate and verify the adequacy of the VCO and bus frequencies f_{VCLK} and f_{BUS}.

$$f_{VCLK} = \frac{2^P N}{R} f_{RCLK}$$

$$f_{BUS} = \frac{f_{VCLK}}{2^P \times 4}$$

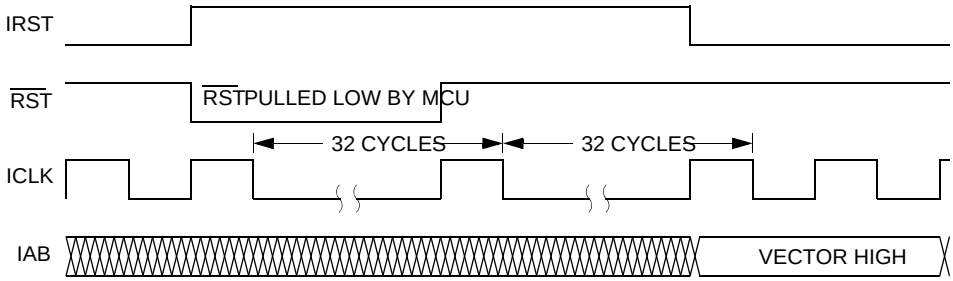

Figure 9-5. Inter nal Reset Timing

The COP reset is asynchronous to the bus clock.

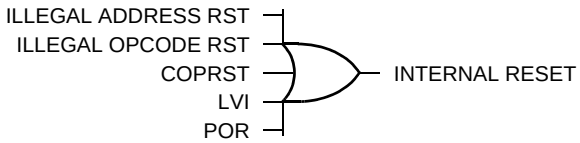

Figure 9-6. Sources of Internal Reset

The active reset feature allows the part to issue a reset to peripherals and other chips within a system built around the MCU.

9.4.2.1 Power-On Reset

When power is first applied to the MCU, the power-on reset module (POR) generates a pulse to indicate that power-on has occurred. The external reset pin ($\overline{RST}$) is held low while the SIM counter counts out 4096 + 32 ICLK cycles. Thirty-two ICLK cycles later, the CPU and memories are released from reset to allow the reset vector sequence to occur.

At power-on, these events occur:

- A POR pulse is generated.
- The internal reset signal is asserted.
- The SIM enables CGMOUT.
- Internal clocks to the CPU and modules are held inactive for 4096 ICLK cycles to allow stabilization of the oscillator.
- The $\overline{RST}$ pin is driven low during the oscillator stabilization time.
- The POR bit of the SIM reset status register (SRSR) is set and all other bits in the register are cleared.

9.8.1 SIM Break Status Register

The SIM break status register (SBSR) contains a flag to indicate that a break caused an exit from stop mode or wait mode.

Address: $FE00

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	R	R	R	R	R	R	SBSW	R
Write:							Note	
Reset:							0	

Note: Writing a logic 0 clears SBSW. R = Reserved

Figure 9-20. SIM Break Stat us Register (SBSR)

SBSW — Break Wait Bit

This status bit is set when a break interrupt causes an exit from wait mode or stop mode. Clear SBSW by writing a logic 0 to it. Reset clears SBSW.

1 = Stop mode or wait mode was exited by break interrupt
0 = Stop mode or wait mode was not exited by break interrupt

SBSW can be read within the break interrupt routine. The user can modify the return address on the stack by subtracting 1 from it. The following code is an example.

This code works if the H register has been pushed onto the stack in the break service routine software. This code should be executed at the end of the break service routine software.

```
HIBYTE    EQU
LOBYTE    EQU
          If not SBSW, do RTI
          BRCLR    SBSW,SBSR, RETURN    ;See if wait mode or stop mode was exited by break.
          TST      LOBYTE,SP            ;If RETURNLO is not zero,
          BNE      DOLO                 ;then just decrement low byte.
          DEC      HIBYTE,SP            ;Else deal with high byte, too.
DOLO      DEC      LOBYTE,SP            ;Point to WAIT/STOP opcode.
RETURN    PULH                          ;Restore H register.
          RTI
```

11.4 Pin Name Conventions

The text that follows describes both timers, TIM1 and TIM2. The TIM input/output (I/O) pin names are T[1,2]CH0 (timer channel 0). T[1,2]CH1 (timer channel 1), and T[1,2]CLK (external timer clock), where “1” is used to indicate TIM1 and “2” is used to indicate TIM2. The full names of the TIM I/O pins are listed in Table 11-1. The generic pin names appear in the text that follows.

Table 11-1. Pin Name Conventions

TIM Generic Pin Names:		T[1,2]CH0	T[1,2]CH1	T[1,2]CLK
Full TIM Pin Names:	TIM1	PTB2/T1CH0	PTB3/T1CH1	PTD4/KBI4/T1CLK
	TIM2	PTB4/T2CH0	PTB5/T2CH1	PTD5/KBI5/T2CLK

NOTE: References to either timer 1 or timer 2 may be made in the following text by omitting the timer number. For example, TCH0 may refer generically to T1CH0 and T2CH0, and TCH1 may refer to T1CH1 and T2CH1.

The T1CLK and T2CLK pins are also shared with KBI4 and KBI5 respectively. To avoid erratic behavior, these two pins should never be configured for use as TCLK and KBI inputs simultaneously.

11.5 Functional Description

Figure 11-1 shows the structure of the TIM. The central component of the TIM is the 16-bit TIM counter that can operate as a free-running counter or a modulo up-counter. The TIM counter provides the timing reference for the input capture and output compare functions. The TIM counter modulo registers, TMODH:TMODL, control the modulo value of the TIM counter. Software can read the TIM counter value at any time without affecting the counting sequence.

The two TIM channels (per timer) are programmable independently as input capture or output compare channels.