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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HC08
Core Size	8-Bit
Speed	8MHz
Connectivity	I²C, IRSCI, SPI
Peripherals	LCD, LVD, POR, PWM
Number of I/O	40
Program Memory Size	24KB (24K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 6x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc908lk24cpbe

1.5 Pin Assignments

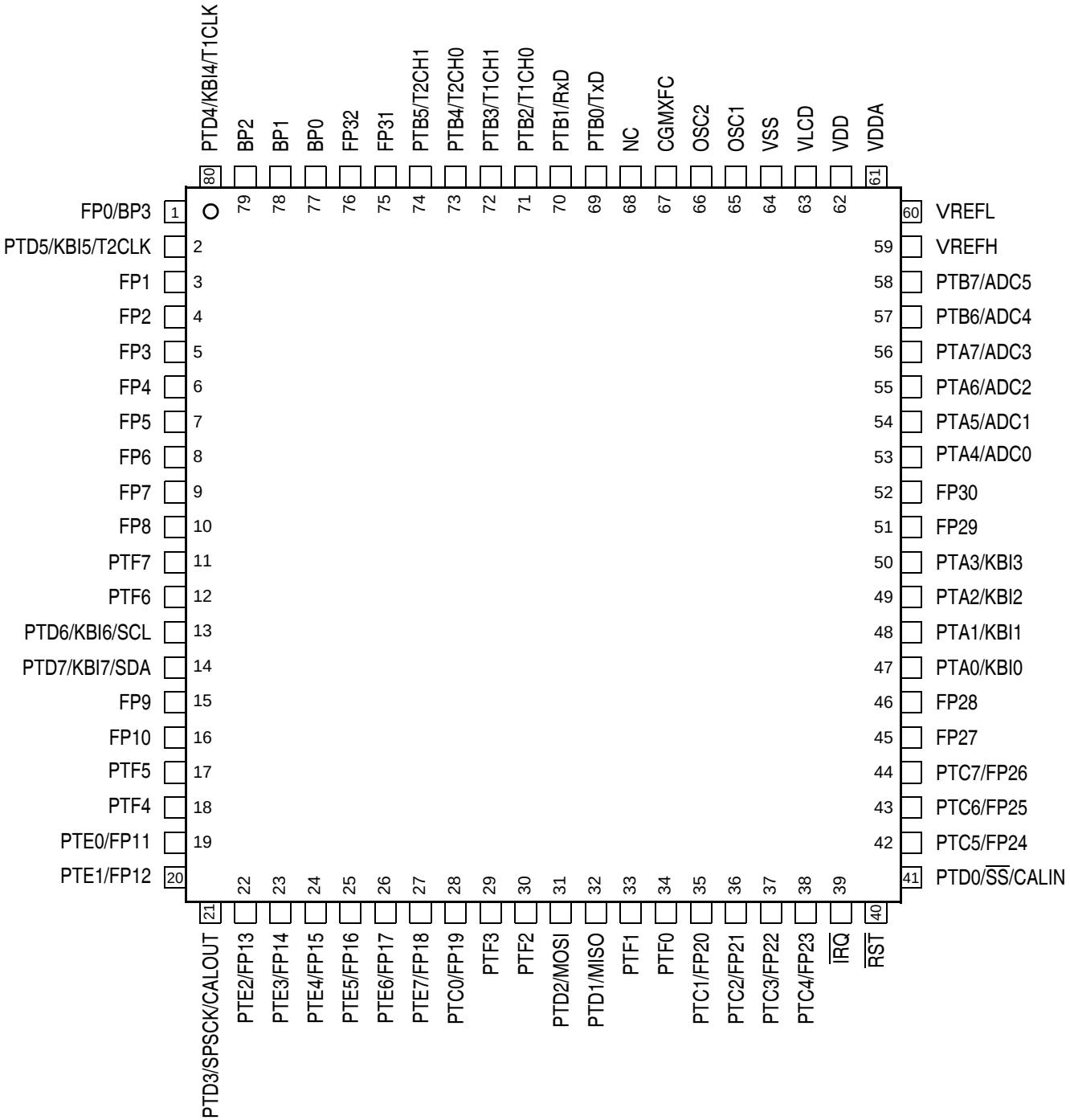


Figure 1-2. 80-Pin QFP and LQFP Pin Assignment

Section 8. Clock Generator Module (CGM)

8.1 Contents

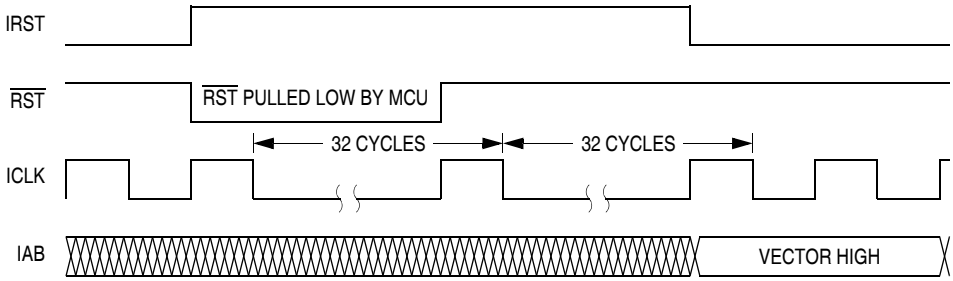


Figure 9-5. Internal Reset Timing

The COP reset is asynchronous to the bus clock.

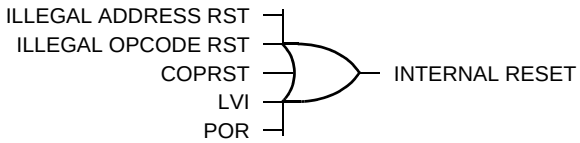


Figure 9-6. Sources of Internal Reset

The active reset feature allows the part to issue a reset to peripherals and other chips within a system built around the MCU.

9.4.2.1 Power-On Reset

When power is first applied to the MCU, the power-on reset module (POR) generates a pulse to indicate that power-on has occurred. The external reset pin ($\overline{RST}$) is held low while the SIM counter counts out 4096 + 32 ICLK cycles. Thirty-two ICLK cycles later, the CPU and memories are released from reset to allow the reset vector sequence to occur.

At power-on, these events occur:

- A POR pulse is generated.
- The internal reset signal is asserted.
- The SIM enables CGMOUT.
- Internal clocks to the CPU and modules are held inactive for 4096 ICLK cycles to allow stabilization of the oscillator.
- The $\overline{RST}$ pin is driven low during the oscillator stabilization time.
- The POR bit of the SIM reset status register (SRSR) is set and all other bits in the register are cleared.

9.8.2 SIM Reset Status Register

This register contains six flags that show the source of the last reset provided all previous reset status bits have been cleared. Clear the SIM reset status register by reading it. A power-on reset sets the POR bit and clears all other bits in the register.

Address: $FE01

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	POR	PIN	COP	ILOP	ILAD	0	LVI	0
Write:								
Reset:	1	0	0	0	0	0	0	0

= Unimplemented

Figure 9-21. SIM Reset Status Register (SRSR)

POR — Power-On Reset Bit
1 = Last reset caused by POR circuit
0 = Read of SRSR

PIN — External Reset Bit
1 = Last reset caused by external reset pin ($\overline{\text{RST}}$)
0 = POR or read of SRSR

COP — Computer Operating Properly Reset Bit
1 = Last reset caused by COP counter
0 = POR or read of SRSR

ILOP — Illegal Opcode Reset Bit
1 = Last reset caused by an illegal opcode
0 = POR or read of SRSR

ILAD — Illegal Address Reset Bit (opcode fetches only)
1 = Last reset caused by an opcode fetch from an illegal address
0 = POR or read of SRSR

LVI — Low-Voltage Inhibit Reset Bit
1 = Last reset caused by the LVI circuit
0 = POR or read of SRSR

11.9 I/O Signals

Port B shares four of its pins with the TIM channel I/O pins: T1CH0, T1CH1, T2CH0, and T2CH1.
Port D shares two of its pins with the TIM clock input pins: T1CLK and T2CLK

11.9.1 TIM Clock Pins (PTD4/KBI4/T1CLK, PTD5/KBI5/T2CLK)

T[1,2]CLK is an external clock input that can be the clock source for the TIM[1,2] counter instead of the prescaled internal bus clock. Select the T[1,2]CLK input by writing logic 1's to the three prescaler select bits, PS[2:0]. (See **11.10.1 TIM Status and Control Register**.) The minimum T[1,2]CLK pulse width, $T[1,2]CLK_{LMIN}$ or $T[1,2]CLK_{HMIN}$, is:

$$\frac{1}{\text{bus frequency}} + t_{SU}$$

The maximum T[1,2]CLK frequency is:

$$\text{bus frequency} \div 2$$

T1CLK and T2CLK are available as standard I/Os or KBI pins when not used as the TIM clock inputs.

11.9.2 TIM Channel I/O Pins (PTB2/T1CH0, PTB3/T1CH1, PTB4/T2CH0, PTB5/T2CH1)

Each channel I/O pin is programmable independently as an input capture pin or an output compare pin. T1CH0 and T2CH0 can be configured as buffered output compare or buffered PWM pins.

11.10 I/O Registers

NOTE: *References to either timer 1 or timer 2 may be made in the following text by omitting the timer number. For example, TSC may generically refer to both T1SC AND T2SC.*

These I/O registers control and monitor operation of the TIM:

- TIM status and control register (TSC)
- TIM counter registers (TCNTH:TCNTL)
- TIM counter modulo registers (TMODH:TMODL)
- TIM channel status and control registers (TSC0, TSC1)
- TIM channel registers (TCH0H:TCH0L, TCH1H:TCH1L)

11.10.1 TIM Status and Control Register

The TIM status and control register (TSC):

- Enables TIM overflow interrupts
- Flags TIM overflows
- Stops the TIM counter
- Resets the TIM counter
- Prescales the TIM counter clock

Address: T1SC, $0020 and T2SC, $002B

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	TOF	TOIE	TSTOP	0	0	PS2	PS1	PS0
Write:	0			TRST				
Reset:	0	0	1	0	0	0	0	0

= Unimplemented

Figure 11-4. TIM Status and Control Register (TSC)

A negative E-value indicates the number of CGMXCLK cycles that needs to be subtracted, because the CGMXCLK is slower than the ideal 32.768kHz; 32768 CGMXCLK cycles will be more longer than 1-second.

A positive E-value indicates the number of CGMXCLK cycles that needs to be added, because the CGMXCLK is faster than the ideal 32.768kHz; 32768 CGMXCLK cycles will be more shorter than 1-second.

If the time difference is more than 31 CGMXCLK cycles, the E-register will overflow, causing the EVOL flag to be set. The maximum (+30) or minimum (–30) value will remain in the E-register.

After calibration, with the E-value stored in the calibration data register, clock compensation is only enabled when the COMEN bit is set in RTCCR2. As the E-value is the time difference for 15 seconds, the CGMXCLK is modified for every 15-second intervals. The CGMXCLK additions and subtractions are simulated using programmable dividers, therefore, the compensated clock does not have the same period within the 15-second, but is consistent for every 15-second periods. See **Table 12-2** and **Figure 12-4**.

12.7.1 Calibration Error

During clock calibration, the reference signal to the CALIN pin is not synchronized to the CGMXCLK being measured. A maximum inaccuracy of minus 1.5×CGMXCLK period or plus 1×CGMXCLK period will be introduced to the time difference measured.

Table 12-2. Compensation Algorithm for Different Values of E

	Period A		Period B	
E	**Number of CGMXCLK Cycles**	**CGMXCLK Divider A**	**Number of CGMXCLK Cycles**	**CGMXCLK Divider B**
–30 ≤ E ≤ –16	(|E| – 15) × 32766	32766	(30 – |E|) × 32767	32767
–15 ≤ E ≤ –1	|E| × 32767	32767	(15 – |E|) × 32768	32768
E = 0	No compensation is required: Divider is 32768 throughout.			
1 ≤ E ≤ 15	|E| × 32769	32769	(15 – |E|) × 32768	32769
16 ≤ E ≤ 30	(|E| – 15) × 32770	32770	(30 – |E|) × 32769	32769

SECIE — Second Interrupt Enable

This read/write bit enables the second flag, SECF, to generate CPU interrupt requests. Reset clears the SECIE bit.

1 = SECF enabled to generate CPU interrupt
0 = SECF not enabled to generate CPU interrupt

TB1IE — Timebase 1 Interrupt Enable

This read/write bit enables the timebase1 flag, TB1F, to generate CPU interrupt requests. Reset clears the TB1IE bit.

1 = TB1F enabled to generate CPU interrupt
0 = TB1F not enabled to generate CPU interrupt

TB2IE — Timebase 2 Interrupt Enable

This read/write bit enables the timebase2 flag, TB2F, to generate CPU interrupt requests. Reset clears the TB2IE bit.

1 = TB2F enabled to generate CPU interrupt
0 = TB2F not enabled to generate CPU interrupt

12.10.4 RTC Control Register 2 (RTCCR2)

The RTC control register 2 (RTCCR2) contains control and clock selection bits for RTC operation.

Address: $0043

Read:	COMEN*	0	CHRE	RTCE*	TBH	0	0	0
Write:		CHRCLR						
Reset:	U	0	0	0††	0	0	0	0

= Unimplemented

†† Reset by POR only.
* COMEN and RTCE bits are write-protected; unprotect by a write sequence to RTCWE[1:0] in RTCCOMR.

Figure 12-9. RTC Control Register 2 (RTCCR2)

COMEN — RTC Compensation Enable

This read/write bit enables the clock compensation mechanism for CGMXCLK frequency errors. Reset has no effect on COMEN bit.

1 = Compensation mechanism enabled
0 = Compensation mechanism not enabled

The infrared sub-module receives two clock sources from the SCI module: SCI_R16XCLK and SCI_R32XCLK. Both reference clocks are used to generate the narrow pulses during data transmission.
The SCI_R16XCLK and SCI_R32XCLK are internal clocks with frequencies that are 16 and 32 times the baud rate respectively. Both SCI_R16XCLK and SCI_R32XCLK clocks are used for transmitting data. The SCI_R16XCLK clock is used only for receiving data.

NOTE: *For proper SCI function (transmit or receive), the bus clock MUST be programmed to at least 32 times that of the selected baud rate.*
When the infrared sub-module is disabled, signals on the TxD and RxD pins pass through unchanged to the SCI module.

13.6 Infrared Functional Description

Figure 13-3 shows the structure of the infrared sub-module.

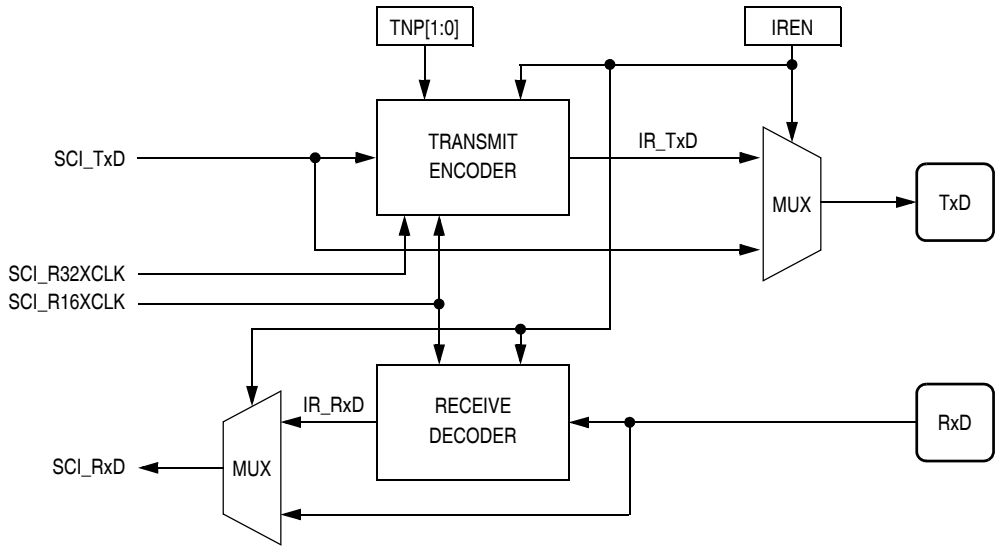


Figure 13-3. Infrared Sub-Module Diagram

The infrared sub-module provides the capability of transmitting narrow pulses to an infrared LED and receiving narrow pulses and transforming them to serial bits, which are sent to the SCI module. The infrared sub-module receives two clocks from the SCI. One of these two clocks is selected as the base clock to generate the 3/16, 1/16, or 1/32 bit width narrow pulses during transmission.

Table 13-9. SCI Baud Rate Selection Examples

SCP1 and SCP0	Prescaler Divisor (PD)	SCR2, SCR1, and SCR0	Baud Rate Divisor (BD)	Baud Rate (f_{BUS} = 4.9152 MHz)
00	1	000	1	—
00	1	001	2	—
00	1	010	4	76800
00	1	011	8	38400
00	1	100	16	19200
00	1	101	32	9600
00	1	110	64	4800
00	1	111	128	2400
01	3	000	1	—
01	3	001	2	51200
01	3	010	4	25600
01	3	011	8	12800
01	3	100	16	6400
01	3	101	32	3200
01	3	110	64	1600
01	3	111	128	800
10	4	000	1	76800
10	4	001	2	38400
10	4	010	4	19200
10	4	011	8	9600
10	4	100	16	4800
10	4	101	32	2400
10	4	110	64	1200
10	4	111	128	600
11	13	000	1	23632
11	13	001	2	11816
11	13	010	4	5908
11	13	011	8	2954
11	13	100	16	1477
11	13	101	32	739
11	13	110	64	369
11	13	111	128	185

14.12 SPI During Break Interrupts

The system integration module (SIM) controls whether status bits in other modules can be cleared during the break state. The BCFE bit in the SIM break flag control register (SBFCR) enables software to clear status bits during the break state. (See **Section 9. System Integration Module (SIM)**.)

To allow software to clear status bits during a break interrupt, write a logic 1 to the BCFE bit. If a status bit is cleared during the break state, it remains cleared when the MCU exits the break state.

To protect status bits during the break state, write a logic 0 to the BCFE bit. With BCFE at logic 0 (its default state), software can read and write I/O registers during the break state without affecting status bits. Some status bits have a 2-step read/write clearing procedure. If software does the first step on such a bit before the break, the bit cannot change during the break state as long as BCFE is at logic 0. After the break, doing the second step clears the status bit.

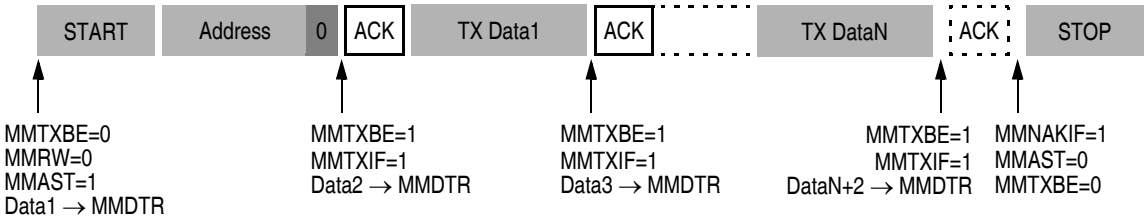
Since the SPTE bit cannot be cleared during a break with the BCFE bit cleared, a write to the transmit data register in break mode does not initiate a transmission nor is this data transferred into the shift register. Therefore, a write to the SPDR in break mode with the BCFE bit cleared has no effect.

14.13 I/O Signals

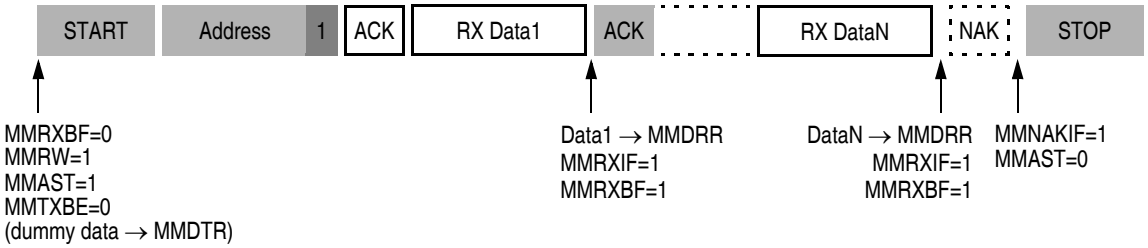
The SPI module has five I/O pins and shares four of them with a parallel I/O port. They are:

- MISO — Data received
- MOSI — Data transmitted
- SPSCK — Serial clock
- $\overline{SS}$ — Slave select
- CGND — Clock ground (internally connected to V_{SS})

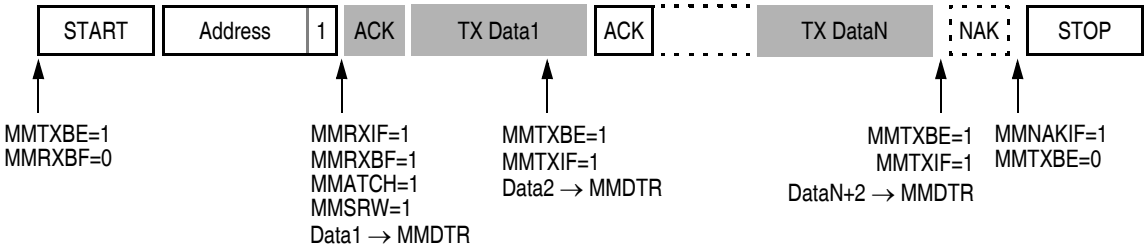
(a) Master Transmit Mode



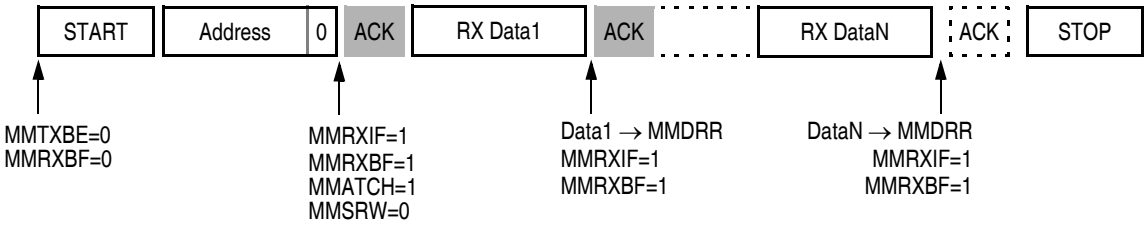
(b) Master Receive Mode



(c) Slave Transmit Mode



(d) Slave Receive Mode



Shaded data packets indicate transmissions by the MCU

Figure 15-8. Data Transfer Sequences for Master/Slave Transmit/Receive Modes

16.8 I/O Registers

These I/O registers control and monitor operation of the ADC:

- ADC status and control register, (ADSCR)
- ADC data register (ADRH:ADRL)
- ADC clock control register (ADCLK)

16.8.1 ADC Status and Control Register

This section describes the function of the ADC status and control register (ADSCR). Writing ADSCR aborts the current conversion and initiates a new conversion.

Address: $003C

Read:	COCO	AIEN	ADCO	ADCH4	ADCH3	ADCH2	ADCH1	ADCH0
Write:								
Reset:	0	0	0	1	1	1	1	1

= Unimplemented

Figure 16-4. ADC Status and Control Register (ADSCR)

COCO — Conversions Complete Bit

When the AIEN bit is a logic 0, the COCO is a read-only bit which is set each time a conversion is completed. This bit is cleared whenever the ADSCR is written, or whenever the ADC clock control register is written, or whenever the ADC data register low, ADRL, is read.

If the AIEN bit is logic 1, the COCO bit always read as logic 0, CPU to service the ADC interrupt will be generated at the end if an ADC conversion. Reset clears the COCO bit.

1 = Conversion completed (AIEN = 0)
0 = Conversion not completed (AIEN = 0)/CPU interrupt (AIEN=1)

AIEN — ADC Interrupt Enable Bit

When this bit is set, an interrupt is generated at the end of an ADC conversion. The interrupt signal is cleared when the data register, ADR0, is read or the ADSCR is written. Reset clears the AIEN bit.

1 = ADC interrupt enabled
0 = ADC interrupt disabled

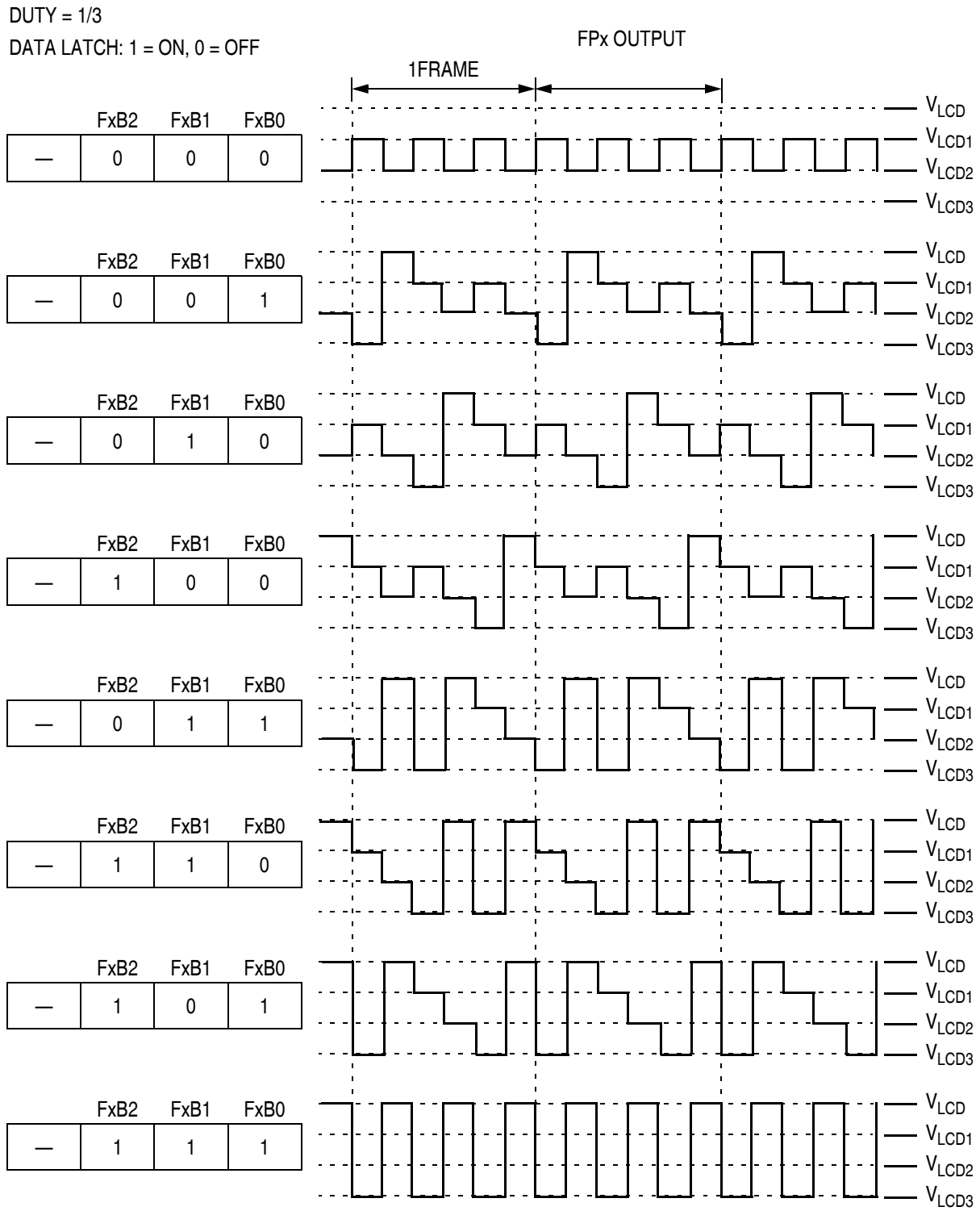


Figure 17-9. 1/3 Duty LCD Frontplane Driver Waveforms

18.3 Port A

Port A is an 8-bit special function port that shares four of its port pins with the analog-to-digital converter (ADC) module and four of its port pins with the keyboard interrupt module (KBI).

18.3.1 Port A Data Register (PTA)

The port A data register contains a data latch for each of the eight port A pins.

Address: $0000

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PTA7	PTA6	PTA5	PTA4	PTA3	PTA2	PTA1	PTA0
Reset:	Unaffected by Reset							
Alternative Function:	ADC3	ADC2	ADC1	ADC0	KBI3	KBI2	KBI1	KBI0

Figure 18-2. Port A Data Register (PTA)

PTA[7:0] — Port A Data Bits

These read/write bits are software programmable. Data direction of each port A pin is under the control of the corresponding bit in data direction register A. Reset has no effect on port A data.

KBI[3:0] — Keyboard Interrupt Channels 3 to 0

KBI[3:0] are pins used for the keyboard interrupt input. The corresponding input, KBI[3:0], can be enabled in the keyboard interrupt enable register, KBIER. Port pins used as KBI input will override any control from the port I/O logic. See **Section 20. Keyboard Interrupt Module (KBI)**.

18.5 Port C

Port C is an 8-bit special function port that shares all of its port pins with the liquid crystal display (LCD) driver module.

Port pins PTC0–PTC7 can be configured for direct LED drive.

18.5.1 Port C Data Register (PTC)

The port C data register contains a data latch for each of the eight port C pins.

Address: $0002

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PTC7	PTC6	PTC5	PTC4	PTC3	PTC2	PTC1	PTC0
Reset:	Unaffected by reset							
Alternative Function:	FP26	FP25	FP24	FP23	FP22	FP21	FP20	FP19
Additional Function:	LED drive	LED drive	LED drive	LED drive	LED drive	LED drive	LED drive	LED drive

Figure 18-9. Port C Data Register (PTC)

PTC[7:0] — Port C Data Bits

These read/write bits are software programmable. Data direction of each port C pin is under the control of the corresponding bit in data direction register C. Reset has no effect on port C data.

FP[26:19] — LCD Driver Frontplanes 26–19

FP[26:19] are pins used for the frontplane output of the LCD driver module. The enable bits, PCEH and PCEL, in the CONFIG2 register, determine whether the PTC7/FP26–PTC4/FP23 and PTC3/FP22–PTC0/FP19 pins are LCD frontplane driver pins or general-purpose I/O pins. See **Section 17. Liquid Crystal Display (LCD) Driver**.

LED drive — Direct LED Drive Pins

PTC0–PTC7 pins can be configured for direct LED drive. See **18.5.3 Port C LED Control Register (LEDC)**.

19.4 Functional Description

A logic 0 applied to the external interrupt pin can latch a CPU interrupt request. **Figure 19-1** shows the structure of the IRQ module.

Interrupt signals on the $\overline{\text{IRQ}}$ pin are latched into the IRQ latch. An interrupt latch remains set until one of the following actions occurs:

- Vector fetch — A vector fetch automatically generates an interrupt acknowledge signal that clears the IRQ latch.
- Software clear — Software can clear the interrupt latch by writing to the acknowledge bit in the interrupt status and control register (INTSCR). Writing a logic 1 to the ACK bit clears the IRQ latch.
- Reset — A reset automatically clears the interrupt latch.

The external interrupt pin is falling-edge-triggered and is software-configurable to be either falling-edge or low-level-triggered. The MODE bit in the INTSCR controls the triggering sensitivity of the $\overline{\text{IRQ}}$ pin.

When the interrupt pin is edge-triggered only, the CPU interrupt request remains set until a vector fetch, software clear, or reset occurs.

When the interrupt pin is both falling-edge and low-level-triggered, the CPU interrupt request remains set until both of the following occur:

- Vector fetch or software clear
- Return of the interrupt pin to logic 1

The vector fetch or software clear may occur before or after the interrupt pin returns to logic 1. As long as the pin is low, the interrupt request remains pending. A reset will clear the latch and the MODE control bit, thereby clearing the interrupt even if the pin stays low.

When set, the IMASK bit in the INTSCR mask all external interrupt requests. A latched interrupt request is not presented to the interrupt priority logic unless the IMASK bit is clear.

NOTE: *The interrupt mask (I) in the condition code register (CCR) masks all interrupt requests, including external interrupt requests.*

21.5 COP Control Register

The COP control register is located at address $FFFF and overlaps the reset vector. Writing any value to $FFFF clears the COP counter and starts a new timeout period. Reading location $FFFF returns the low byte of the reset vector.

Address: $FFFF

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	Low byte of reset vector							
Write:	Clear COP counter							
Reset:	Unaffected by reset							

Figure 21-3. COP Control Register (COPCTL)

21.6 Interrupts

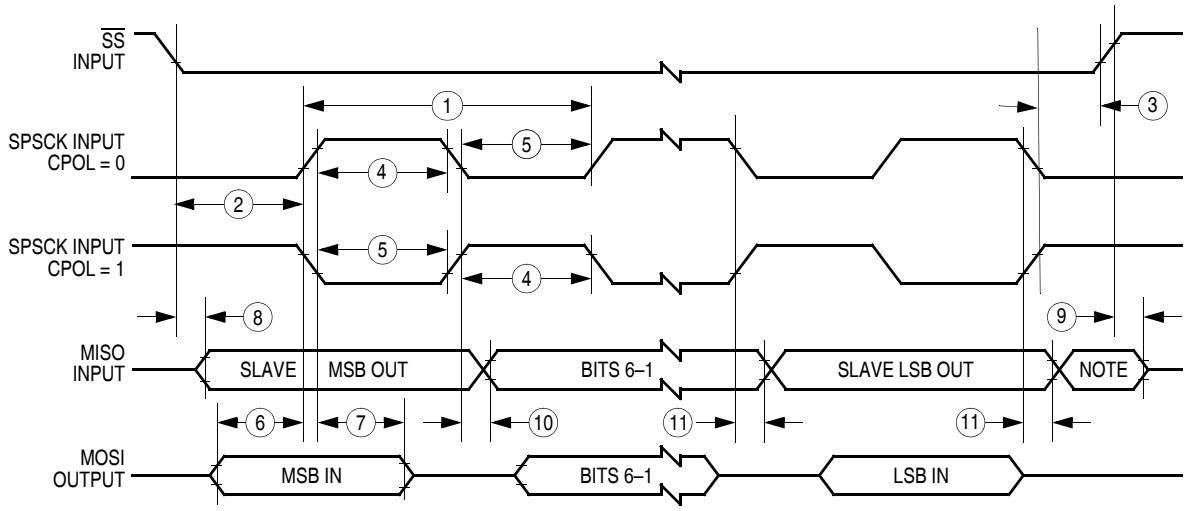
The COP does not generate CPU interrupt requests.

21.7 Monitor Mode

When monitor mode is entered with V_{TST} on the $\overline{IRQ}$ pin, the COP is disabled as long as V_{TST} remains on the $\overline{IRQ}$ pin or the $\overline{RST}$ pin. When monitor mode is entered by having blank reset vectors and not having V_{TST} on the $\overline{IRQ}$ pin, the COP is automatically disabled until a POR occurs.

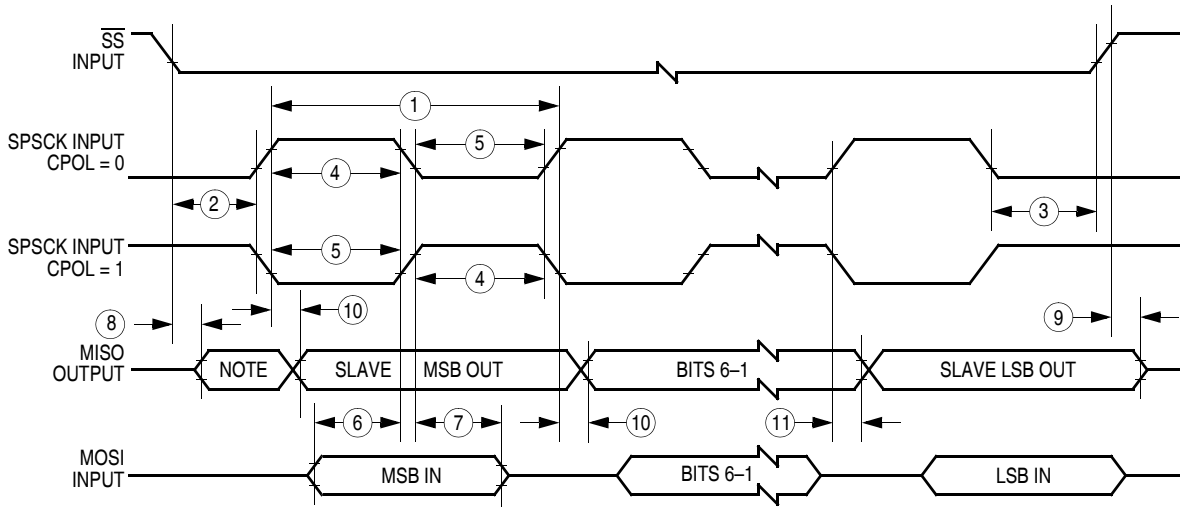
21.8 Low-Power Modes

The WAIT and STOP instructions put the MCU in low power-consumption standby modes.



Note: Not defined but normally MSB of character just received

a) SPI Slave Timing (CPHA = 0)



Note: Not defined but normally LSB of character previously transmitted

b) SPI Slave Timing (CPHA = 1)

Figure 24-3. SPI Slave Timing

Section 25. Mechanical Specifications

25.1 Contents

25.2 Introduction

This section gives the dimensions for:

- 64-pin low-profile quad flat pack (case no. 840F)
- 64-pin quad flat pack (case no. 840B)
- 80-pin low-profile quad flat pack (case no. 917)
- 80-pin quad flat pack (case no. 841B)