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Details

Product Status	Obsolete
Core Processor	HC08
Core Size	8-Bit
Speed	8MHz
Connectivity	I ² C, IRSCI, SPI
Peripherals	LCD, LVD, POR, PWM
Number of I/O	40
Program Memory Size	24KB (24K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 6x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-FQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc908lk24cpker

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1.2 Introduction

The MC68HC908LJ24 is a member of the low-cost, high-performance M68HC08 Family of 8-bit microcontroller units (MCUs). The M68HC08 Family is based on the customer-specified integrated circuit (CSIC) design strategy. All MCUs in the family use the enhanced M68HC08 central processor unit (CPU08) and are available with a variety of modules, memory sizes and types, and package types.

1.3 Features

Features of the MC68HC908LJ24 include the following:

- High-performance M68HC08 architecture
- Fully upward-compatible object code with M6805, M146805, and M68HC05 Families
 - 8-MHz at 5V operating voltage
 - 4-MHz at 3.3V operating voltage
- 32.768kHz crystal oscillator clock input with 32MHz internal PLL
- Optional continuous crystal oscillator operation in stop mode
- 24K-bytes user program FLASH memory with security¹ feature
- 768 bytes of on-chip RAM
- Up to 48 general-purpose input/output (I/O) pins:
 - High current 15mA sink capability on 30 pins
- Two 16-bit, 2-channel timer interface modules (TIM1 and TIM2) with selectable input capture, output compare, PWM capability on each channel, and external clock input option (T1CLK and T2CLK)
- Real time clock (RTC) with:
 - Clock, calendar, alarm, and chronograph functions
 - Selectable periodic interrupt requests for seconds, minutes, hours, days, 2-Hz, 4-Hz, 8-Hz, 16-Hz, and 128-Hz

¹ No security feature is absolutely secure. However, Freescale strategy is to make reading or copying the FLASH difficult for unauthorized users.

- Temperature drift compensation by user software and external temperature sensor with temperature drift profile from crystal vendor
- Serial communications interface module (SCI) with infrared (IR) encoder/decoder
- Inter-IC Bus interface module (IIC)
- Serial peripheral interface module (SPI)
- $\overline{\text{IRQ}}$ external interrupt pin with integrated pullup
- 8-bit keyboard wakeup port with programmable pullup
- 4/3 backplanes and static with maximum 32/33 frontplanes liquid crystal display (LCD) driver
- 6-channel, 10-bit successive approximation analog-to-digital converter (ADC)
- Resident routines for in-circuit programming and EEPROM emulation
- Low-power design (fully static with stop and wait modes)
- Master reset pin (with integrated pullup) and power-on reset
- Spike filter protection for EMC performance enhancement
- System protection features
 - Optional computer operating properly (COP) reset, driven by internal RC oscillator
 - Low-voltage detection with optional reset or interrupt
 - Illegal opcode detection with reset
 - Illegal address detection with reset
- 80-pin quad flat pack (QFP), 80-pin low-profile quad flat pack (LQFP), 64-pin quad flat pack (QFP), and 64-pin low-profile quad flat pack (LQFP)

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
\$0058	LCD Data Register 7 (LDAT7)	Read:								
		Write:	F13B3	F13B2	F13B1	F13B0	F12B3	F12B2	F12B1	F12B0
		Reset:	U	U	U	U	U	U	U	U
\$0059	LCD Data Register 8 (LDAT8)	Read:								
		Write:	F15B3	F15B2	F15B1	F15B0	F14B3	F14B2	F14B1	F14B0
		Reset:	U	U	U	U	U	U	U	U
\$005A	LCD Data Register 9 (LDAT9)	Read:								
		Write:	F17B3	F17B2	F17B1	F17B0	F16B3	F16B2	F16B1	F16B0
		Reset:	U	U	U	U	U	U	U	U
\$005B	LCD Data Register 10 (LDAT10)	Read:								
		Write:	F19B3	F19B2	F19B1	F19B0	F18B3	F18B2	F18B1	F18B0
		Reset:	U	U	U	U	U	U	U	U
\$005C	LCD Data Register 11 (LDAT11)	Read:								
		Write:	F21B3	F21B2	F21B1	F21B0	F20B3	F20B2	F20B1	F20B0
		Reset:	U	U	U	U	U	U	U	U
\$005D	LCD Data Register 12 (LDAT12)	Read:								
		Write:	F23B3	F23B2	F23B1	F23B0	F22B3	F22B2	F22B1	F22B0
		Reset:	U	U	U	U	U	U	U	U
\$005E	LCD Data Register 13 (LDAT13)	Read:								
		Write:	F25B3	F25B2	F25B1	F25B0	F24B3	F24B2	F24B1	F24B0
		Reset:	U	U	U	U	U	U	U	U
\$005F	LCD Data Register 14 (LDAT14)	Read:								
		Write:	F27B3	F27B2	F27B1	F27B0	F26B3	F26B2	F26B1	F26B0
		Reset:	U	U	U	U	U	U	U	U
\$0060	LCD Data Register 15 (LDAT15)	Read:								
		Write:	F29B3	F29B2	F29B1	F29B0	F28B3	F28B2	F28B1	F28B0
		Reset:	U	U	U	U	U	U	U	U
\$0061	LCD Data Register 16 (LDAT16)	Read:								
		Write:	F31B3	F31B2	F31B1	F31B0	F30B3	F30B2	F30B1	F30B0
		Reset:	U	U	U	U	U	U	U	U

U = Unaffected X = Indeterminate = Unimplemented R = Reserved

Figure 2-2. Control, Status, and Data Registers (Sheet 10 of 13)

4.8 FLASH Block Protection

Due to the ability of the on-board charge pump to erase and program the FLASH memory in the target application, provision is made to protect pages of memory from unintentional erase or program operations due to system malfunction. This protection is done by use of a FLASH block protect register (FLBPR). The FLBPR determines the range of the FLASH memory which is to be protected. The range of the protected area starts from a location defined by FLBPR and ends to the bottom of the FLASH memory (\$FFFF). When the memory is protected, the HVEN bit cannot be set in either erase or program operations.

NOTE: *The 48 bytes of user interrupt vectors are always protected, regardless of the value in the FLASH block protect register. A mass erase is required to erase the vectors.*

When the FLBPR is program with \$20, the entire memory is protected from being programmed and erased. When the FLBPR is erased (\$FF), the entire memory is accessible for program and erase.

Once the FLBPR is programmed with a value other than \$FF, the FLBPR itself is protected. It can only be erased using a mass erase operation.

NOTE: *In performing a program or erase operation, the FLASH block protect register must be read after setting the PGM or ERASE bit and before asserting the HVEN bit*

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
\$0036	PLL Control Register (PTCL)	Read:	PLLIE	PLLF	PLLON	BCS	PRE1	PRE0	VPR1	VPR0
		Write:								
		Reset:	0	0	1	0	0	0	0	0
\$0037	PLL Bandwidth Control Register (PBWC)	Read:	AUTO	LOCK	ACQ	0	0	0	0	R
		Write:								
		Reset:	0	0	0	0	0	0	0	0
\$0038	PLL Multiplier Select Register High (PMSH)	Read:	0	0	0	0	MUL11	MUL10	MUL9	MUL8
		Write:								
		Reset:	0	0	0	0	0	0	0	0
\$0039	PLL Multiplier Select Register Low (PMSL)	Read:	MUL7	MUL6	MUL5	MUL4	MUL3	MUL2	MUL1	MUL0
		Write:								
		Reset:	0	1	0	0	0	0	0	0
\$003A	PLL VCO Range Select Register (PMRS)	Read:	VRS7	VRS6	VRS5	VRS4	VRS3	VRS2	VRS1	VRS0
		Write:								
		Reset:	0	1	0	0	0	0	0	0
\$003B	PLL Reference Divider Select Register (PMDS)	Read:	0	0	0	0	RDS3	RDS2	RDS1	RDS0
		Write:								
		Reset:	0	0	0	0	0	0	0	1
			= Unimplemented				R = Reserved			

NOTES:

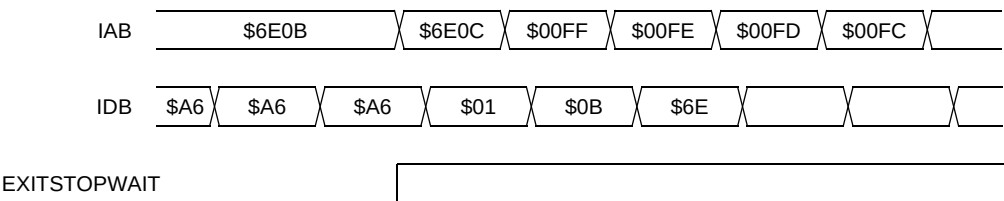
1. When AUTO = 0, PLLIE is forced clear and is read-only.
2. When AUTO = 0, PLLF and LOCK read as clear.
3. When AUTO = 1, ACQ is read-only.
4. When PLLON = 0 or VRS7:VRS0 = \$0, BCS is forced clear and is read-only.
5. When PLLON = 1, the PLL programming register is read-only.
6. When BCS = 1, PLLON is forced set and is read-only.

Figure 8-2. CGM I/O Register Summary

Section 9. System Integration Module (SIM)

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NOTE: EXITSTOPWAIT = $\overline{\text{RST}}$ pin OR CPU interrupt OR break interrupt

Figure 9-16. Wait Recovery from Interrupt or Break

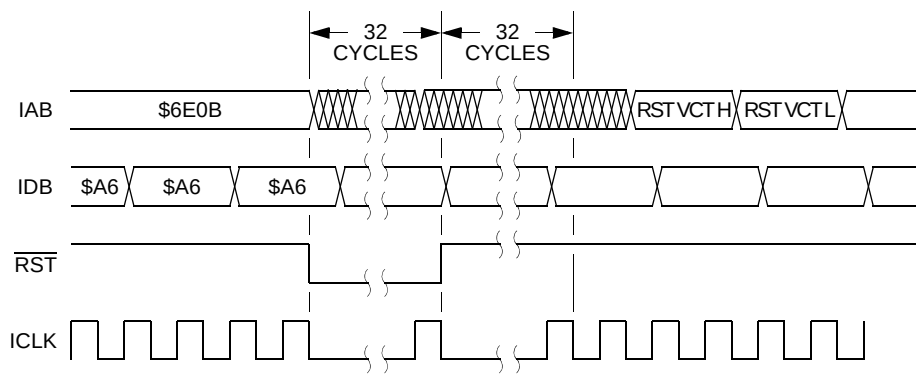


Figure 9-17. Wait Recovery from Internal Reset

9.7.2 Stop Mode

In stop mode, the SIM counter is reset and the system clocks are disabled. An interrupt request from a module can cause an exit from stop mode. Stacking for interrupts begins after the selected stop recovery time has elapsed. Reset or break also causes an exit from stop mode.

The SIM disables the clock generator module output (CGMOUT) in stop mode, stopping the CPU and peripherals. Stop recovery time is selectable using the SSREC bit in the configuration register 1 (CONFIG1). If SSREC is set, stop recovery is reduced from the normal delay of 4096 ICLK cycles down to 32. This is ideal for applications using canned oscillators that do not require long start-up times from stop mode.

NOTE: External crystal applications should use the full stop recovery time by clearing the SSREC bit.

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0	
\$0020	Timer 1 Status and Control Register (T1SC)	Read:	TOF	TOIE	TSTOP	0	0	PS2	PS1	PS0	
		Write:	0			TRST					
		Reset:	0	0	1	0	0	0	0	0	
\$0021	Timer 1 Counter Register High (T1CNTH)	Read:	Bit 15	14	13	12	11	10	9	Bit 8	
		Write:									
		Reset:	0	0	0	0	0	0	0	0	
\$0022	Timer 1 Counter Register Low (T1CNTL)	Read:	Bit 7	6	5	4	3	2	1	Bit 0	
		Write:									
		Reset:	0	0	0	0	0	0	0	0	
\$0023	Timer 1 Counter Modulo Register High (T1MODH)	Read:	Bit 15	14	13	12	11	10	9	Bit 8	
		Write:									
		Reset:	1	1	1	1	1	1	1	1	
\$0024	Timer 1 Counter Modulo Register Low (T1MODL)	Read:	Bit 7	6	5	4	3	2	1	Bit 0	
		Write:									
		Reset:	1	1	1	1	1	1	1	1	
\$0025	Timer 1 Channel 0 Status and Control Register (T1SC0)	Read:	CH0F	CH0IE	MS0B	MS0A	ELS0B	ELS0A	TOV0	CH0MAX	
		Write:	0								
		Reset:	0	0	0	0	0	0	0	0	
\$0026	Timer 1 Channel 0 Register High (T1CH0H)	Read:	Bit 15	14	13	12	11	10	9	Bit 8	
		Write:									
		Reset:	Indeterminate after reset								
\$0027	Timer 1 Channel 0 Register Low (T1CH0L)	Read:	Bit 7	6	5	4	3	2	1	Bit 0	
		Write:									
		Reset:	Indeterminate after reset								
\$0028	Timer 1 Channel 1 Status and Control Register (T1SC1)	Read:	CH1F	CH1IE	0	MS1A	ELS1B	ELS1A	TOV1	CH1MAX	
		Write:	0								
		Reset:	0	0	0	0	0	0	0	0	
				= Unimplemented							

Figure 11-2. TIM I/O Register Summary (Sheet 1 of 3)

Address: T1CNTL, \$0022 and T2CNTL, \$002D

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	Bit 7	6	5	4	3	2	1	Bit 0
Write:								
Reset:	0	0	0	0	0	0	0	0

 = Unimplemented

Figure 11-6. TIM Counter Registers Low (TCNTL)

11.10.3 TIM Counter Modulo Registers

The read/write TIM modulo registers contain the modulo value for the TIM counter. When the TIM counter reaches the modulo value, the overflow flag (TOF) becomes set, and the TIM counter resumes counting from \$0000 at the next timer clock. Writing to the high byte (TMODH) inhibits the TOF bit and overflow interrupts until the low byte (TMDL) is written. Reset sets the TIM counter modulo registers.

Address: T1MODH, \$0023 and T2MODH, \$002E

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	Bit 15	14	13	12	11	10	9	Bit 8
Write:	Bit 15	14	13	12	11	10	9	Bit 8
Reset:	1	1	1	1	1	1	1	1

Figure 11-7. TIM Counter Modulo Register High (TMODH)

Address: T1MODL, \$0024 and T2MODL, \$002F

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	Bit 7	6	5	4	3	2	1	Bit 0
Write:	Bit 7	6	5	4	3	2	1	Bit 0
Reset:	1	1	1	1	1	1	1	1

Figure 11-8. TIM Counter Modulo Register Low (TMDL)

NOTE: Reset the TIM counter before writing to the TIM counter modulo registers.

13.8 Low-Power Modes

The WAIT and STOP instructions put the MCU in low power-consumption standby modes.

13.8.1 Wait Mode

The SCI module remains active after the execution of a WAIT instruction. In wait mode, the SCI module registers are not accessible by the CPU. Any enabled CPU interrupt request from the SCI module can bring the MCU out of wait mode.

If SCI module functions are not required during wait mode, reduce power consumption by disabling the module before executing the WAIT instruction.

Refer to [9.7 Low-Power Modes](#) for information on exiting wait mode.

13.8.2 Stop Mode

The SCI module is inactive after the execution of a STOP instruction. The STOP instruction does not affect SCI register states. SCI module operation resumes after an external interrupt.

Because the internal clock is inactive during stop mode, entering stop mode during an SCI transmission or reception results in invalid data.

Refer to [9.7 Low-Power Modes](#) for information on exiting stop mode.

13.11.1 SCI Control Register 1

SCI control register 1:

- Enables loop mode operation
- Enables the SCI
- Controls output polarity
- Controls character length
- Controls SCI wakeup method
- Controls idle character detection
- Enables parity function
- Controls parity type

Address: \$0013

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	LOOPS	ENSCI	0	M	WAKE	ILTY	PEN	PTY
Write:								
Reset:	0	0	0	0	0	0	0	0

Figure 13-12. SCI Control Register 1 (SCC1)

LOOPS — Loop Mode Select Bit

This read/write bit enables loop mode operation for the SCI only. In loop mode the RxD pin is disconnected from the SCI, and the transmitter output goes into the receiver input. Both the transmitter and the receiver must be enabled to use loop mode. The infrared encoder/decoder is not in the loop. Reset clears the LOOPS bit.

- 1 = Loop mode enabled
- 0 = Normal operation enabled

ENSCI — Enable SCI Bit

This read/write bit enables the SCI and the SCI baud rate generator. Clearing ENSCI sets the SCTE and TC bits in SCI status register 1 and disables transmitter interrupts. Reset clears the ENSCI bit.

- 1 = SCI enabled
- 0 = SCI disabled

In slave mode, the data in MMDRR is:

- the calling address from the master when the address match flag is set (MMATCH = 1); or
- the last data received when MMATCH = 0.

In master mode, the data in the MMDRR is:

- the last data received.

When the MMDRR is read by the CPU, the receive buffer full flag is cleared (MMRXBF = 0), and the next received data is loaded to the MMDRR. Each time when new data is loaded to the MMDRR, the MMRXIF interrupt flag is set, indicating that new data is available in MMDRR.

The sequence of events for slave receive and master receive are illustrated in [Figure 15-8](#).

15.6 Programming Considerations

When the MMIIC module detects an arbitration loss in master mode, it will release both SDA and SCL lines immediately. But if there are no further STOP conditions detected, the module will hang up. Therefore, it is recommended to have time-out software to recover from such ill condition. The software can start the time-out counter by looking at the MMBB (Bus Busy) flag in the MIMCR and reset the counter on the completion of one byte transmission. If a time-out occur, software can clear the MMEN bit (disable MMIIC module) to release the bus, and hence clearing the MMBB flag. This is the only way to clear the MMBB flag by software if the module hangs up due to a no STOP condition received. The MMIIC can resume operation again by setting the MMEN bit.

16.2 Introduction

This section describes the analog-to-digital convert (ADC). The ADC is a 6-channel 10-bit linear successive approximation ADC.

16.3 Features

Features of the ADC module include:

- Six channels with multiplexed input
- High impedance buffered input
- Linear successive approximation with monotonicity
- 10-Bit resolution
- Single or continuous conversion
- Conversion complete flag or conversion complete interrupt
- Selectable ADC clock
- Conversion result justification
 - 8-bit truncated mode
 - Right justified mode
 - Left justified mode
 - Left justified sign mode

Section 17. Liquid Crystal Display (LCD) Driver

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DUTY[1:0] — Duty Cycle Select

These read/write bits select the duty cycle of the LCD driver output waveforms. The multiplexed FP0/BP3 pin is controlled by the duty cycle selected. Reset clears these bits.

Table 17-5. LCD Duty Cycle Selection

DUTY1:DUTY0	Description
00	Static selected; FP0/BP3 pin function as FP0.
01	1/3 duty cycle selected; FP0/BP3 pin functions as FP0.
10	1/4 duty cycle selected; FP0/BP3 pin functions as BP3.
11	Not used

LCLK[2:0] — LCD Waveform Base Clock Select

These read/write bits selects the LCD waveform base clock. Reset clears these bits.

Table 17-6. LCD Waveform Base Clock Selection

LCLK2	LCLK1	LCLK0	Divide Ratio	LCD Waveform Base Clock Frequency LCDCLK (Hz)		LCD Frame Rate $f_{XTAL}^{(1)} = 32.768\text{ kHz}$		LCD Frame Rate $f_{XTAL} = 4.9152\text{ MHz}$	
				$f_{XTAL} = 32.768\text{ kHz}$	$f_{XTAL} = 4.9152\text{ MHz}$	1/3 duty	1/4 duty	1/3 duty	1/4 duty
0	0	0	128	256	—	85.3	64	—	—
0	0	1	256	128	—	42.7	32	—	—
0	1	0	512	64	—	21.3	16	—	—
0	1	1	1024	32	—	10.7	8	—	—
1	0	0	16384	—	300	—	—	100	75
1	0	1	32768	—	150	—	—	50	37.5
1	1	0	65536	—	75	—	—	25	18.75
1	1	1	Reserved						

Notes:

1. f_{XTAL} is the same as CGMXCLK (see [Section 7. Oscillator \(OSC\)](#)).

ADC[3:0] — ADC channels 0 to 3

ADC[3:0] are pins used for the input channels to the analog-to-digital converter module. The channel select bits, ADCH[4:0], in the ADC status and control register define which port pin will be used as an ADC input and overrides any control from the port I/O logic. See [Section 16. Analog-to-Digital Converter \(ADC\)](#).

NOTE: Care must be taken when reading port A while applying analog voltages to ADC[3:0] pins. If the appropriate ADC channel is not enabled, excessive current drain may occur if analog voltages are applied to the PTAx/ADCx pin, while PTA is read as a digital input. Those ports not selected as analog input channels are considered digital I/O ports.

18.3.2 Data Direction Register A (DDRA)

Data direction register A determines whether each port A pin is an input or an output. Writing a logic 1 to a DDRA bit enables the output buffer for the corresponding port A pin; a logic 0 disables the output buffer.

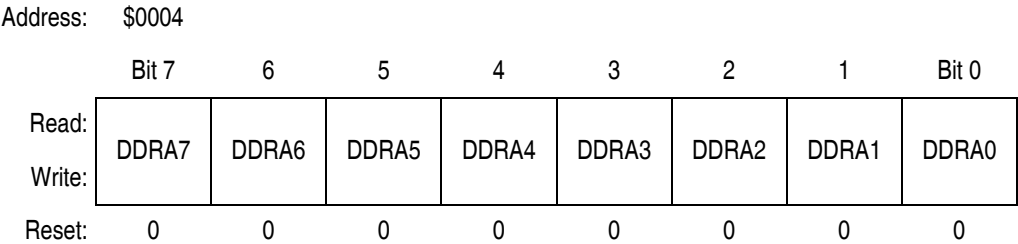


Figure 18-3. Data Direction Register A (DDRA)

DDRA[7:0] — Data Direction Register A Bits

These read/write bits control port A data direction. Reset clears DDRA[7:0], configuring all port A pins as inputs.

- 1 = Corresponding port A pin configured as output
- 0 = Corresponding port A pin configured as input

NOTE: Avoid glitches on port A pins by writing to the port A data register before changing data direction register A bits from 0 to 1. [Figure 18-4](#) shows the port A I/O logic.

A.3 Oscillator

The low-power oscillator supports a reference frequency of 32.768kHz only; either from a crystal oscillator circuit ([Figure A-1](#)) or a direct clock input to the OSC1 pin.

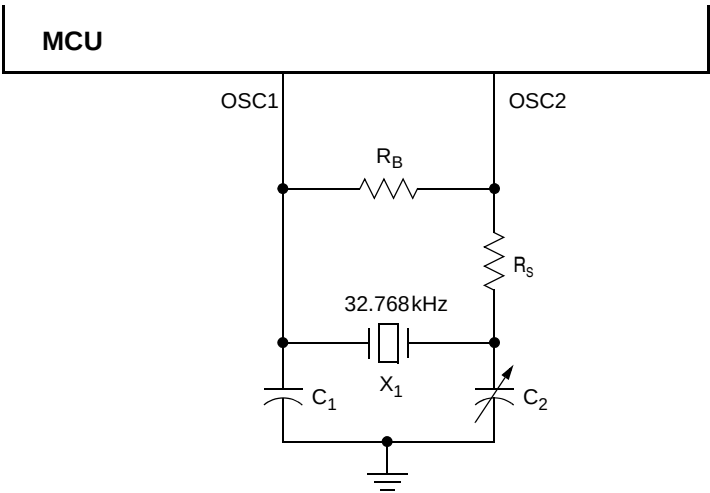


Figure A-1. MC68HC908LK24 Crystal Oscillator Connection

A.4 Low-Voltage Inhibit

The LVIPWRD bit in CONFIG1 register is logic 1 after any reset.

Address: \$001F

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	COPRS	LVISTOP	LVIRSTD	LVIPWRD	0	SSREC	STOP	COPD
Write:								
MC68HC908LK24	Reset: 0	0	0	1	0	0	0	0
MC68HC908LJ24	Reset: 0	0	0	0 ^{††}	0	0	0	0

^{††} Reset by POR only.
 = Unimplemented

Figure A-2. MC68HC908LK24 Configuration Register 1 (CONFIG1)

LVIPWRD — LVI Power Disable Bit

LVIPWRD disables the LVI module.

1 = LVI module power disabled

0 = LVI module power enabled