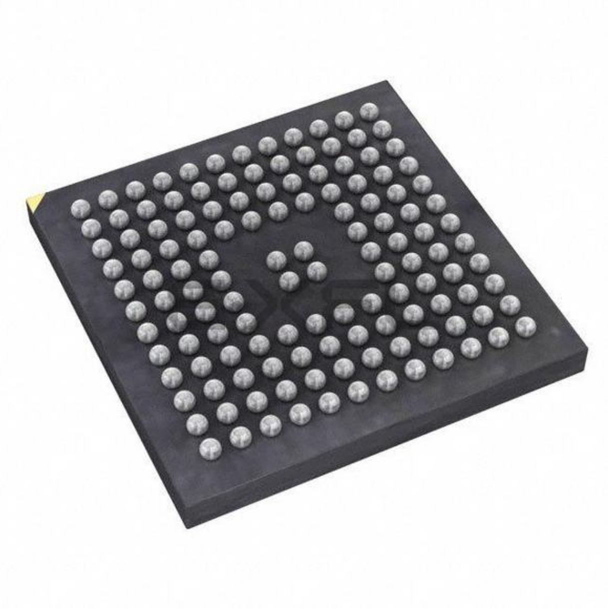
STMicroelectronics - STM32L486QGI6 Datasheet



Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, MMC/SD, QSPI, SAI, SPI, SWPMI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, LCD, PWM, WDT
Number of I/O	109
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 19x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	132-UFBGA
Supplier Device Package	132-UFBGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l486qgi6

Table 4. STM32L486xx modes overview

Mode	Regulator (1)	CPU	Flash	SRAM	Clocks	DMA & Peripherals(2)	Wakeup source	Consumption(3)	Wakeup time
Run	Range 1	Yes	ON(4)	ON	Any	All	N/A	112 µA/MHz	N/A
	Range2					All except OTG_FS, RNG		100 µA/MHz	
LPRun	LPR	Yes	ON(4)	ON	Any except PLL	All except OTG_FS, RNG	N/A	136 µA/MHz	to Range 1: 4 µs to Range 2: 64 µs
Sleep	Range 1	No	ON(4)	ON(5)	Any	All	Any interrupt or event	37 µA/MHz	6 cycles
	Range 2					All except OTG_FS, RNG		35 µA/MHz	6 cycles
LPSleep	LPR	No	ON(4)	ON(5)	Any except PLL	All except OTG_FS, RNG	Any interrupt or event	40 µA/MHz	6 cycles
Stop 0	Range 1	No	Off	ON	LSE LSI	BOR, PVD, PVM RTC, LCD,IWDG COMPx (x=1,2) DACx (x=1,2) OPAMPx (x=1,2) USARTx (x=1...5)(6) LPUART1(6) I2Cx (x=1...3)(7) LPTIMx (x=1,2) *** All other peripherals are frozen.	Reset pin, all I/Os BOR, PVD, PVM RTC, LCD,IWDG COMPx (x=1..2) USARTx (x=1...5)(6) LPUART1(6) I2Cx (x=1...3)(7) LPTIMx (x=1,2) OTG_FS(8) SWPMI1(9)	108 µA	0.7 µs in SRAM 4.5 µs in Flash
	Range 2								

By default, the microcontroller is in Run mode after a system or a power Reset. It is up to the user to select one of the low-power modes described below:

- **Sleep** mode

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.
- **Low-power run** mode

  This mode is achieved with VCORE supplied by the low-power regulator to minimize the regulator's operating current. The code can be executed from SRAM or from Flash, and the CPU frequency is limited to 2 MHz. The peripherals with independent clock can be clocked by HSI16.
- **Low-power sleep** mode

  This mode is entered from the low-power run mode. Only the CPU clock is stopped. When wakeup is triggered by an event or an interrupt, the system reverts to the low-power run mode.
- **Stop 0, Stop 1 and Stop 2** modes

  Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. All clocks in the VCORE domain are stopped, the PLL, the MSI RC, the HSI16 RC and the HSE crystal oscillators are disabled. The LSE or LSI is still running.

  The RTC can remain active (Stop mode with RTC, Stop mode without RTC).

  Some peripherals with wakeup capability can enable the HSI16 RC during Stop mode to detect their wakeup condition.

  Three Stop modes are available: Stop 0, Stop 1 and Stop 2 modes. In Stop 2 mode, most of the VCORE domain is put in a lower leakage mode.

  Stop 1 offers the largest number of active peripherals and wakeup sources, a smaller wakeup time but a higher consumption than Stop 2. In Stop 0 mode, the main regulator remains ON, allowing a very fast wakeup time but with much higher consumption.

  The system clock when exiting from Stop 0, Stop1 or Stop2 modes can be either MSI up to 48 MHz or HSI16, depending on software configuration.
- **Standby** mode

  The Standby mode is used to achieve the lowest power consumption with BOR. The internal regulator is switched off so that the VCORE domain is powered off. The PLL, the MSI RC, the HSI16 RC and the HSE crystal oscillators are also switched off.

  The RTC can remain active (Standby mode with RTC, Standby mode without RTC).

  The brown-out reset (BOR) always remains active in Standby mode.

  The state of each I/O during standby mode can be selected by software: I/O with internal pull-up, internal pull-down or floating.

  After entering Standby mode, SRAM1 and register contents are lost except for registers in the Backup domain and Standby circuitry. Optionally, SRAM2 can be retained in

Table 10. Timer feature comparison (continued)

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Complementary outputs
General-purpose	TIM16, TIM17	16-bit	Up	Any integer between 1 and 65536	Yes	1	1
Basic	TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No

3.25.1 Advanced-control timer (TIM1, TIM8)

The advanced-control timer can each be seen as a three-phase PWM multiplexed on 6 channels. They have complementary PWM outputs with programmable inserted dead-times. They can also be seen as complete general-purpose timers. The 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes) with full modulation capability (0-100%)
- One-pulse mode output

In debug mode, the advanced-control timer counter can be frozen and the PWM outputs disabled to turn off any power switches driven by these outputs.

Many features are shared with those of the general-purpose TIMx timers (described in *Section 3.25.2*) using the same architecture, so the advanced-control timers can work together with the TIMx timers via the Timer Link feature for synchronization or event chaining.

3.29 Low-power universal asynchronous receiver transmitter (LPUART)

The device embeds one Low-Power UART. The LPUART supports asynchronous serial communication with minimum power consumption. It supports half duplex single wire communication and modem operations (CTS/RTS). It allows multiprocessor communication.

The LPUART has a clock domain independent from the CPU clock, and can wakeup the system from Stop mode using baudrates up to 220 Kbaud. The wake up events from Stop mode are programmable and can be:

- Start bit detection
- Any received data frame
- A specific programmed data frame

Only a 32.768 kHz clock (LSE) is needed to allow LPUART communication up to 9600 baud. Therefore, even in Stop mode, the LPUART can wait for an incoming frame while having an extremely low energy consumption. Higher speed clock can be used to reach higher baudrates.

LPUART interface can be served by the DMA controller.

Table 14. Legend/abbreviations used in the pinout table

Name	Abbreviation	Definition
Pin name	Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type	S	Supply pin
	I	Input only pin
	I/O	Input / output pin
I/O structure	FT	5 V tolerant I/O
	TT	3.6 V tolerant I/O
	B	Dedicated BOOT0 pin
	RST	Bidirectional reset pin with embedded weak pull-up resistor
	Option for TT or FT I/Os	
	_f (1)	I/O, Fm+ capable
	_l (2)	I/O, with LCD function supplied by V_{LCD}
	_u (3)	I/O, with USB function supplied by V_{DDUSB}
	_a (4)	I/O, with Analog switch function supplied by V_{DDA}
	_s (5)	I/O supplied only by V_{DDIO2}
Notes	Unless otherwise specified by a note, all I/Os are set as analog inputs during and after reset.	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers
	Additional functions	Functions directly selected/enabled through peripheral registers

1. The related I/O structures in *Table 15* are: FT_f, FT_fa, FT_fl, FT_fla.
2. The related I/O structures in *Table 15* are: FT_l, FT_fl, FT_lu.
3. The related I/O structures in *Table 15* are: FT_u, FT_lu.
4. The related I/O structures in *Table 15* are: FT_a, FT_la, FT_fa, FT_fla, TT_a, TT_la.
5. The related I/O structures in *Table 15* are: FT_s, FT_fs.

Table 16. Alternate function AF0 to AF7 (for AF8 to AF15 see *Table 17*) (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS_AF	**TIM1/TIM2/ TIM5/TIM8/ LPTIM1**	**TIM1/TIM2/ TIM3/TIM4/ TIM5**	**TIM8**	**I2C1/I2C2/I2C3**	**SPI1/SPI2**	**SPI3/DFSDM**	**USART1/ USART2/ USART3**
Port C	PC0	-	LPTIM1_IN1	-	-	I2C3_SCL	-	DFSDM1_ DATIN4	-
	PC1	-	LPTIM1_OUT	-	-	I2C3_SDA	-	DFSDM1_CKIN4	-
	PC2	-	LPTIM1_IN2	-	-	-	SPI2_MISO	DFSDM1_ CKOUT	-
	PC3	-	LPTIM1_ETR	-	-	-	SPI2_MOSI	-	-
	PC4	-	-	-	-	-	-	-	USART3_TX
	PC5	-	-	-	-	-	-	-	USART3_RX
	PC6	-	-	TIM3_CH1	TIM8_CH1	-	-	DFSDM1_CKIN3	-
	PC7	-	-	TIM3_CH2	TIM8_CH2	-	-	DFSDM1_ DATIN3	-
	PC8	-	-	TIM3_CH3	TIM8_CH3	-	-	-	-
	PC9	-	TIM8_BKIN2	TIM3_CH4	TIM8_CH4	-	-	-	-
	PC10	-	-	-	-	-	-	SPI3_SCK	USART3_TX
	PC11	-	-	-	-	-	-	SPI3_MISO	USART3_RX
	PC12	-	-	-	-	-	-	SPI3_MOSI	USART3_CK
	PC13	-	-	-	-	-	-	-	-
	PC14	-	-	-	-	-	-	-	-
	PC15	-	-	-	-	-	-	-	-

Table 16. Alternate function AF0 to AF7 (for AF8 to AF15 see *Table 17*) (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS_AF	TIM1/TIM2/ TIM5/TIM8/ LPTIM1	TIM1/TIM2/ TIM3/TIM4/ TIM5	TIM8	I2C1/I2C2/I2C3	SPI1/SPI2	SPI3/DFSDM	USART1/ USART2/ USART3
Port F	PF0	-	-	-	-	I2C2_SDA	-	-	-
	PF1	-	-	-	-	I2C2_SCL	-	-	-
	PF2	-	-	-	-	I2C2_SMBA	-	-	-
	PF3	-	-	-	-	-	-	-	-
	PF4	-	-	-	-	-	-	-	-
	PF5	-	-	-	-	-	-	-	-
	PF6	-	TIM5_ETR	TIM5_CH1	-	-	-	-	-
	PF7	-	-	TIM5_CH2	-	-	-	-	-
	PF8	-	-	TIM5_CH3	-	-	-	-	-
	PF9	-	-	TIM5_CH4	-	-	-	-	-
	PF10	-	-	-	-	-	-	-	-
	PF11	-	-	-	-	-	-	-	-
	PF12	-	-	-	-	-	-	-	-
	PF13	-	-	-	-	-	-	DFSDM1_ DATIN6	-
	PF14	-	-	-	-	-	-	DFSDM1_CKIN6	-
	PF15	-	-	-	-	-	-	-	-

Table 18. STM32L486xx memory map and peripheral register boundary addresses[(1)] (continued)

Bus	Boundary address	Size (bytes)	Peripheral
APB1	0x4000 9800 - 0x4000 FFFF	26 KB	Reserved
	0x4000 9400 - 0x4000 97FF	1 KB	LPTIM2
	0x4000 8C00 - 0x4000 93FF	2 KB	Reserved
	0x4000 8800 - 0x4000 8BFF	1 KB	SWPMI1
	0x4000 8400 - 0x4000 87FF	1 KB	Reserved
	0x4000 8000 - 0x4000 83FF	1 KB	LPUART1
	0x4000 7C00 - 0x4000 7FFF	1 KB	LPTIM1
	0x4000 7800 - 0x4000 7BFF	1 KB	OPAMP
	0x4000 7400 - 0x4000 77FF	1 KB	DAC
	0x4000 7000 - 0x4000 73FF	1 KB	PWR
	0x4000 6800 - 0x4000 6FFF	1 KB	Reserved
	0x4000 6400 - 0x4000 67FF	1 KB	CAN1
	0x4000 6000 - 0x4000 63FF	1 KB	Reserved
	0x4000 5C00- 0x4000 5FFF	1 KB	I2C3
	0x4000 5800 - 0x4000 5BFF	1 KB	I2C2
	0x4000 5400 - 0x4000 57FF	1 KB	I2C1
	0x4000 5000 - 0x4000 53FF	1 KB	UART5
	0x4000 4C00 - 0x4000 4FFF	1 KB	UART4

Table 18. STM32L486xx memory map and peripheral register boundary addresses[1] (continued)

Bus	Boundary address	Size (bytes)	Peripheral
APB1	0x4000 4800 - 0x4000 4BFF	1 KB	USART3
	0x4000 4400 - 0x4000 47FF	1 KB	USART2
	0x4000 4000 - 0x4000 43FF	1 KB	Reserved
	0x4000 3C00 - 0x4000 3FFF	1 KB	SPI3
	0x4000 3800 - 0x4000 3BFF	1 KB	SPI2
	0x4000 3400 - 0x4000 37FF	1 KB	Reserved
	0x4000 3000 - 0x4000 33FF	1 KB	IWDG
	0x4000 2C00 - 0x4000 2FFF	1 KB	WWDG
	0x4000 2800 - 0x4000 2BFF	1 KB	RTC
	0x4000 2400 - 0x4000 27FF	1 KB	LCD
	0x4000 1800 - 0x4000 23FF	3 KB	Reserved
	0x4000 1400 - 0x4000 17FF	1 KB	TIM7
	0x4000 1000 - 0x4000 13FF	1 KB	TIM6
	0x4000 0C00- 0x4000 0FFF	1 KB	TIM5
	0x4000 0800 - 0x4000 0BFF	1 KB	TIM4
	0x4000 0400 - 0x4000 07FF	1 KB	TIM3
	0x4000 0000 - 0x4000 03FF	1 KB	TIM2

1. The gray color is used for reserved boundary addresses.

Table 22. General operating conditions (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
T_A	Ambient temperature for the suffix 6 version	Maximum power dissipation	–40	85	°C
		Low-power dissipation(5)	–40	105	
	Ambient temperature for the suffix 7 version	Maximum power dissipation	–40	105	
		Low-power dissipation(5)	–40	125	
	Ambient temperature for the suffix 3 version	Maximum power dissipation	–40	125	
		Low-power dissipation(5)	–40	130	
T_J	Junction temperature range	Suffix 6 version	–40	105	°C
		Suffix 7 version	–40	125	
		Suffix 3 version	–40	130	

1. When RESET is released functionality is guaranteed down to V_{BOR0} Min.
2. This formula has to be applied only on the power supplies related to the IO structure described by the pin definition table. Maximum I/O input voltage is the smallest value between MIN(V_{DD}, V_{DDA}, V_{DDIO2}, V_{DDUSB}, V_{LCD})+3.6 V and 5.5V.
3. For operation with voltage higher than Min (V_{DD}, V_{DDA}, V_{DDIO2}, V_{DDUSB}, V_{LCD}) +0.3 V, the internal Pull-up and Pull-Down resistors must be disabled.
4. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_{Jmax} (see *Section 7.6: Thermal characteristics*).
5. In low-power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax} (see *Section 7.6: Thermal characteristics*).

6.3.2 Operating conditions at power-up / power-down

The parameters given in *Table 23* are derived from tests performed under the ambient temperature condition summarized in *Table 22*.

Table 23. Operating conditions at power-up / power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	-	0	∞	µs/V
	V_{DD} fall time rate		10	∞	
t_{VDDA}	V_{DDA} rise time rate	-	0	∞	µs/V
	V_{DDA} fall time rate		10	∞	
t_{VDDUSB}	V_{DDUSB} rise time rate	-	0	∞	µs/V
	V_{DDUSB} fall time rate		10	∞	
t_{VDDIO2}	V_{DDIO2} rise time rate	-	0	∞	µs/V
	V_{DDIO2} fall time rate		10	∞	

6.3.3 Embedded reset and power control block characteristics

The parameters given in *Table 24* are derived from tests performed under the ambient temperature conditions summarized in *Table 22: General operating conditions*.

Table 24. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions(1)	Min	Typ	Max	Unit
$t_{RSTTEMPO}$(2)	Reset temporization after BOR0 is detected	V_{DD} rising	-	250	400	µs
V_{BOR0}(2)	Brown-out reset threshold 0	Rising edge	1.62	1.66	1.7	V
		Falling edge	1.6	1.64	1.69	
V_{BOR1}	Brown-out reset threshold 1	Rising edge	2.06	2.1	2.14	V
		Falling edge	1.96	2	2.04	
V_{BOR2}	Brown-out reset threshold 2	Rising edge	2.26	2.31	2.35	V
		Falling edge	2.16	2.20	2.24	
V_{BOR3}	Brown-out reset threshold 3	Rising edge	2.56	2.61	2.66	V
		Falling edge	2.47	2.52	2.57	
V_{BOR4}	Brown-out reset threshold 4	Rising edge	2.85	2.90	2.95	V
		Falling edge	2.76	2.81	2.86	
V_{PVD0}	Programmable voltage detector threshold 0	Rising edge	2.1	2.15	2.19	V
		Falling edge	2	2.05	2.1	
V_{PVD1}	PVD threshold 1	Rising edge	2.26	2.31	2.36	V
		Falling edge	2.15	2.20	2.25	
V_{PVD2}	PVD threshold 2	Rising edge	2.41	2.46	2.51	V
		Falling edge	2.31	2.36	2.41	
V_{PVD3}	PVD threshold 3	Rising edge	2.56	2.61	2.66	V
		Falling edge	2.47	2.52	2.57	
V_{PVD4}	PVD threshold 4	Rising edge	2.69	2.74	2.79	V
		Falling edge	2.59	2.64	2.69	
V_{PVD5}	PVD threshold 5	Rising edge	2.85	2.91	2.96	V
		Falling edge	2.75	2.81	2.86	
V_{PVD6}	PVD threshold 6	Rising edge	2.92	2.98	3.04	V
		Falling edge	2.84	2.90	2.96	
V_{hyst_BORH0}	Hysteresis voltage of BORH0	Hysteresis in continuous mode	-	20	-	mV
		Hysteresis in other mode	-	30	-	
$V_{hyst\_BOR\_PVD}$	Hysteresis voltage of BORH (except BORH0) and PVD	-	-	100	-	mV
I_{DD} (BOR_PVD)(2)	BOR(3) (except BOR0) and PVD consumption from V_{DD}	-	-	1.1	1.6	µA
V_{PVM1}	V_{DDUSB} peripheral voltage monitoring	-	1.18	1.22	1.26	V

Table 39. Current consumption in VBAT mode

Symbol	Parameter	Conditions		TYP					MAX[1]					Unit
		-	V_{BAT}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD}(VBAT)	Backup domain supply current	RTC disabled	1.8 V	4	29	196	587	1663	10.8	73	490	1468	4158	nA
			2.4 V	5.27	36	226	673	1884	13.2	90	565	1683	4710	
			3 V	6	42	264	775	2147	15.5	106	660	1938	5368	
			3.6 V	10	58	323	919	2488	25.8	144	808	2298	6220	
		RTC enabled and clocked by LSE bypassed at 32768 Hz	1.8 V	183	201	367	729	-	-	-	-	-	-	
			2.4 V	268	295	486	901	-	-	-	-	-	-	
			3 V	376	412	602	1075	-	-	-	-	-	-	
			3.6 V	508	558	752	1299	-	-	-	-	-	-	
		RTC enabled and clocked by LSE quartz[2]	1.8 V	302	344	521	915	1978	-	-	-	-	-	
			2.4 V	388	436	639	1091	2289	-	-	-	-	-	
			3 V	494	549	784	1301	2656	-	-	-	-	-	
			3.6 V	630	692	971	1571	3115	-	-	-	-	-	

1. Guaranteed by characterization results, unless otherwise specified.
2. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.

Table 41. Low-power mode wakeup timings[1] (continued)

Symbol	Parameter	Conditions		Typ	Max	Unit
$t_{WUSTOP1}$	Wake up time from Stop 1 mode to Run mode in Flash	Range 1	Wakeup clock MSI = 48 MHz	6.2	10.2	µs
			Wakeup clock HSI16 = 16 MHz	6.3	8.99	
		Range 2	Wakeup clock MSI = 24 MHz	6.3	10.46	
			Wakeup clock HSI16 = 16 MHz	6.3	8.87	
			Wakeup clock MSI = 4 MHz	8.0	13.23	
	Wake up time from Stop 1 mode to Run mode in SRAM1	Range 1	Wakeup clock MSI = 48 MHz	4.5	5.78	
			Wakeup clock HSI16 = 16 MHz	5.5	7.1	
		Range 2	Wakeup clock MSI = 24 MHz	5.0	6.5	
			Wakeup clock HSI16 = 16 MHz	5.5	7.1	
			Wakeup clock MSI = 4 MHz	8.2	13.5	
	Wake up time from Stop 1 mode to Low-power run mode in Flash	Regulator in low-power mode (LPR=1 in PWR_CR1)	Wakeup clock MSI = 2 MHz	12.7	20	
	Wake up time from Stop 1 mode to Low-power run mode in SRAM1			10.7	21.5	
$t_{WUSTOP2}$	Wake up time from Stop 2 mode to Run mode in Flash	Range 1	Wakeup clock MSI = 48 MHz	8.0	9.4	µs
			Wakeup clock HSI16 = 16 MHz	7.3	9.3	
		Range 2	Wakeup clock MSI = 24 MHz	8.2	9.9	
			Wakeup clock HSI16 = 16 MHz	7.3	9.3	
			Wakeup clock MSI = 4 MHz	10.6	15.8	
	Wake up time from Stop 2 mode to Run mode in SRAM1	Range 1	Wakeup clock MSI = 48 MHz	5.1	6.7	
			Wakeup clock HSI16 = 16 MHz	5.7	8	
		Range 2	Wakeup clock MSI = 24 MHz	5.5	6.65	
			Wakeup clock HSI16 = 16 MHz	5.7	7.53	
			Wakeup clock MSI = 4 MHz	8.2	16.6	
t_{WUSTBY}	Wakeup time from Standby mode to Run mode	Range 1	Wakeup clock MSI = 8 MHz	14.3	20.8	µs
			Wakeup clock MSI = 4 MHz	20.1	35.5	
$t_{WUSTBY SRAM2}$	Wakeup time from Standby with SRAM2 to Run mode	Range 1	Wakeup clock MSI = 8 MHz	14.3	24.3	µs
			Wakeup clock MSI = 4 MHz	20.1	38.5	
t_{WUSHDN}	Wakeup time from Shutdown mode to Run mode	Range 1	Wakeup clock MSI = 4 MHz	256	330.6	µs

1. Guaranteed by characterization results.

Equation 1: R_{AIN} max formula

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The formula above (*Equation 1*) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

Table 65. Maximum ADC RAIN[(1)(2)]

Resolution	Sampling cycle @80 MHz	Sampling time [ns] @80 MHz	RAIN max (Ω)	
			Fast channels(3)	Slow channels(4)
12 bits	2.5	31.25	100	N/A
	6.5	81.25	330	100
	12.5	156.25	680	470
	24.5	306.25	1500	1200
	47.5	593.75	2200	1800
	92.5	1156.25	4700	3900
	247.5	3093.75	12000	10000
	640.5	8006.75	39000	33000
10 bits	2.5	31.25	120	N/A
	6.5	81.25	390	180
	12.5	156.25	820	560
	24.5	306.25	1500	1200
	47.5	593.75	2200	1800
	92.5	1156.25	5600	4700
	247.5	3093.75	12000	10000
	640.5	8006.75	47000	39000
8 bits	2.5	31.25	180	N/A
	6.5	81.25	470	270
	12.5	156.25	1000	680
	24.5	306.25	1800	1500
	47.5	593.75	2700	2200
	92.5	1156.25	6800	5600
	247.5	3093.75	15000	12000
	640.5	8006.75	50000	50000

Table 72. VREFBUF characteristics[1] (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DDA}(VREF BUF)	VREFBUF consumption from V_{DDA}	I_{load} = 0 µA	-	16	25	µA
		I_{load} = 500 µA	-	18	30	
		I_{load} = 4 mA	-	35	50	

1. Guaranteed by design, unless otherwise specified.
2. In degraded mode, the voltage reference buffer can not maintain accurately the output voltage which will follow (V_{DDA} - drop voltage).
3. Guaranteed by test in production.
4. The capacitive load must include a 100 nF capacitor in order to cut-off the high frequency noise.
5. To correctly control the VREFBUF inrush current during start-up phase and scaling change, the V_{DDA} voltage should be in the range [2.4 V to 3.6 V] and [2.8 V to 3.6 V] respectively for V_{RS} = 0 and V_{RS} = 1.

6.3.27 Communication interfaces characteristics

I²C interface characteristics

The I2C interface meets the timings requirements of the I²C-bus specification and user manual rev. 03 for:

- Standard-mode (Sm): with a bit rate up to 100 kbit/s
- Fast-mode (Fm): with a bit rate up to 400 kbit/s
- Fast-mode Plus (Fm+): with a bit rate up to 1 Mbit/s.

The I2C timings requirements are guaranteed by design when the I2C peripheral is properly configured (refer to RM0351 reference manual).

The SDA and SCL I/O requirements are met with the following restrictions: the SDA and SCL I/O pins are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DDIOx} is disabled, but is still present. Only FT_f I/O pins support Fm+ low level output current maximum requirement. Refer to *Section 6.3.14: I/O port characteristics* for the I2C I/Os characteristics.

All I2C SDA and SCL I/Os embed an analog filter. Refer to the table below for the analog filter characteristics:

Table 83. I2C analog filter characteristics(1)

Symbol	Parameter	Min	Max	Unit
t_{AF}	Maximum pulse width of spikes that are suppressed by the analog filter	50(2)	260(3)	ns

1. Guaranteed by design.
2. Spikes with widths below $t_{AF(min)}$ are filtered.
3. Spikes with widths above $t_{AF(max)}$ are not filtered

As applications do not commonly use the STM32L486xx at maximum dissipation, it is useful to calculate the exact power consumption and junction temperature to determine which temperature range will be best suited to the application.

The following examples show how to calculate the temperature range needed for a given application.

Example 1: High-performance application

Assuming the following application conditions:

Maximum ambient temperature T_{Amax} = 82 °C (measured according to JESD51-2), I_{DDmax} = 50 mA, V_{DD} = 3.5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V and maximum 8 I/Os used at the same time in output at low level with I_{OL} = 20 mA, V_{OL}= 1.3 V

P_{INTmax} = 50 mA × 3.5 V= 175 mW

P_{IOmax} = 20 × 8 mA × 0.4 V + 8 × 20 mA × 1.3 V = 272 mW

This gives: P_{INTmax} = 175 mW and P_{IOmax} = 272 mW:

P_{Dmax} = 175 + 272 = 447 mW

Using the values obtained in *Table 113* T_{Jmax} is calculated as follows:

– For LQFP64, 45 °C/W

T_{Jmax} = 82 °C + (45 °C/W × 447 mW) = 82 °C + 20.115 °C = 102.115 °C

This is within the range of the suffix 6 version parts (–40 < T_J < 105 °C) see *Section 8: Part numbering*.

In this case, parts must be ordered at least with the temperature range suffix 6 (see Part numbering).

Note: With this given P_{Dmax} we can find the T_{Amax} allowed for a given device temperature range (order code suffix 6 or 7).

Suffix 6: T_{Amax} = T_{Jmax} - (45°C/W × 447 mW) = 105-20.115 = 84.885 °C

Suffix 7: T_{Amax} = T_{Jmax} - (45°C/W × 447 mW) = 125-20.115 = 104.885 °C

Example 2: High-temperature application

Using the same rules, it is possible to address applications that run at high ambient temperatures with a low dissipation, as long as junction temperature T_J remains within the specified range.

Assuming the following application conditions:

Maximum ambient temperature T_{Amax} = 100 °C (measured according to JESD51-2), I_{DDmax} = 20 mA, V_{DD} = 3.5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V

P_{INTmax} = 20 mA × 3.5 V= 70 mW

P_{IOmax} = 20 × 8 mA × 0.4 V = 64 mW

This gives: P_{INTmax} = 70 mW and P_{IOmax} = 64 mW:

P_{Dmax} = 70 + 64 = 134 mW

Thus: P_{Dmax} = 134 mW

Using the values obtained in *Table 113* T_{Jmax} is calculated as follows:

– For LQFP64, 45 °C/W

T_{Jmax} = 100 °C + (45 °C/W × 134 mW) = 100 °C + 6.03 °C = 106.03 °C

This is above the range of the suffix 6 version parts (–40 < T_J < 105 °C).

In this case, parts must be ordered at least with the temperature range suffix 7 (see *Section 8: Part numbering*) unless we reduce the power dissipation in order to be able to use suffix 6 parts.

Refer to *Figure 64* to select the required temperature range (suffix 6 or 7) according to your ambient temperature or power requirements.

Figure 64. LQFP64 P_D max vs. T_A