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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, I²C, IrDA, LINbus, MMC/SD, QSPI, SAI, SPI, SWPMI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, LCD, PWM, WDT
Number of I/O	51
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l486rgt7

Table 2. STM32L486xx family device features and peripheral counts (continued)

Peripheral	STM32L486Zx	STM32L486Qx	STM32L486Vx	STM32L486Jx	STM32L486Rx
GPIOs Wakeup pins Nb of I/Os down to 1.08 V	114 5 14	109 5 14	82 5 0	57 4 6	51 4 0
Capacitive sensing Number of channels	24	24	21	12	12
12-bit ADCs Number of channels	3 24	3 19	3 16	3 16	3 16
12-bit DAC channels	2				
Internal voltage reference buffer	Yes				No
Analog comparator	2				
Operational amplifiers	2				
Max. CPU frequency	80 MHz				
Operating voltage	1.71 to 3.6 V				
Operating temperature	Ambient operating temperature: -40 to 85 °C / -40 to 105 °C / -40 to 125 °C Junction temperature: -40 to 105 °C / -40 to 125 °C / -40 to 130 °C				
Packages	LQFP144	UFBGA132	LQFP100	WLCSP72	LQFP64

1. For the LQFP100 package, only FMC Bank1 is available. Bank1 can only support a multiplexed NOR/PSRAM memory using the NE1 Chip Select.

Table 4. STM32L486xx modes overview (continued)

Mode	Regulator (1)	CPU	Flash	SRAM	Clocks	DMA & Peripherals(2)	Wakeup source	Consumption(3)	Wakeup time
Stop 1	LPR	No	Off	ON	LSE LSI	BOR, PVD, PVM RTC, LCD,IWDG COMPx (x=1,2) DACx (x=1,2) OPAMPx (x=1,2) USARTx (x=1...5)(6) LPUART1(6) I2Cx (x=1...3)(7) LPTIMx (x=1,2) *** All other peripherals are frozen.	Reset pin, all I/Os BOR, PVD, PVM RTC, LCD,IWDG COMPx (x=1..2) USARTx (x=1...5)(6) LPUART1(6) I2Cx (x=1...3)(7) LPTIMx (x=1,2) OTG_FS(8) SWPMI1(9)	6.6 µA w/o RTC 6.9 µA w RTC	4 µs in SRAM 6 µs in Flash
Stop 2	LPR	No	Off	ON	LSE LSI	BOR, PVD, PVM RTC, LCD,IWDG COMPx (x=1..2) I2C3(7) LPUART1(6) LPTIM1 *** All other peripherals are frozen.	Reset pin, all I/Os BOR, PVD, PVM RTC, LCD,IWDG COMPx (x=1..2) I2C3(7) LPUART1(6) LPTIM1	1.1 µA w/o RTC 1.4 µA w/RTC	5 µs in SRAM 7 µs in Flash

The AES peripheral supports:

- Encryption/Decryption using AES Rijndael Block Cipher algorithm
- NIST FIPS 197 compliant implementation of AES encryption/decryption algorithm
- 128-bit and 256-bit register for storing the encryption, decryption or derivation key (4x 32-bit registers)
- Electronic codebook (ECB), Cipher block chaining (CBC), Counter mode (CTR), Galois Counter Mode (GCM), Galois Message Authentication Code mode (GMAC) and Cipher Message Authentication Code mode (CMAC) supported.
- Key scheduler
- Key derivation for decryption
- 128-bit data block processing
- 128-bit, 256-bit key length
- 1x32-bit INPUT buffer and 1x32-bit OUTPUT buffer.
- Register access supporting 32-bit data width only.
- One 128-bit Register for the initialization vector when AES is configured in CBC mode or for the 32-bit counter initialization when CTR mode is selected, GCM mode or CMAC mode.
- Automatic data flow control with support of direct memory access (DMA) using 2 channels, one for incoming data, and one for outcoming data.
- Suspend a message if another message with a higher priority needs to be processed

3.25 Timers and watchdogs

The STM32L486xx includes two advanced control timers, up to nine general-purpose timers, two basic timers, two low-power timers, two watchdog timers and a SysTick timer. The table below compares the features of the advanced control, general purpose and basic timers.

Table 10. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Complementary outputs
Advanced control	TIM1, TIM8	16-bit	Up, down, Up/down	Any integer between 1 and 65536	Yes	4	3
General-purpose	TIM2, TIM5	32-bit	Up, down, Up/down	Any integer between 1 and 65536	Yes	4	No
General-purpose	TIM3, TIM4	16-bit	Up, down, Up/down	Any integer between 1 and 65536	Yes	4	No
General-purpose	TIM15	16-bit	Up	Any integer between 1 and 65536	Yes	2	1

Table 10. Timer feature comparison (continued)

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Complementary outputs
General-purpose	TIM16, TIM17	16-bit	Up	Any integer between 1 and 65536	Yes	1	1
Basic	TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No

3.25.1 Advanced-control timer (TIM1, TIM8)

The advanced-control timer can each be seen as a three-phase PWM multiplexed on 6 channels. They have complementary PWM outputs with programmable inserted dead-times. They can also be seen as complete general-purpose timers. The 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes) with full modulation capability (0-100%)
- One-pulse mode output

In debug mode, the advanced-control timer counter can be frozen and the PWM outputs disabled to turn off any power switches driven by these outputs.

Many features are shared with those of the general-purpose TIMx timers (described in *Section 3.25.2*) using the same architecture, so the advanced-control timers can work together with the TIMx timers via the Timer Link feature for synchronization or event chaining.

This low-power timer supports the following features:

- 16-bit up counter with 16-bit autoreload register
- 16-bit compare register
- Configurable output: pulse, PWM
- Continuous/ one shot mode
- Selectable software/hardware input trigger
- Selectable clock source
  - Internal clock sources: LSE, LSI, HSI16 or APB clock
  - External clock source over LPTIM input (working even with no internal clock source running, used by pulse counter application).
- Programmable digital glitch filter
- Encoder mode (LPTIM1 only)

3.25.5 Infrared interface (IRTIM)

The STM32L486xx includes one infrared interface (IRTIM). It can be used with an infrared LED to perform remote control functions. It uses TIM16 and TIM17 output channels to generate output signal waveforms on IR_OUT pin.

3.25.6 Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 32 kHz internal RC (LSI) and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

3.25.7 System window watchdog (WWDG)

The window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.25.8 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source

Table 15. STM32L486xx pin definitions (continued)

Pin Number					Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	WLCSP72	LQFP100	UFBGA132	LQFP144					Alternate functions	Additional functions
35	G2	53	K11	75	PB14	I/O	FT_fl	-	TIM1_CH2N, TIM8_CH2N, I2C2_SDA, SPI2_MISO, DFSDM1_DATIN2, USART3_RTS_DE, TSC_G1_IO3, LCD_SEG14, SWPMI1_RX, SAI2_MCLK_A, TIM15_CH1, EVENTOUT	-
36	G1	54	K10	76	PB15	I/O	FT_l	-	RTC_REFIN, TIM1_CH3N, TIM8_CH3N, SPI2_MOSI, DFSDM1_CKIN2, TSC_G1_IO4, LCD_SEG15, SWPMI1_SUSPEND, SAI2_SD_A, TIM15_CH2, EVENTOUT	-
-	-	55	K9	77	PD8	I/O	FT_l	-	USART3_TX, LCD_SEG28, FMC_D13, EVENTOUT	-
-	-	56	K8	78	PD9	I/O	FT_l	-	USART3_RX, LCD_SEG29, FMC_D14, SAI2_MCLK_A, EVENTOUT	-
-	-	57	J12	79	PD10	I/O	FT_l	-	USART3_CK, TSC_G6_IO1, LCD_SEG30, FMC_D15, SAI2_SCK_A, EVENTOUT	-
-	-	58	J11	80	PD11	I/O	FT_l	-	USART3_CTS, TSC_G6_IO2, LCD_SEG31, FMC_A16, SAI2_SD_A, LPTIM2_ETR, EVENTOUT	-
-	-	59	J10	81	PD12	I/O	FT_l	-	TIM4_CH1, USART3_RTS_DE, TSC_G6_IO3, LCD_SEG32, FMC_A17, SAI2_FS_A, LPTIM2_IN1, EVENTOUT	-
-	-	60	H12	82	PD13	I/O	FT_l	-	TIM4_CH2, TSC_G6_IO4, LCD_SEG33, FMC_A18, LPTIM2_OUT, EVENTOUT	-
-	-	-	-	83	VSS	S	-	-	-	-
-	-	-	-	84	VDD	S	-	-	-	-

Table 15. STM32L486xx pin definitions (continued)

Pin Number					Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	WLCSP72	LQFP100	UFBGA132	LQFP144					Alternate functions	Additional functions
62	E8	96	B3	140	PB9	I/O	FT_fl	-	IR_OUT, TIM4_CH4, I2C1_SDA, SPI2_NSS, DFSDM1_CKIN6, CAN1_TX, LCD_COM3, SDMMC1_D5, SAI1_FS_A, TIM17_CH1, EVENTOUT	-
-	-	97	C3	141	PE0	I/O	FT_l	-	TIM4_ETR, LCD_SEG36, FMC_NBL0, TIM16_CH1, EVENTOUT	-
-	-	98	A2	142	PE1	I/O	FT_l	-	LCD_SEG37, FMC_NBL1, TIM17_CH1, EVENTOUT	-
63	A8	99	D3	143	VSS	S	-	-	-	-
64	A9	100	C4	144	VDD	S	-	-	-	-

1. PC13, PC14 and PC15 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is limited:
   - The speed should not exceed 2 MHz with a maximum load of 30 pF
   - These GPIOs must not be used as current sources (e.g. to drive an LED).
2. After a Backup domain power-up, PC13, PC14 and PC15 operate as GPIOs. Their function then depends on the content of the RTC registers which are not reset by the system reset. For details on how to manage these GPIOs, refer to the Backup domain and RTC register descriptions in the RM0351 reference manual.
3. After reset, these pins are configured as JTAG/SW debug alternate functions, and the internal pull-up on PA15, PA13, PB4 pins and the internal pull-down on PA14 pin are activated.

Table 16. Alternate function AF0 to AF7 (for AF8 to AF15 see *Table 17*)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS_AF	TIM1/TIM2/ TIM5/TIM8/ LPTIM1	TIM1/TIM2/ TIM3/TIM4/ TIM5	TIM8	I2C1/I2C2/I2C3	SPI1/SPI2	SPI3/DFSDM	USART1/ USART2/ USART3
Port A	PA0	-	TIM2_CH1	TIM5_CH1	TIM8_ETR	-	-	-	USART2_CTS
	PA1	-	TIM2_CH2	TIM5_CH2	-	-	-	-	USART2_RTS_ DE
	PA2	-	TIM2_CH3	TIM5_CH3	-	-	-	-	USART2_TX
	PA3	-	TIM2_CH4	TIM5_CH4	-	-	-	-	USART2_RX
	PA4	-	-	-	-	-	SPI1_NSS	SPI3_NSS	USART2_CK
	PA5	-	TIM2_CH1	TIM2_ETR	TIM8_CH1N	-	SPI1_SCK	-	-
	PA6	-	TIM1_BKIN	TIM3_CH1	TIM8_BKIN	-	SPI1_MISO	-	USART3_CTS
	PA7	-	TIM1_CH1N	TIM3_CH2	TIM8_CH1N	-	SPI1_MOSI	-	-
	PA8	MCO	TIM1_CH1	-	-	-	-	-	USART1_CK
	PA9	-	TIM1_CH2	-	-	-	-	-	USART1_TX
	PA10	-	TIM1_CH3	-	-	-	-	-	USART1_RX
	PA11	-	TIM1_CH4	TIM1_BKIN2	-	-	-	-	USART1_CTS
	PA12	-	TIM1_ETR	-	-	-	-	-	USART1_RTS_ DE
	PA13	JTMS-SWDIO	IR_OUT	-	-	-	-	-	-
	PA14	JTCK-SWCLK	-	-	-	-	-	-	-
	PA15	JTDI	TIM2_CH1	TIM2_ETR	-	-	SPI1_NSS	SPI3_NSS	-

Table 17. Alternate function AF8 to AF15 (for AF0 to AF7 see *Table 16*)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		UART4, UART5, LPUART1	CAN1, TSC	OTG_FS, QUADSPI	LCD	SDMMC1, COMP1, COMP2, FMC, SWPMI1	SAI1, SAI2	TIM2, TIM15, TIM16, TIM17, LPTIM2	EVENTOUT
Port A	PA0	UART4_TX	-	-	-	-	SAI1_EXTCLK	TIM2_ETR	EVENTOUT
	PA1	UART4_RX	-	-	LCD_SEG0	-	-	TIM15_CH1N	EVENTOUT
	PA2	-	-	-	LCD_SEG1	-	SAI2_EXTCLK	TIM15_CH1	EVENTOUT
	PA3	-	-	-	LCD_SEG2	-	-	TIM15_CH2	EVENTOUT
	PA4	-	-	-	-	-	SAI1_FS_B	LPTIM2_OUT	EVENTOUT
	PA5	-	-	-	-	-	-	LPTIM2_ETR	EVENTOUT
	PA6	-	-	QUADSPI_BK1_IO3	LCD_SEG3	TIM1_BKIN_ COMP2	TIM8_BKIN_ COMP2	TIM16_CH1	EVENTOUT
	PA7	-	-	QUADSPI_BK1_IO2	LCD_SEG4	-	-	TIM17_CH1	EVENTOUT
	PA8	-	-	OTG_FS_SOF	LCD_COM0	-	-	LPTIM2_OUT	EVENTOUT
	PA9	-	-	-	LCD_COM1	-	-	TIM15_BKIN	EVENTOUT
	PA10	-	-	OTG_FS_ID	LCD_COM2	-	-	TIM17_BKIN	EVENTOUT
	PA11	-	CAN1_RX	OTG_FS_DM	-	TIM1_BKIN2_ COMP1	-	-	EVENTOUT
	PA12	-	CAN1_TX	OTG_FS_DP	-	-	-	-	EVENTOUT
	PA13	-	-	OTG_FS_NOE	-	-	-	-	EVENTOUT
	PA14	-	-	-	-	-	-	-	EVENTOUT
	PA15	UART4_RTS _DE	TSC_G3_IO1	-	LCD_SEG17	-	SAI2_FS_B	-	EVENTOUT

Table 17. Alternate function AF8 to AF15 (for AF0 to AF7 see *Table 16*) (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		UART4, UART5, LPUART1	CAN1, TSC	OTG_FS, QUADSPI	LCD	SDMMC1, COMP1, COMP2, FMC, SWPMI1	SAI1, SAI2	TIM2, TIM15, TIM16, TIM17, LPTIM2	EVENTOUT
Port D	PD0	-	CAN1_RX	-	-	FMC_D2	-	-	EVENTOUT
	PD1	-	CAN1_TX	-	-	FMC_D3	-	-	EVENTOUT
	PD2	UART5_RX	TSC_SYNC	-	LCD_COM7/ LCD_SEG31/ LCD_SEG43	SDMMC1_CMD	-	-	EVENTOUT
	PD3	-	-	-	-	FMC_CLK	-	-	EVENTOUT
	PD4	-	-	-	-	FMC_NOE	-	-	EVENTOUT
	PD5	-	-	-	-	FMC_NWE	-	-	EVENTOUT
	PD6	-	-	-	-	FMC_NWAIT	SAI1_SD_A	-	EVENTOUT
	PD7	-	-	-	-	FMC_NE1	-	-	EVENTOUT
	PD8	-	-	-	LCD_SEG28	FMC_D13	-	-	EVENTOUT
	PD9	-	-	-	LCD_SEG29	FMC_D14	SAI2_MCLK_A	-	EVENTOUT
	PD10	-	TSC_G6_IO1	-	LCD_SEG30	FMC_D15	SAI2_SCK_A	-	EVENTOUT
	PD11	-	TSC_G6_IO2	-	LCD_SEG31	FMC_A16	SAI2_SD_A	LPTIM2_ETR	EVENTOUT
	PD12	-	TSC_G6_IO3	-	LCD_SEG32	FMC_A17	SAI2_FS_A	LPTIM2_IN1	EVENTOUT
	PD13	-	TSC_G6_IO4	-	LCD_SEG33	FMC_A18	-	LPTIM2_OUT	EVENTOUT
	PD14	-	-	-	LCD_SEG34	FMC_D0	-	-	EVENTOUT
	PD15	-	-	-	LCD_SEG35	FMC_D1	-	-	EVENTOUT

6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ±3σ).

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = V_{DDA} = 3 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean ±2σ).

6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 11*.

6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 12*.

Figure 11. Pin loading conditions

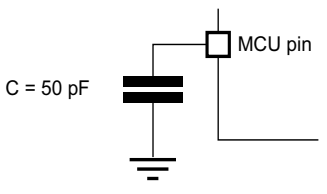


Figure 12. Pin input voltage

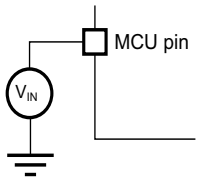


Table 35. Current consumption in Stop 1 mode (continued)

Symbol	Parameter	Conditions			TYP					MAX(1)					Unit
		-	-	V_{DD}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD} (wakeup from Stop1)	Supply current during wakeup from Stop 1	Wakeup clock MSI = 48 MHz, voltage Range 1. See (4).		3 V	1.47	-	-	-	-	-					mA
		Wakeup clock MSI = 4 MHz, voltage Range 2. See (4).		3 V	1.7	-	-	-	-						
		Wakeup clock HSI16 = 16 MHz, voltage Range 1. See (4).		3 V	1.62	-	-	-	-						

1. Guaranteed by characterization results, unless otherwise specified.
2. LCD enabled with external voltage source. Consumption from VLCD excluded. Refer to LCD controller characteristics for I_{VLCD}.
3. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.
4. Wakeup with code execution from Flash. Average value given for a typical wakeup time as specified in *Table 41: Low-power mode wakeup timings*.

Table 39. Current consumption in VBAT mode

Symbol	Parameter	Conditions		TYP					MAX(1)					Unit
		-	V_{BAT}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD}(VBAT)	Backup domain supply current	RTC disabled	1.8 V	4	29	196	587	1663	10.8	73	490	1468	4158	nA
			2.4 V	5.27	36	226	673	1884	13.2	90	565	1683	4710	
			3 V	6	42	264	775	2147	15.5	106	660	1938	5368	
			3.6 V	10	58	323	919	2488	25.8	144	808	2298	6220	
		RTC enabled and clocked by LSE bypassed at 32768 Hz	1.8 V	183	201	367	729	-	-	-	-	-	-	
			2.4 V	268	295	486	901	-	-	-	-	-	-	
			3 V	376	412	602	1075	-	-	-	-	-	-	
			3.6 V	508	558	752	1299	-	-	-	-	-	-	
		RTC enabled and clocked by LSE quartz(2)	1.8 V	302	344	521	915	1978	-	-	-	-	-	
			2.4 V	388	436	639	1091	2289	-	-	-	-	-	
			3 V	494	549	784	1301	2656	-	-	-	-	-	
			3.6 V	630	692	971	1571	3115	-	-	-	-	-	

1. Guaranteed by characterization results, unless otherwise specified.
2. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.

Table 59. I/O static characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{lkg}	FT_xx input leakage current(3)	$V_{IN} \le Max(V_{DDXXX})$(4)	-	-	±100	nA
		$Max(V_{DDXXX}) \le V_{IN} \le Max(V_{DDXXX})+1$ V(4)(5)	-	-	650(3)(6)	
		$Max(V_{DDXXX})+1$ V < VIN ≤ 5.5 V(3)(5)	-	-	200(6)	
	FT_lu, FT_u and PC3 IO	$V_{IN} \le Max(V_{DDXXX})$ (4)	-	-	±150	
		$Max(V_{DDXXX}) \le V_{IN} \le Max(V_{DDXXX})+1$ V(4)	-	-	2500(3)(7)	
		$Max(V_{DDXXX})+1$ V < VIN ≤ 5.5 V(4)(5)(7)	-	-	250(7)	
	TT_xx input leakage current	$V_{IN} \le Max(V_{DDXXX})$(6)	-	-	±150	
		$Max(V_{DDXXX}) \le V_{IN}$ < 3.6 V(6)	-	-	2000(3)	
	OPAMPx_VINM (x=1,2) dedicated input leakage current (UFBGA132 only)	-	-	-	(8)	
R_{PU}	Weak pull-up equivalent resistor (9)	$V_{IN} = V_{SS}$	25	40	55	kΩ
R_{PD}	Weak pull-down equivalent resistor(9)	$V_{IN} = V_{DDIOx}$	25	40	55	kΩ
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. Refer to *Figure 22: I/O input characteristics*.
2. Tested in production.
3. Guaranteed by design.
4. $Max(V_{DDXXX})$ is the maximum value of all the I/O supplies. Refer to *Table: Legend/Abbreviations used in the pinout table.*
5. All TX_xx IO except FT_lu, FT_u and PC3.
6. This value represents the pad leakage of the IO itself. The total product pad leakage is provided by this formula: $I_{Total\_Ileak\_max}$ = 10 µA + [number of IOs where V_{IN} is applied on the pad] x I_{lkg}(Max).
7. To sustain a voltage higher than MIN(V_{DD}, V_{DDA}, V_{DDIO2}, V_{DDUSB}, V_{LCD}) +0.3 V, the internal Pull-up and Pull-Down resistors must be disabled.
8. Refer to I_{bias} in *Table 74: OPAMP characteristics* for the values of the OPAMP dedicated input leakage current.
9. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimal (~10% order).

Table 65. Maximum ADC RAIN(1)(2) (continued)

Resolution	Sampling cycle @80 MHz	Sampling time [ns] @80 MHz	RAIN max (Ω)	
			Fast channels(3)	Slow channels(4)
6 bits	2.5	31.25	220	N/A
	6.5	81.25	560	330
	12.5	156.25	1200	1000
	24.5	306.25	2700	2200
	47.5	593.75	3900	3300
	92.5	1156.25	8200	6800
	247.5	3093.75	18000	15000
	640.5	8006.75	50000	50000

1. Guaranteed by design.
2. The I/O analog switch voltage booster is enable when V_{DDA} < 2.4 V (BOOSTEN = 1 in the SYSCFG_CFGR1 when V_{DDA} < 2.4V). It is disable when V_{DDA} ≥ 2.4 V.
3. Fast channels are: PC0, PC1, PC2, PC3, PA0, PA1.
4. Slow channels are: all ADC inputs except the fast channels.

Table 69. ADC accuracy - limited test conditions 4(1)(2)(3) (continued)

Symbol	Parameter	Conditions(4)			Min	Typ	Max	Unit
THD	Total harmonic distortion	ADC clock frequency ≤ 26 MHz, 1.65 V ≤ V_{DDA} = VREF+ ≤ 3.6 V, Voltage scaling Range 2	Single ended	Fast channel (max speed)	-	-71	-69	dB
				Slow channel (max speed)	-	-71	-69	
			Differential	Fast channel (max speed)	-	-73	-72	
				Slow channel (max speed)	-	-73	-72	

1. Guaranteed by design.
2. ADC DC accuracy values are measured after internal calibration.
3. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
4. The I/O analog switch voltage booster is enable when V_{DDA} < 2.4 V (BOOSTEN = 1 in the SYSCFG_CFGR1 when V_{DDA} < 2.4 V). It is disable when V_{DDA} ≥ 2.4 V. No oversampling.

Figure 25. ADC accuracy characteristics

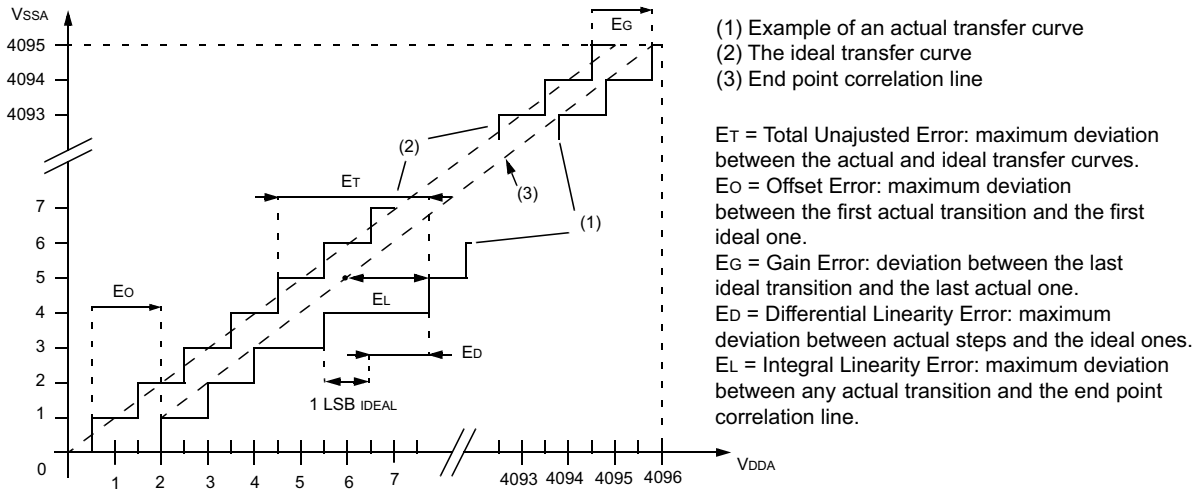
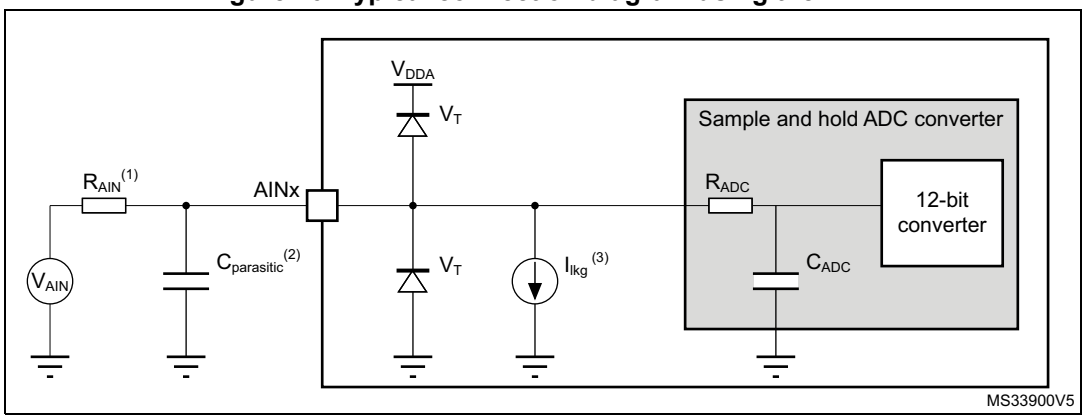


Figure 26. Typical connection diagram using the ADC

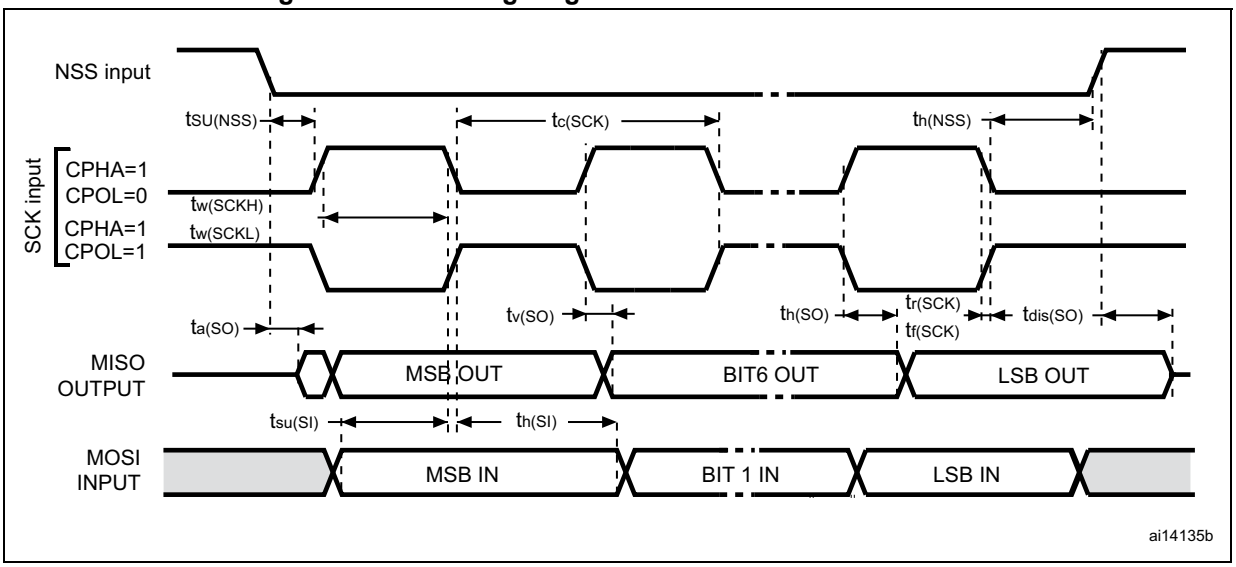


1. Refer to *Table 64: ADC characteristics* for the values of R_{AIN}, R_{ADC} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (refer to *Table 59: I/O static characteristics* for the value of the pad capacitance). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.
3. Refer to *Table 59: I/O static characteristics* for the values of I_{lkg}.

General PCB design guidelines

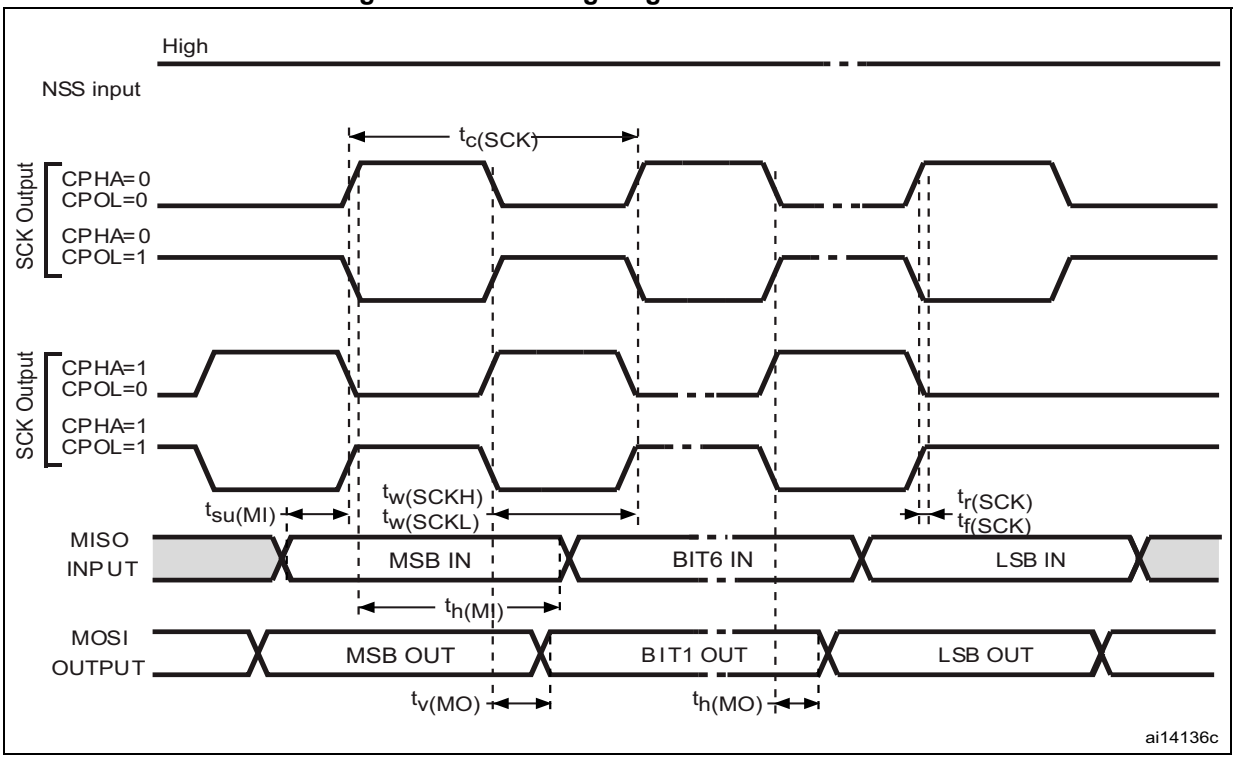
Power supply decoupling should be performed as shown in *Figure 13: Power supply scheme*. The 10 nF capacitor should be ceramic (good quality) and it should be placed as close as possible to the chip.

Figure 29. SPI timing diagram - slave mode and CPHA = 1



1. Measurement points are done at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

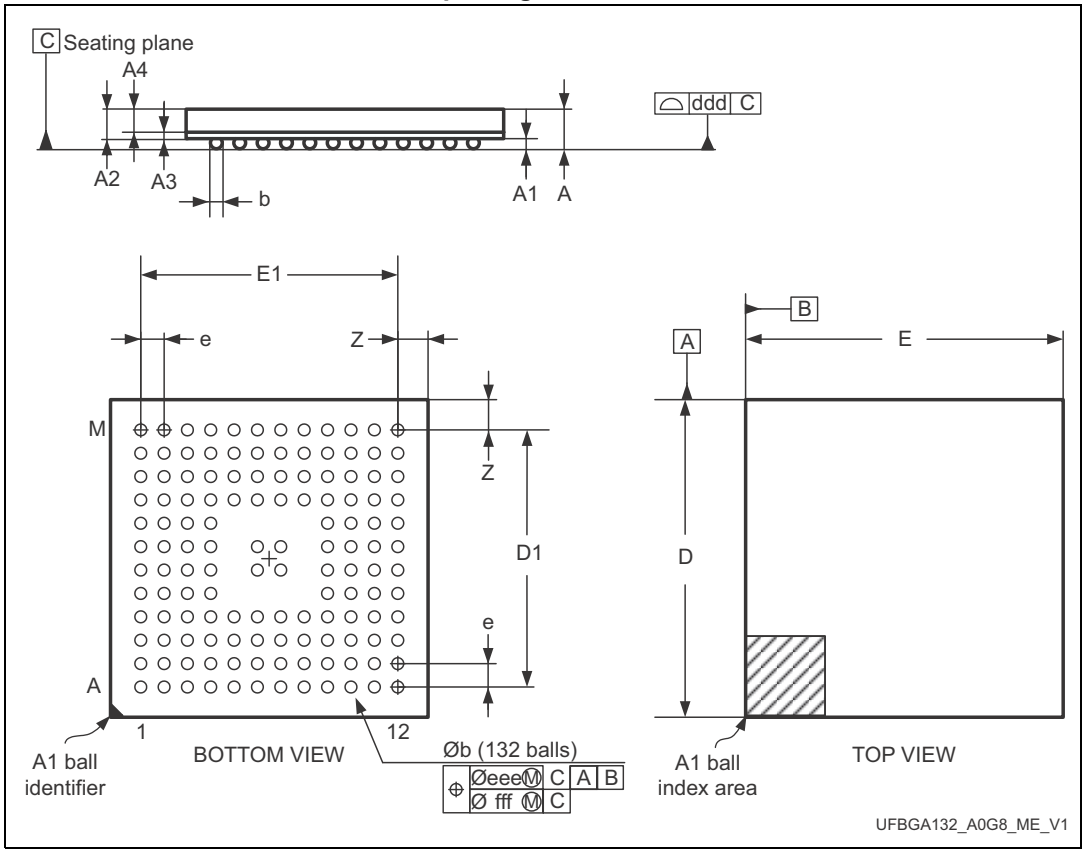
Figure 30. SPI timing diagram - master mode



1. Measurement points are done at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

7.2 UFBGA132 package information

Figure 52. UFBGA132 - 132-ball, 7 x 7 mm ultra thin fine pitch ball grid array package outline



1. Drawing is not to scale.

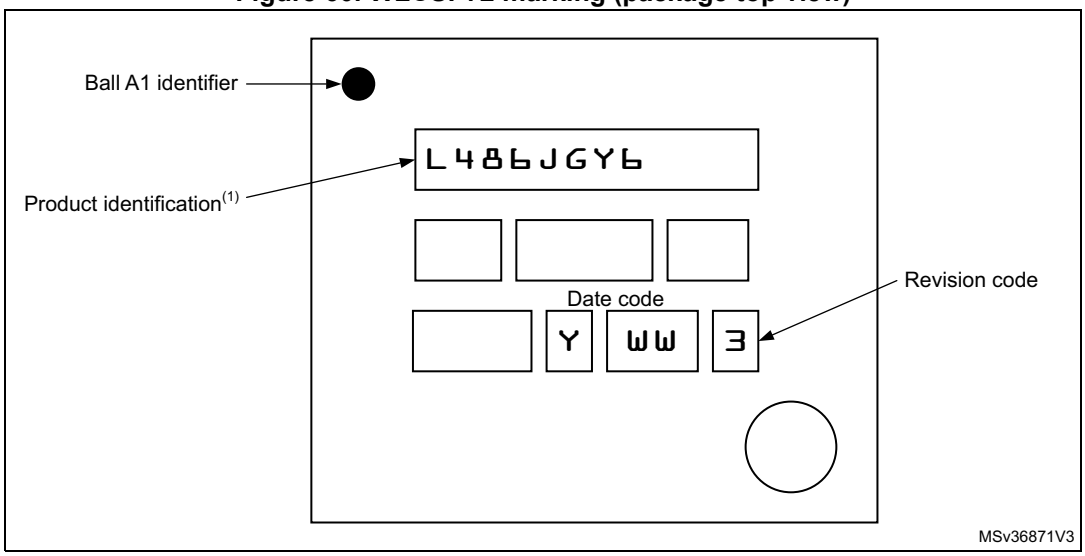
Table 107. UFBGA132 - 132-ball, 7 x 7 mm ultra thin fine pitch ball grid array package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	0.600	-	-	0.0236
A1	-	-	0.110	-	-	0.0043
A2	-	0.450	-	-	0.0177	-
A3	-	0.130	-	-	0.0051	0.0094
A4	-	0.320	-	-	0.0126	-
b	0.240	0.290	0.340	0.0094	0.0114	0.0134
D	6.850	7.000	7.150	0.2697	0.2756	0.2815
D1	-	5.500	-	-	0.2165	-
E	6.850	7.000	7.150	0.2697	0.2756	0.2815
E1	-	5.500	-	-	0.2165	-

Device marking

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

Figure 60. WLCSP72 marking (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.