STMicroelectronics - STM32L486VGT6TR Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, MMC/SD, QSPI, SAI, SPI, SWPMI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, LCD, PWM, WDT
Number of I/O	82
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l486vgt6tr

3.10 Interconnect matrix

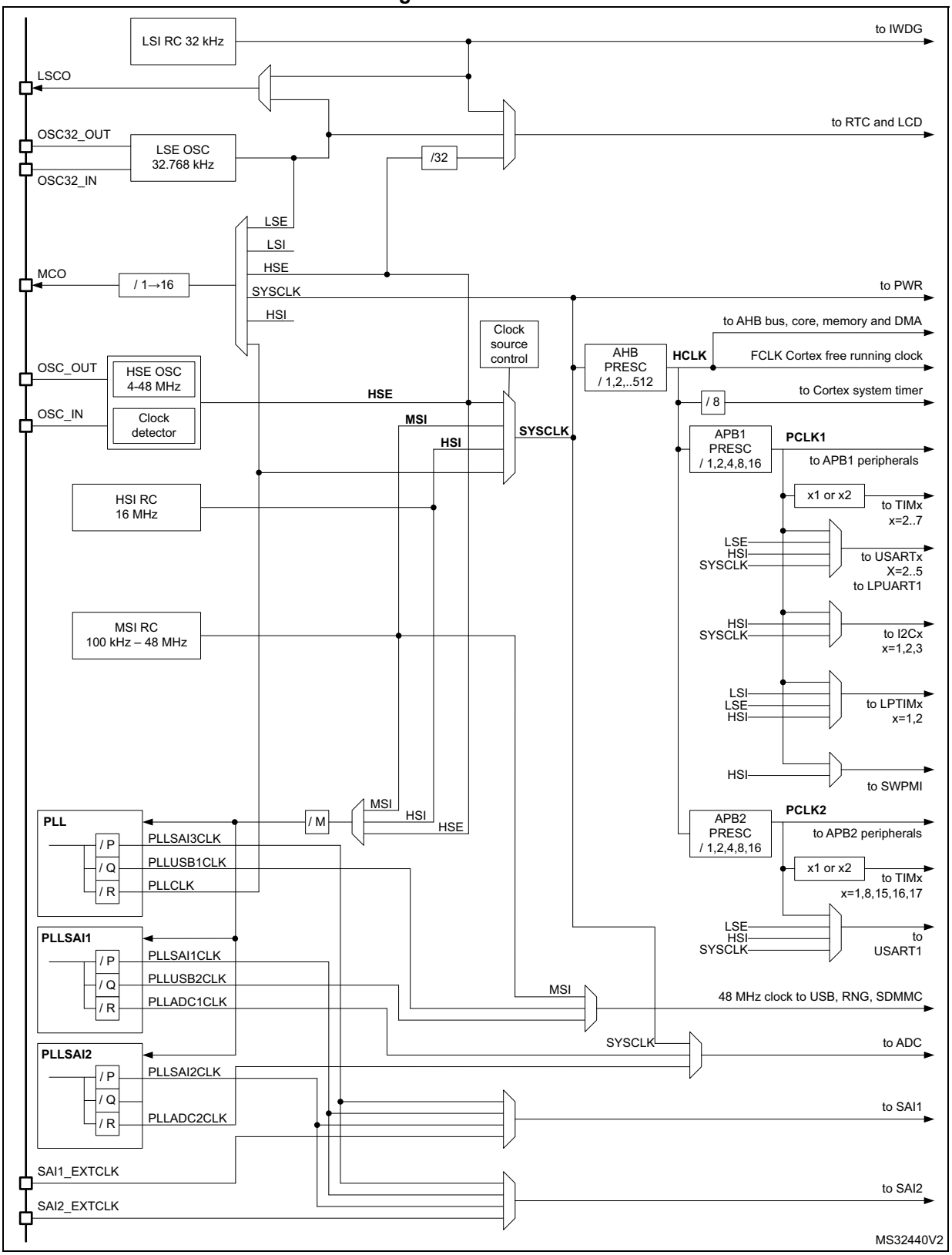
Several peripherals have direct connections between them. This allows autonomous communication between peripherals, saving CPU resources thus power supply consumption. In addition, these hardware connections allow fast and predictable latency.

Depending on peripherals, these interconnections can operate in Run, Sleep, low-power run and sleep, Stop 0, Stop 1 and Stop 2 modes.

Table 6. STM32L486xx peripherals interconnect matrix

Interconnect source	Interconnect destination	Interconnect action	Run	Sleep	Low-power run	Low-power sleep	Stop 0 / Stop 1	Stop 2
TIMx	TIMx	Timers synchronization or chaining	Y	Y	Y	Y	-	-
	ADCx DACx DFSDM1	Conversion triggers	Y	Y	Y	Y	-	-
	DMA	Memory to memory transfer trigger	Y	Y	Y	Y	-	-
	COMPx	Comparator output blanking	Y	Y	Y	Y	-	-
TIM16/TIM17	IRTIM	Infrared interface output generation	Y	Y	Y	Y	-	-
COMPx	TIM1, 8 TIM2, 3	Timer input channel, trigger, break from analog signals comparison	Y	Y	Y	Y	-	-
	LPTIMERx	Low-power timer triggered by analog signals comparison	Y	Y	Y	Y	Y	Y (1)
ADCx	TIM1, 8	Timer triggered by analog watchdog	Y	Y	Y	Y	-	-
RTC	TIM16	Timer input channel from RTC events	Y	Y	Y	Y	-	-
	LPTIMERx	Low-power timer triggered by RTC alarms or tampers	Y	Y	Y	Y	Y	Y (1)
All clocks sources (internal and external)	TIM2 TIM15, 16, 17	Clock source used as input channel for RC measurement and trimming	Y	Y	Y	Y	-	-
USB	TIM2	Timer triggered by USB SOF	Y	Y	-	-	-	-
CSS CPU (hard fault) RAM (parity error) Flash memory (ECC error) COMPx PVD DFSDM1 (analog watchdog, short circuit detection)	TIM1,8 TIM15,16,17	Timer break	Y	Y	Y	Y	-	-

Figure 3. Clock tree



- Transmission
  - Three transmit mailboxes
  - Configurable transmit priority
- Reception
  - Two receive FIFOs with three stages
  - 14 Scalable filter banks
  - Identifier list feature
  - Configurable FIFO overrun
- Time-triggered communication option
  - Disable automatic retransmission mode
  - 16-bit free running timer
  - Time Stamp sent in last two data bytes
- Management
  - Maskable interrupts
  - Software-efficient mailbox mapping at a unique address space

3.34 Secure digital input/output and MultiMediaCards Interface (SDMMC)

The card host interface (SDMMC) provides an interface between the APB peripheral bus and MultiMediaCards (MMCs), SD memory cards and SDIO cards.

The SDMMC features include the following:

- Full compliance with MultiMediaCard System Specification Version 4.2. Card support for three different databus modes: 1-bit (default), 4-bit and 8-bit
- Full compatibility with previous versions of MultiMediaCards (forward compatibility)
- Full compliance with SD Memory Card Specifications Version 2.0
- Full compliance with SD I/O Card Specification Version 2.0: card support for two different databus modes: 1-bit (default) and 4-bit
- Data transfer up to 48 MHz for the 8 bit mode
- Data write and read with DMA capability

3.35 Universal serial bus on-the-go full-speed (OTG_FS)

The devices embed an USB OTG full-speed device/host/OTG peripheral with integrated transceivers. The USB OTG FS peripheral is compliant with the USB 2.0 specification and with the OTG 2.0 specification. It has software-configurable endpoint setting and supports suspend/resume. The USB OTG controller requires a dedicated 48 MHz clock that can be provided by the internal multispeed oscillator (MSI) automatically trimmed by 32.768 kHz external oscillator (LSE).This allows to use the USB device without external high speed crystal (HSE).

3.37 Quad SPI memory interface (QUADSPI)

The Quad SPI is a specialized communication interface targeting single, dual or quad SPI flash memories. It can operate in any of the three following modes:

- Indirect mode: all the operations are performed using the QUADSPI registers
- Status polling mode: the external flash status register is periodically read and an interrupt can be generated in case of flag setting
- Memory-mapped mode: the external Flash is memory mapped and is seen by the system as if it were an internal memory

The Quad SPI interface supports:

- Three functional modes: indirect, status-polling, and memory-mapped
- SDR and DDR support
- Fully programmable opcode for both indirect and memory mapped mode
- Fully programmable frame format for both indirect and memory mapped mode
- Each of the 5 following phases can be configured independently (enable, length, single/dual/quad communication)
  - Instruction phase
  - Address phase
  - Alternate bytes phase
  - Dummy cycles phase
  - Data phase
- Integrated FIFO for reception and transmission
- 8, 16, and 32-bit data accesses are allowed
- DMA channel for indirect mode operations
- Programmable masking for external flash flag management
- Timeout management
- Interrupt generation on FIFO threshold, timeout, status match, operation complete, and access error

Table 15. STM32L486xx pin definitions (continued)

Pin Number					Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	WLCSP72	LQFP100	UFBGA132	LQFP144					Alternate functions	Additional functions
-	-	10	F2	16	VSS	S	-	-	-	-
-	-	11	G2	17	VDD	S	-	-	-	-
-	-	-	-	18	PF6	I/O	FT_a	-	TIM5_ETR, TIM5_CH1, SAI1_SD_B, EVENTOUT	ADC3_IN9
-	-	-	-	19	PF7	I/O	FT_a	-	TIM5_CH2, SAI1_MCLK_B, EVENTOUT	ADC3_IN10
-	-	-	-	20	PF8	I/O	FT_a	-	TIM5_CH3, SAI1_SCK_B, EVENTOUT	ADC3_IN11
-	-	-	-	21	PF9	I/O	FT_a	-	TIM5_CH4, SAI1_FS_B, TIM15_CH1, EVENTOUT	ADC3_IN12
-	-	-	-	22	PF10	I/O	FT_a	-	TIM15_CH2, EVENTOUT	ADC3_IN13
5	D9	12	F1	23	PH0-OSC_IN (PH0)	I/O	FT	-	EVENTOUT	OSC_IN
6	D8	13	G1	24	PH1-OSC_OUT (PH1)	I/O	FT	-	EVENTOUT	OSC_OUT
7	E9	14	H2	25	NRST	I/O	RST	-	-	-
8	F9	15	H1	26	PC0	I/O	FT_fla	-	LPTIM1_IN1, I2C3_SCL, DFSDM1_DATIN4, LPUART1_RX, LCD_SEG18, LPTIM2_IN1, EVENTOUT	ADC123_IN1
9	F8	16	J2	27	PC1	I/O	FT_fla	-	LPTIM1_OUT, I2C3_SDA, DFSDM1_CKIN4, LPUART1_TX, LCD_SEG19, EVENTOUT	ADC123_IN2
10	F7	17	J3	28	PC2	I/O	FT_la	-	LPTIM1_IN2, SPI2_MISO, DFSDM1_CKOUT, LCD_SEG20, EVENTOUT	ADC123_IN3
11	G7	18	K2	29	PC3	I/O	FT_a	-	LPTIM1_ETR, SPI2_MOSI, LCD_VLCD, SAI1_SD_A, LPTIM2_ETR, EVENTOUT	ADC123_IN4
-	-	19	-	30	VSSA	S	-	-	-	-
-	-	20	-	31	VREF-	S	-	-	-	-
12	G9	-	J1	-	VSSA/VREF-	S	-	-	-	-
-	G8	21	L1	32	VREF+	S	-	-	-	VREFBUF_OUT
-	H9	22	M1	33	VDDA	S	-	-	-	-
13	-	-	-	-	VDDA/VREF+	S	-	-	-	-

Table 16. Alternate function AF0 to AF7 (for AF8 to AF15 see *Table 17*)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS_AF	TIM1/TIM2/ TIM5/TIM8/ LPTIM1	TIM1/TIM2/ TIM3/TIM4/ TIM5	TIM8	I2C1/I2C2/I2C3	SPI1/SPI2	SPI3/DFSDM	USART1/ USART2/ USART3
Port A	PA0	-	TIM2_CH1	TIM5_CH1	TIM8_ETR	-	-	-	USART2_CTS
	PA1	-	TIM2_CH2	TIM5_CH2	-	-	-	-	USART2_RTS_ DE
	PA2	-	TIM2_CH3	TIM5_CH3	-	-	-	-	USART2_TX
	PA3	-	TIM2_CH4	TIM5_CH4	-	-	-	-	USART2_RX
	PA4	-	-	-	-	-	SPI1_NSS	SPI3_NSS	USART2_CK
	PA5	-	TIM2_CH1	TIM2_ETR	TIM8_CH1N	-	SPI1_SCK	-	-
	PA6	-	TIM1_BKIN	TIM3_CH1	TIM8_BKIN	-	SPI1_MISO	-	USART3_CTS
	PA7	-	TIM1_CH1N	TIM3_CH2	TIM8_CH1N	-	SPI1_MOSI	-	-
	PA8	MCO	TIM1_CH1	-	-	-	-	-	USART1_CK
	PA9	-	TIM1_CH2	-	-	-	-	-	USART1_TX
	PA10	-	TIM1_CH3	-	-	-	-	-	USART1_RX
	PA11	-	TIM1_CH4	TIM1_BKIN2	-	-	-	-	USART1_CTS
	PA12	-	TIM1_ETR	-	-	-	-	-	USART1_RTS_ DE
	PA13	JTMS-SWDIO	IR_OUT	-	-	-	-	-	-
	PA14	JTCK-SWCLK	-	-	-	-	-	-	-
	PA15	JTDI	TIM2_CH1	TIM2_ETR	-	-	SPI1_NSS	SPI3_NSS	-

6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ±3σ).

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = V_{DDA} = 3 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean ±2σ).

6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 11*.

6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 12*.

Figure 11. Pin loading conditions

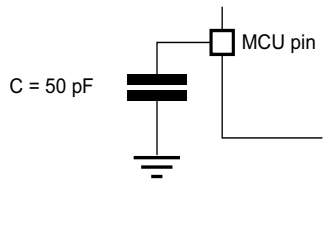
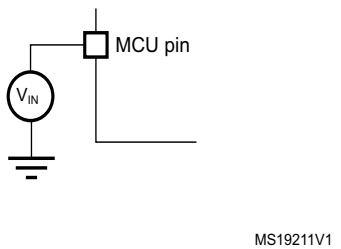


Figure 12. Pin input voltage



6.3.4 Embedded voltage reference

The parameters given in *Table 25* are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 22: General operating conditions*.

Table 25. Embedded internal voltage reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	–40 °C < T_A < +130 °C	1.182	1.212	1.232	V
$t_{S_vrefint}$ (1)	ADC sampling time when reading the internal reference voltage	-	4(2)	-	-	µs
$t_{start_vrefint}$	Start time of reference voltage buffer when ADC is enable	-	-	8	12(2)	µs
$I_{DD}(V_{REFINTBUF})$	V_{REFINT} buffer consumption from V_{DD} when converted by ADC	-	-	12.5	20(2)	µA
ΔV_{REFINT}	Internal reference voltage spread over the temperature range	V_{DD} = 3 V	-	5	7.5(2)	mV
T_{Coeff}	Average temperature coefficient	–40°C < T_A < +130°C	-	30	50(2)	ppm/°C
A_{Coeff}	Long term stability	1000 hours, T = 25°C	-	300	1000(2)	ppm
$V_{DDCoeff}$	Average voltage coefficient	3.0 V < V_{DD} < 3.6 V	-	250	1200(2)	ppm/V
V_{REFINT_DIV1}	1/4 reference voltage	-	24	25	26	% V_{REFINT}
V_{REFINT_DIV2}	1/2 reference voltage		49	50	51	
V_{REFINT_DIV3}	3/4 reference voltage		74	75	76	

1. The shortest sampling time can be determined in the application by multiple iterations.
2. Guaranteed by design.

Table 27. Current consumption in Run and Low-power run modes, code with data processing running from Flash, ART disable

Symbol	Parameter	Conditions			TYP					MAX(1)					Unit
		-	Voltage scaling	f_{HCLK}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD}(Run)	Supply current in Run mode	$f_{HCLK} = f_{HSE}$ up to 48MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	Range 2	26 MHz	3.15	3.19	3.31	3.50	3.85	3.47	3.70	3.84	4.26	4.88	mA
				16 MHz	2.24	2.28	2.39	2.57	2.90	2.46	2.60	2.74	3.16	3.78	
				8 MHz	1.26	1.29	1.40	1.57	1.89	1.40	1.50	1.64	2.06	2.68	
				4 MHz	0.71	0.75	0.85	1.02	1.34	0.79	0.88	1.06	1.38	2.21	
				2 MHz	0.42	0.45	0.55	0.72	1.04	0.46	0.55	0.73	1.09	1.88	
				1 MHz	0.27	0.30	0.40	0.57	0.89	0.30	0.38	0.57	0.90	1.61	
				100 kHz	0.14	0.17	0.27	0.43	0.75	0.17	0.22	0.40	0.74	1.44	
			Range 1	80 MHz	10.0	10.1	10.3	10.6	11.0	11.00	11.35	11.64	12.26	13.10	
				72 MHz	9.06	9.13	9.28	9.51	9.92	9.97	10.36	10.65	11.06	11.69	
				64 MHz	8.96	9.04	9.22	9.48	9.92	9.86	10.25	10.54	10.95	11.79	
				48 MHz	7.64	7.72	7.91	8.17	8.62	8.40	8.76	8.90	9.52	10.36	
				32 MHz	5.49	5.57	5.74	5.98	6.40	6.04	6.40	6.69	7.10	7.94	
				24 MHz	4.16	4.22	4.36	4.57	4.96	4.60	4.86	5.15	5.56	6.19	
				16 MHz	2.93	2.99	3.13	3.35	3.75	3.22	3.43	3.72	4.13	4.97	
I_{DD}(LPRun)	Supply current in Low-power run	$f_{HCLK} = f_{MSI}$ all peripherals disable		2 MHz	358	392	503	683	1050	435	501	694	1069	1819	µA
				1 MHz	197	230	340	519	880	245	312	512	887	1637	
				400 kHz	97	126	235	414	778	130	202	402	777	1527	
				100 kHz	47	77	186	365	726	85	147	347	711	1472	

1. Guaranteed by characterization results, unless otherwise specified.

Table 28. Current consumption in Run and Low-power run modes, code with data processing running from SRAM1

Symbol	Parameter	Conditions			TYP					MAX(1)					Unit
		-	Voltage scaling	f_{HCLK}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD}(Run)	Supply current in Run mode	$f_{HCLK} = f_{HSE}$ up to 48MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	Range 2	26 MHz	2.88	2.94	3.05	3.23	3.58	3.18	3.26	3.40	4.02	4.65	mA
				16 MHz	1.83	1.87	1.98	2.15	2.50	2.01	2.16	2.30	2.72	3.34	
				8 MHz	0.97	1.00	1.11	1.27	1.62	1.07	1.16	1.32	1.73	2.36	
				4 MHz	0.54	0.57	0.67	0.84	1.18	0.59	0.69	0.88	1.23	1.96	
				2 MHz	0.33	0.36	0.46	0.62	0.96	0.37	0.45	0.63	0.98	1.70	
				1 MHz	0.22	0.25	0.35	0.51	0.85	0.25	0.33	0.50	0.86	1.57	
				100 kHz	0.12	0.15	0.25	0.41	0.75	0.15	0.21	0.39	0.74	1.45	
			Range 1	80 MHz	10.2	10.3	10.5	10.7	11.1	11.22	11.57	11.86	12.07	13.11	
				72 MHz	9.25	9.31	9.46	9.68	10.1	10.18	10.41	10.55	10.76	11.80	
				64 MHz	8.25	8.31	8.46	8.67	9.08	9.08	9.37	9.66	9.87	10.91	
				48 MHz	6.26	6.33	6.48	6.69	7.11	6.89	7.11	7.25	7.67	8.50	
				32 MHz	4.22	4.28	4.42	4.63	5.03	4.64	4.86	5.15	5.56	6.19	
				24 MHz	3.20	3.25	3.38	3.59	3.99	3.52	3.70	3.84	4.26	5.09	
				16 MHz	2.18	2.22	2.35	2.55	2.94	2.40	2.55	2.84	3.25	4.09	
I_{DD}(LPRun)	Supply current in low-power run mode	$f_{HCLK} = f_{MSI}$ all peripherals disable FLASH in power-down		2 MHz	242	275	384	562	924	300	380	573	927	1677	µA
				1 MHz	130	162	269	445	809	180	243	435	810	1560	
				400 kHz	61	90	197	374	734	95	160	353	728	1478	
				100 kHz	26	56	163	339	702	55	122	314	679	1429	

1. Guaranteed by characterization results, unless otherwise specified.

Table 35. Current consumption in Stop 1 mode (continued)

Symbol	Parameter	Conditions			TYP					MAX(1)					Unit
		-	-	V_{DD}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD} (wakeup from Stop1)	Supply current during wakeup from Stop 1	Wakeup clock MSI = 48 MHz, voltage Range 1. See (4).		3 V	1.47	-	-	-	-	-					mA
		Wakeup clock MSI = 4 MHz, voltage Range 2. See (4).		3 V	1.7	-	-	-	-						
		Wakeup clock HSI16 = 16 MHz, voltage Range 1. See (4).		3 V	1.62	-	-	-	-						

1. Guaranteed by characterization results, unless otherwise specified.
2. LCD enabled with external voltage source. Consumption from VLCD excluded. Refer to LCD controller characteristics for I_{VLCD}.
3. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.
4. Wakeup with code execution from Flash. Average value given for a typical wakeup time as specified in *Table 41: Low-power mode wakeup timings*.

1. The BusMatrix is automatically active when at least one master is ON (CPU, DMA).
2. The GPIOx (x= A…H) dynamic current consumption is approximately divided by a factor two versus this table values when the GPIO port is locked thanks to LCKK and LCKy bits in the GPIOx_LCKR register. In order to save the full GPIOx current consumption, the GPIOx clock should be disabled in the RCC when all port I/Os are used in alternate function or analog mode (clock is only required to read or write into GPIO registers, and is not used in AF or analog modes).
3. The AHB to APB1 Bridge is automatically active when at least one peripheral is ON on the APB1.
4. The AHB to APB2 Bridge is automatically active when at least one peripheral is ON on the APB2.

6.3.6 Wakeup time from low-power modes and voltage scaling transition times

The wakeup times given in *Table 41* are the latency between the event and the execution of the first user instruction.

The device goes in low-power mode after the WFE (Wait For Event) instruction.

Table 41. Low-power mode wakeup timings(1)

Symbol	Parameter	Conditions		Typ	Max	Unit
$t_{WUSLEEP}$	Wakeup time from Sleep mode to Run mode	-		6	6	Nb of CPU cycles
$t_{WULPSLEEP}$	Wakeup time from Low-power sleep mode to Low-power run mode	Wakeup in Flash with Flash in power-down during low-power sleep mode (SLEEP_PD=1 in FLASH_ACR) and with clock MSI = 2 MHz		6	9.3	
$t_{WUSTOP0}$	Wake up time from Stop 0 mode to Run mode in Flash	Range 1	Wakeup clock MSI = 48 MHz	5.6	10.9	µs
			Wakeup clock HSI16 = 16 MHz	4.7	10.4	
		Range 2	Wakeup clock MSI = 24 MHz	5.7	11.1	
			Wakeup clock HSI16 = 16 MHz	4.5	10.5	
			Wakeup clock MSI = 4 MHz	6.6	14.2	
	Wake up time from Stop 0 mode to Run mode in SRAM1	Range 1	Wakeup clock MSI = 48 MHz	0.7	2.05	
			Wakeup clock HSI16 = 16 MHz	1.7	2.8	
		Range 2	Wakeup clock MSI = 24 MHz	0.8	2.72	
			Wakeup clock HSI16 = 16 MHz	1.7	2.8	
			Wakeup clock MSI = 4 MHz	2.4	11.32	

Table 49. MSI oscillator characteristics(1) (continued)

Symbol	Parameter	Conditions			Min	Typ	Max	Unit
$I_{DD}(MSI)$(6)	MSI oscillator power consumption	MSI and PLL mode	Range 0	-	-	0.6	1	µA
			Range 1	-	-	0.8	1.2	
			Range 2	-	-	1.2	1.7	
			Range 3	-	-	1.9	2.5	
			Range 4	-	-	4.7	6	
			Range 5	-	-	6.5	9	
			Range 6	-	-	11	15	
			Range 7	-	-	18.5	25	
			Range 8	-	-	62	80	
			Range 9	-	-	85	110	
			Range 10	-	-	110	130	
			Range 11	-	-	155	190	

1. Guaranteed by characterization results.
2. This is a deviation for an individual part once the initial frequency has been measured.
3. Sampling mode means Low-power run/Low-power sleep modes with Temperature sensor disable.
4. Average period of MSI @48 MHz is compared to a real 48 MHz clock over 28 cycles. It includes frequency tolerance + jitter of MSI @48 MHz clock.
5. Only accumulated jitter of MSI @48 MHz is extracted over 28 cycles.
   For next transition: min. and max. jitter of 2 consecutive frame of 28 cycles of the MSI @48 MHz, for 1000 captures over 28 cycles.
   For paired transitions: min. and max. jitter of 2 consecutive frame of 56 cycles of the MSI @48 MHz, for 1000 captures over 56 cycles.
6. Guaranteed by design.

Table 51. PLL, PLLSAI1, PLLSAI2 characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock(2)	-	4	-	16	MHz
	PLL input clock duty cycle	-	45	-	55	%
$f_{PLL_P_OUT}$	PLL multiplier output clock P	Voltage scaling Range 1	2.0645	-	80	MHz
		Voltage scaling Range 2	2.0645	-	26	
$f_{PLL_Q_OUT}$	PLL multiplier output clock Q	Voltage scaling Range 1	8	-	80	MHz
		Voltage scaling Range 2	8	-	26	
$f_{PLL_R_OUT}$	PLL multiplier output clock R	Voltage scaling Range 1	8	-	80	MHz
		Voltage scaling Range 2	8	-	26	
f_{VCO_OUT}	PLL VCO output	Voltage scaling Range 1	64	-	344	MHz
		Voltage scaling Range 2	64	-	128	
t_{LOCK}	PLL lock time	-	-	15	40	µs
Jitter	RMS cycle-to-cycle jitter	System clock 80 MHz	-	40	-	±ps
	RMS period jitter		-	30	-	
I_{DD}(PLL)	PLL power consumption on V_{DD}(1)	VCO freq = 64 MHz	-	150	200	µA
		VCO freq = 96 MHz	-	200	260	
		VCO freq = 192 MHz	-	300	380	
		VCO freq = 344 MHz	-	520	650	

1. Guaranteed by design.
2. Take care of using the appropriate division factor M to obtain the specified PLL input clock values. The M factor is shared between the 3 PLLs.

6.3.10 Flash memory characteristics

Table 52. Flash memory characteristics(1)

Symbol	Parameter	Conditions	Typ	Max	Unit
t_{prog}	64-bit programming time	-	81.69	90.76	µs
t_{prog_row}	one row (32 double word) programming time	normal programming	2.61	2.90	ms
		fast programming	1.91	2.12	
t_{prog_page}	one page (2 Kbyte) programming time	normal programming	20.91	23.24	
		fast programming	15.29	16.98	
t_{ERASE}	Page (2 KB) erase time	-	22.02	24.47	
t_{prog_bank}	one bank (512 Kbyte) programming time	normal programming	5.35	5.95	s
		fast programming	3.91	4.35	
t_{ME}	Mass erase time (one or two banks)	-	22.13	24.59	ms

Figure 38. Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms

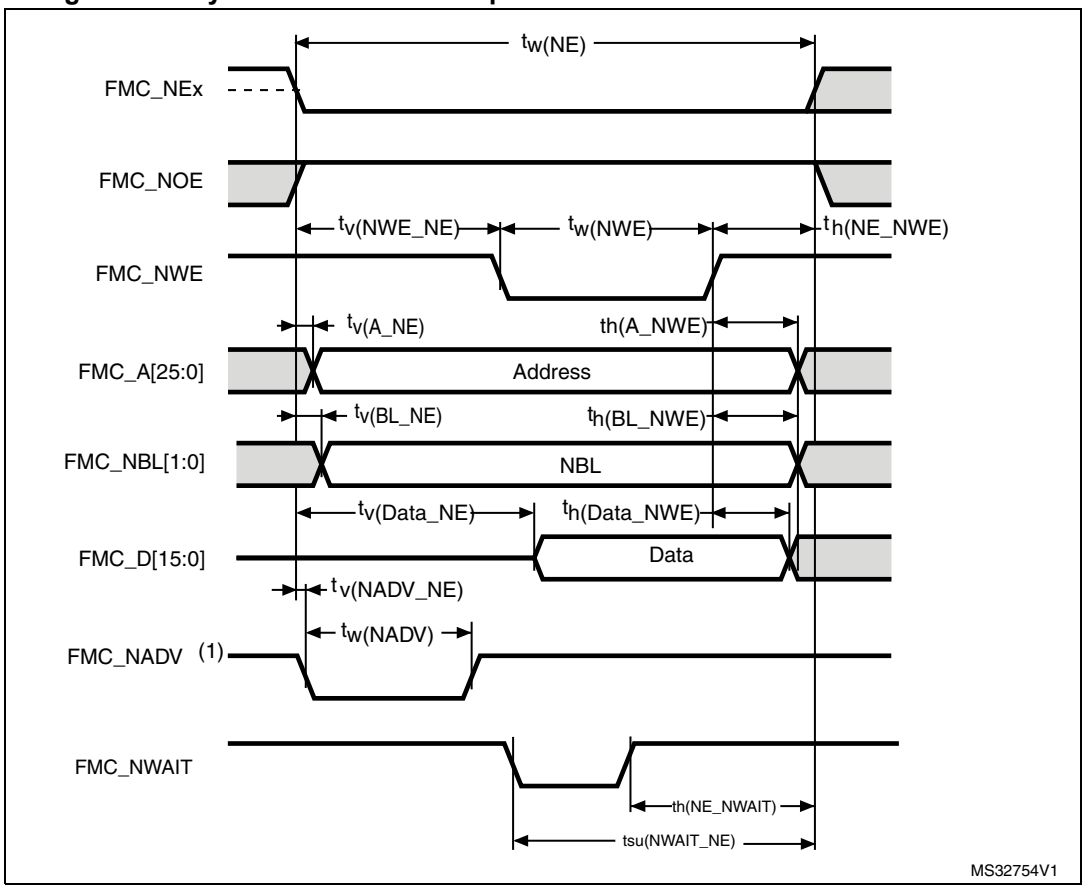
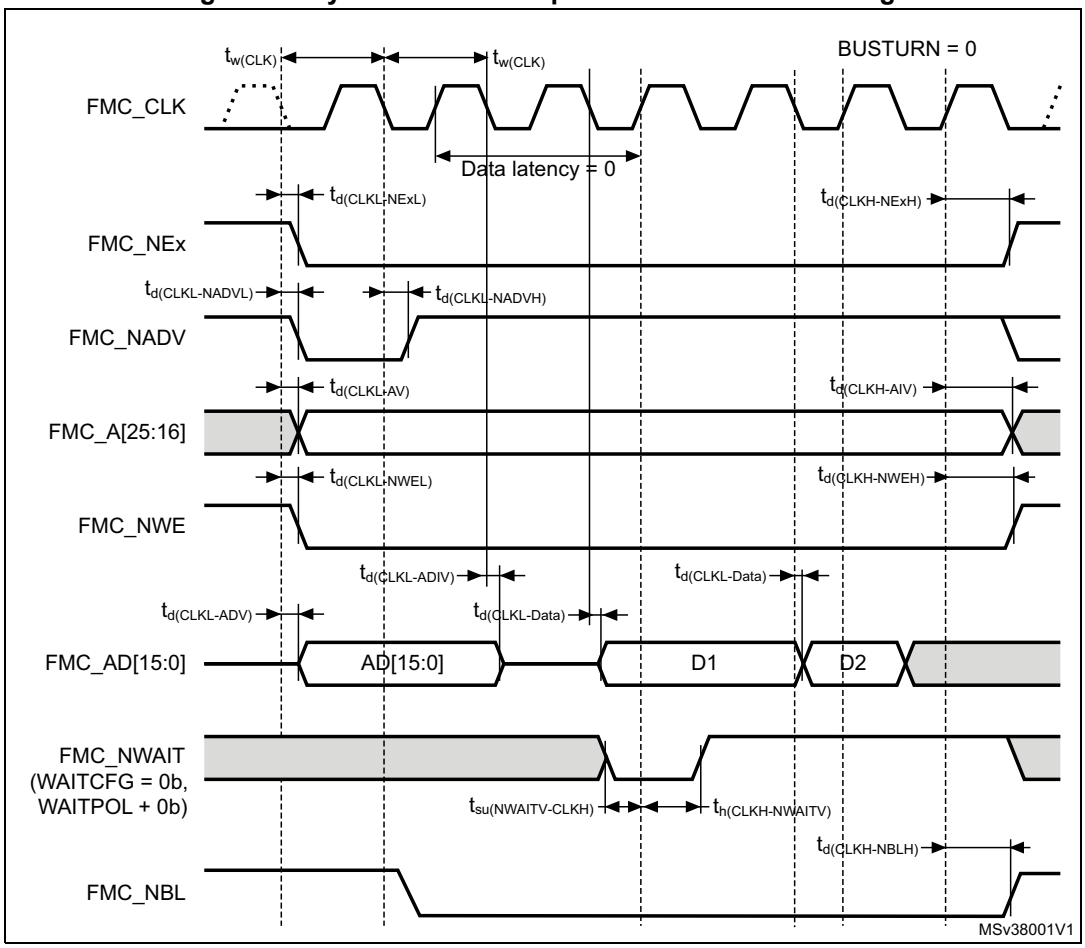


Table 93. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$3T_{HCLK}$-1	$3T_{HCLK}$+2	ns
$t_{v(NWE_NE)}$	FMC_NEx low to FMC_NWE low	T_{HCLK}-0.5	T_{HCLK}+1.5	
$t_{w(NWE)}$	FMC_NWE low time	T_{HCLK}-1	T_{HCLK}+1	
$t_{h(NE_NWE)}$	FMC_NWE high to FMC_NE high hold time	T_{HCLK}-0.5	-	
$t_{v(A_NE)}$	FMC_NEx low to FMC_A valid	-	0	
$t_{h(A_NWE)}$	Address hold time after FMC_NWE high	T_{HCLK}-1	-	
$t_{v(BL_NE)}$	FMC_NEx low to FMC_BL valid	-	1.5	
$t_{h(BL_NWE)}$	FMC_BL hold time after FMC_NWE high	T_{HCLK}-0.5	-	
$t_{v(Data_NE)}$	Data to FMC_NEx low to Data valid	-	T_{HCLK}+4	
$t_{h(Data_NWE)}$	Data hold time after FMC_NWE high	T_{HCLK}+1	-	
$t_{v(NADV_NE)}$	FMC_NEx low to FMC_NADV low	-	1	
$t_{w(NADV)}$	FMC_NADV low time	-	T_{HCLK}+0.5	

1. CL = 30 pF.
2. Guaranteed by characterization results.

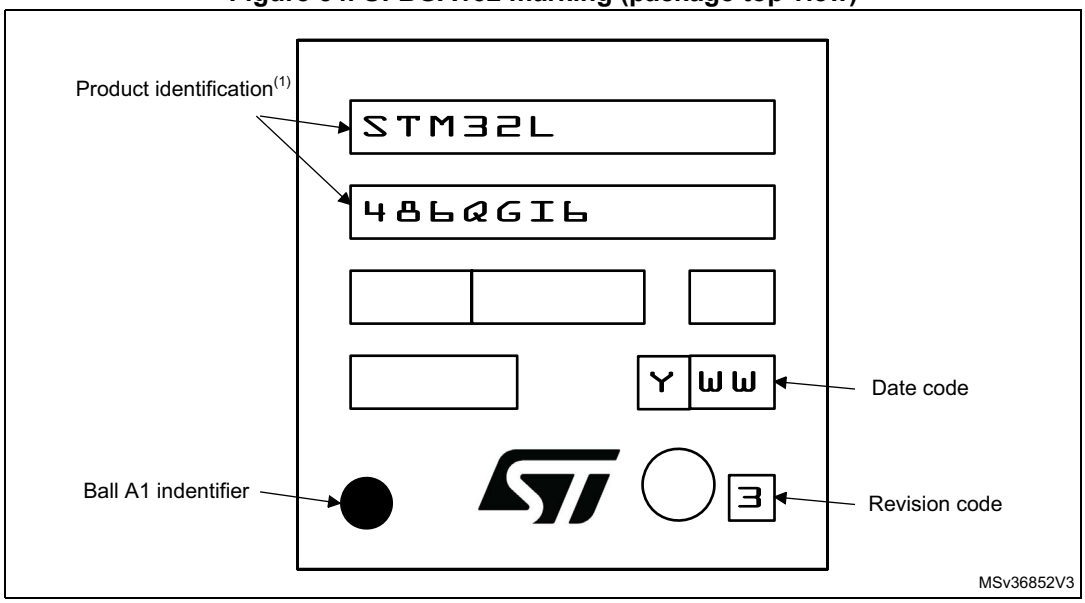
Figure 42. Synchronous multiplexed PSRAM write timings



Device marking

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

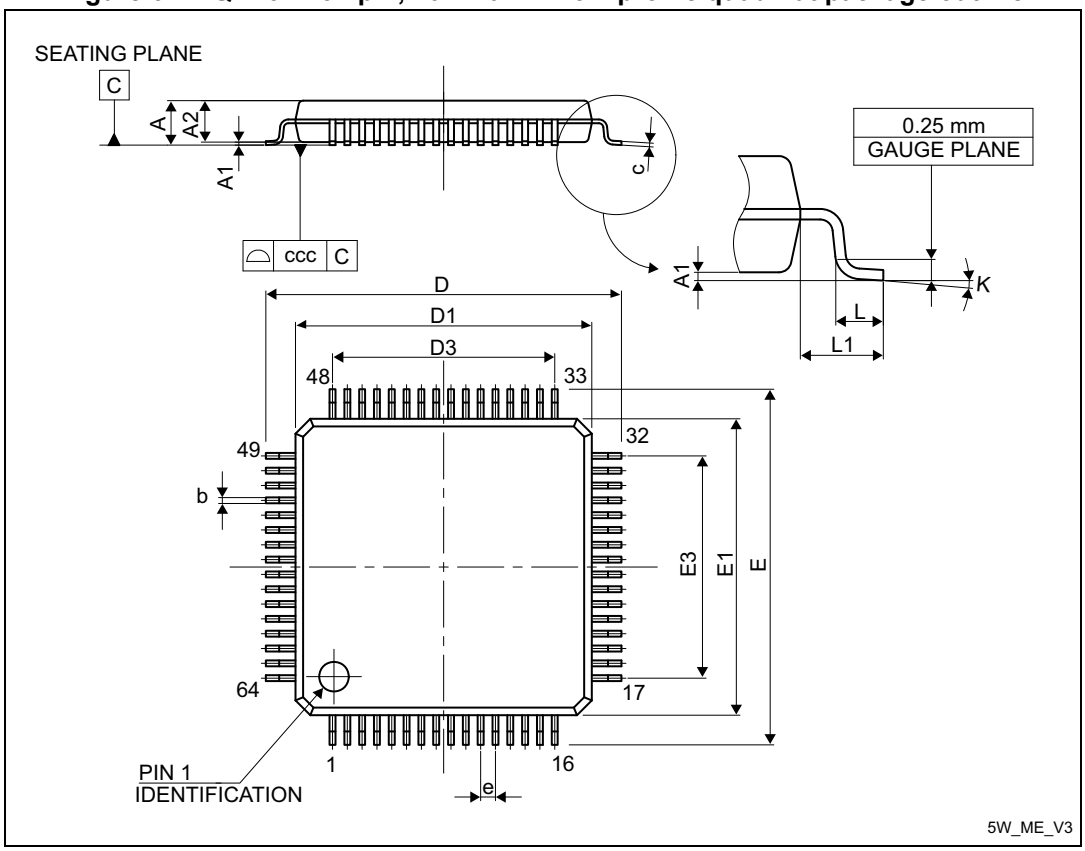
Figure 54. UFBGA132 marking (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

7.5 LQFP64 package information

Figure 61. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package outline



1. Drawing is not to scale.

Table 112. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data

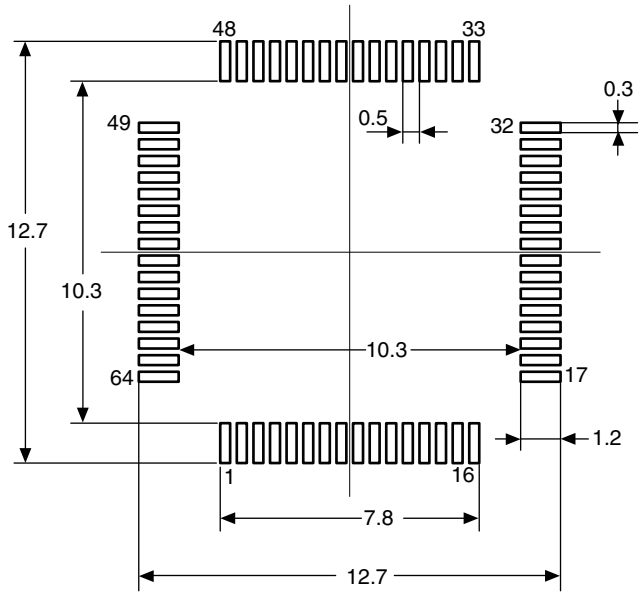
Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	-	12.000	-	-	0.4724	-
D1	-	10.000	-	-	0.3937	-
D3	-	7.500	-	-	0.2953	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-

Table 112. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
E3	-	7.500	-	-	0.2953	-
e	-	0.500	-	-	0.0197	-
K	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 62. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

7.6 Thermal characteristics

The maximum chip junction temperature ($T_J$max) must never exceed the values given in *Table 22: General operating conditions*.

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = \Sigma (V_{OL} \times I_{OL}) + \Sigma ((V_{DDIOx} - V_{OH}) \times I_{OH}),$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 113. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal resistance junction-ambient** LQFP64 - 10 × 10 mm / 0.5 mm pitch	45	°C/W
	Thermal resistance junction-ambient LQFP100 - 14 × 14mm	42	
	Thermal resistance junction-ambient LQFP144 - 20 × 20 mm	32	
	Thermal resistance junction-ambient UFBGA132 - 7 × 7 mm	55	
	Thermal resistance junction-ambient WLCSP72	46	

7.6.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org

7.6.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in *Section 8: Part numbering*.

Each temperature range suffix corresponds to a specific guaranteed ambient temperature at maximum dissipation and, to a specific maximum junction temperature.