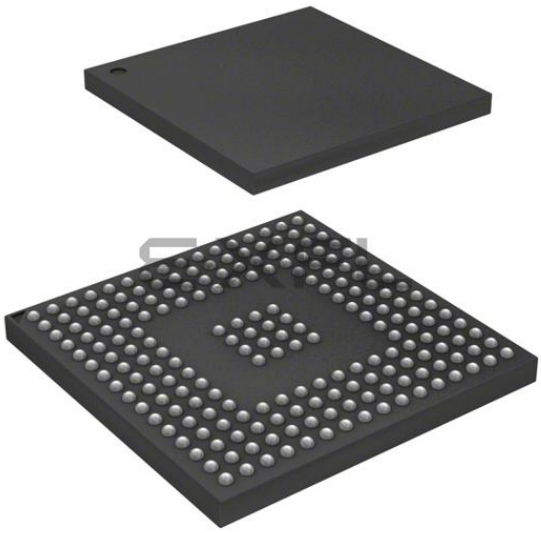

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	ST10
Core Size	16-Bit
Speed	40MHz
Connectivity	ASC, CANbus, EBI/EMI, SSC
Peripherals	POR, PWM, WDT
Number of I/O	143
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	18K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 32x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	208-BGA
Supplier Device Package	208-PBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/st10f280-q3tr

1 Description

The ST10F280 is a new derivative of the STMicroelectronics® ST10 family of 16-bit single-chip CMOS microcontrollers. It combines high CPU performance (up to 20 million instructions per second) with high peripheral functionality and enhanced I/O-capabilities. It also provides on-chip high-speed single voltage FLASH memory, on-chip high-speed RAM, and clock generation via PLL.

ST10F280 is processed in 0.35µm CMOS technology. The MCU core and the logic is supplied with a 5V to 3.3V on chip voltage regulator. The part is supplied with a single 5V supply and I/Os work at 5V.

The device is upward compatible with the ST10F269 device, with the following set of differences:

- Two supply pins (DC1,DC2) on the PBGA-208 package are used for decoupling the internally generated 3.3V core logic supply. Do not connect these two pins to 5.0V external supply. Instead, these pins should be connected to a decoupling capacitor (ceramic type, value ≥ 330nF).
- The A/D Converter characteristics stay identical but 16 new input channel are added. A bit in a new register (XADCMUX) control the multiplexage between the first block of 16 channel (on Port5) and the second block (on XPort10). The conversion result registers stay identical and the software management can determine the block in use. A new dedicated timer controls now the ADC channel injection mode on the input CC31 (P7.7). The output of this timer is visible on a dedicated pin (XADCINJ) to emulate this new functionality.
- A second XPWM peripheral (4 new channels) is added. Four dedicated pins are reserved for the outputs (XPWM[0:3])
- A new general purpose I/O port named XPORT9 (16 bits) is added. Due to the bit addressing management, it will be different from other standard general purpose I/O ports.

Table 1. Ball description (continued)

Symbol	Ball number	Type	Function
P2.0 – P2.15		I/O	Port 2 is a 16-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 2 outputs can be configured as push/pull or open drain drivers. The input threshold of Port 2 is selectable (TTL or special). The following Port 2 pins also serve for alternate functions:
	T7	I/O	P2.0 CC0IO CAPCOM: CC0 Capture Input / Compare Output
	P8	I/O	P2.1 CC1IO CAPCOM: CC1 Capture Input / Compare Output
	R8	I/O	P2.2 CC2IO CAPCOM: CC2 Capture Input / Compare Output
	T8	I/O	P2.3 CC3IO CAPCOM: CC3 Capture Input / Compare Output
	T9	I/O	P2.4 CC4IO CAPCOM: CC4 Capture Input / Compare Output
	P9	I/O	P2.5 CC5IO CAPCOM: CC5 Capture Input / Compare Output
	R9	I/O	P2.6 CC6IO CAPCOM: CC6 Capture Input / Compare Output
	U9	I/O	P2.7 CC7IO CAPCOM: CC7 Capture Input / Compare Output
	T10	I/O I	P2.8 CC8IO CAPCOM: CC8 Capture Input / Compare Output, EX0IN Fast External Interrupt 0 Input
	R10	I/O I	P2.9 CC9IO CAPCOM: CC9 Capture Input / Compare Output, EX1IN Fast External Interrupt 1 Input
	P10	I/O I	P2.10 CC10IO CAPCOM: CC10 Capture Input / Compare Output, EX2IN Fast External Interrupt 2 Input
	T11	I/O I	P2.11 CC11IO CAPCOM: CC11 Capture Input / Compare Output, EX3IN Fast External Interrupt 3 Input
	R11	I/O I	P2.12 CC12IO CAPCOM: CC12 Capture Input / Compare Output, EX4IN Fast External Interrupt 4 Input
	U12	I/O I	P2.13 CC13IO CAPCOM: CC13 Capture Input / Compare Output, EX5IN Fast External Interrupt 5 Input
	P11	I/O I	P2.14 CC14IO CAPCOM: CC14 Capture Input / Compare Output, EX6IN Fast External Interrupt 6 Input
	T12	I/O I I	P2.15 CC15IO CAPCOM: CC15 Capture Input / Compare Output, EX7IN Fast External Interrupt 7 Input T7IN CAPCOM2 Timer T7 Count Input

Table 2. 512 Kbyte Flash memory block organization

Block	Addresses (segment 0)	Addresses (segment 1)	Size (Kbyte)
0	00'0000h to 00'3FFFh	01'0000h to 01'3FFFh	16
1	00'4000h to 00'5FFFh	01'4000h to 01'5FFFh	8
2	00'6000h to 00'7FFFh	01'6000h to 01'7FFFh	8
3	01'8000h to 01'FFFFh	01'8000h to 01'FFFFh	32
4	02'0000h to 02'FFFFh	02'0000h to 02'FFFFh	64
5	03'0000h to 03'FFFFh	03'0000h to 03'FFFFh	64
6	04'0000h to 04'FFFFh	04'0000h to 04'FFFFh	64
7	05'0000h to 05'FFFFh	05'0000h to 05'FFFFh	64
8	06'0000h to 06'FFFFh	06'0000h to 06'FFFFh	64
9	07'0000h to 07'FFFFh	07'0000h to 07'FFFFh	64
10	08'0000h to 08'FFFFh	08'0000h to 08'FFFFh	64

5.2.2 Instructions and commands

All operations besides normal read operations are initiated and controlled by command sequences written to the Flash Command Interface (CI). The Command Interface (CI) interprets words written to the Flash memory and enables one of the following operations:

- Read memory array
- Program word
- Block erase
- Chip erase
- Erase suspend
- Erase resume
- Block protection
- Block temporary unprotection
- Code protection

Commands are composed of several write cycles at specific addresses of the Flash memory. The different write cycles of such command sequences offer a fail-safe feature to protect against an inadvertent write.

A command only starts when the Command Interface has decoded the last write cycle of an operation. Until that last write is performed, Flash memory remains in Read Mode

Note: As it is not possible to perform write operations in the Flash while fetching code from Flash, the Flash commands must be written by instructions executed from internal RAM or external memory.

Command write cycles do not need to be consecutively received, pauses are allowed, save for Block Erase command. During this operation all Erase Confirm commands must be sent to complete any block erase operation before time-out period expires (typically 96µs). Command sequencing must be followed exactly. Any invalid combination of commands will reset the Command Interface to Read Mode.

5.2.8 Power supply, reset

The Flash module uses a single power supply for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations from 5V supply. Once a program or erase cycle has been completed, the device resets to the standard read mode. At power-on, the Flash memory has a setup phase of some microseconds (dependent on the power supply ramp-up). During this phase, Flash can not be read. Thus, if $\overline{EA}$ pin is high (execution will start from Flash memory), the CPU remains in reset state until the Flash can be accessed.

5.3 Architectural description

The Flash module distinguishes two basic operating modes, the standard read mode and the command mode. The initial state after power-on and after reset is the standard read mode.

5.3.1 Read mode

The Flash module enters the standard operating mode, the read mode:

- After reset command
- After every completed erase operation
- After every completed programming operation
- After every other completed command execution
- Few microseconds after a CPU-reset has started
- After incorrect address and data values of command sequences or writing them in an improper sequence
- After incorrect write access to a read protected Flash memory

The read mode remains active until the last command of a command sequence is decoded which starts directly a Flash array operation, such as:

- Erase one or several blocks
- Program a word into Flash array
- Protect / temporary unprotect a block.

In the standard read mode read accesses are directly controlled by the Flash memory array, delivering a 32-bit double Word from the addressed position. Read accesses are always aligned to double Word boundaries. Thus, both low order address bit A1 and A0 are not used in the Flash array for read accesses. The high order address bit A18/A17/A16 define the physical 64K Bytes segment being accessed within the Flash array.

5.3.2 Command mode

Every operation besides standard read operations is initiated by commands written to the Flash command register. The addresses used for command cycles define in conjunction with the actual state the specific step within command sequences. With the last command of a command sequence, the Erase-Program Controller (EPC) starts the execution of the command. The EPC status is indicated during command execution by:

- Status Register
- Ready/Busy signal

The system configuration register SYSCON

This bit-addressable register provides general system configuration and control functions. The reset value for register SYSCON depends on the state of the PORT0 pins during reset.

SYSCON

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STKSZ			ROMS1	SGTDIS	ROMEN	BYTDIS	CLKEN	WRCFG	CSCFG	PWDCFG	OWDDIS	BDRSTEN	XPEN	VISIBLE	XPER-SHARE
R/W			R/W	R/W	R/W(1)	R/W(1)	R/W	R/W(1)	R/W	R/W	R/W	R/W	R/W	R/W	R/W

1. These bit are set directly or indirectly according to PORT0 and EA pin configuration during reset sequence. Register SYSCON cannot be changed after execution of the EINIT instruction.

Address: 0xFF12h / 89h SFR

Reset: 0x0XX0h

Type: R/W

XPEN XBUS Peripheral Enable Bit

0: Accesses to the on-chip X-Peripherals and their functions are disabled

1: The on-chip X-Peripherals are enabled and can be accessed.

BDRSTEN Bidirectional Reset Enable

0: $\overline{\text{RSTIN}}$ pin is an input pin only. SW Reset or WDT Reset have no effect on this pin

1: $\overline{\text{RSTIN}}$ pin is a bidirectional pin. This pin is pulled low during 1024 TCL during reset sequence.

OWDDIS Oscillator Watchdog Disable Control

0: Oscillator Watchdog (OWD) is enabled. If PLL is bypassed, the OWD monitors XTAL1 activity. If there is no activity on XTAL1 for at least 1 µs, the CPU clock is switched automatically to PLL's base frequency (2 to 10MHz).

1: OWD is disabled. If the PLL is bypassed, the CPU clock is always driven by XTAL1 signal. The PLL is turned off to reduce power supply current.

PWDCFG Power Down Mode Configuration Control

0: Power Down Mode can only be entered during PWRDN instruction execution if $\overline{\text{NMI}}$ pin is low, otherwise the instruction has no effect. To exit Power Down Mode, an external reset must occurs by asserting the $\overline{\text{RSTIN}}$ pin.

1: Power Down Mode can only be entered during PWRDN instruction execution if all enabled fast external interrupt EXxIN pins are in their inactive level. Exiting this mode can be done by asserting one enabled EXxIN pin.

CSCFG Chip Select Configuration Control

0: Latched Chip Select lines: CSx change 1 TCL after rising edge of ALE

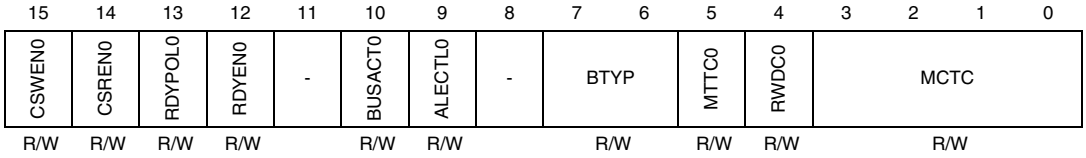
1: Unlatched Chip Slect lines: CSx change with rising edge of ALE

Table 5. MAC coprocessor specific instructions (continued)

Mnemonic	Addressing modes	Repeatability
CoNEG	-	No
CoNEG, rnd		
CoRND		
CoSTORE	Rw_n, CoReg	No
	[Rw_n⊗], Coreg	Yes
CoMOV	[IDX_i⊗], [Rw_m⊗]	Yes
CoMACM	[IDX_i⊗], [Rw_m⊗]	Yes
CoMACMu		
CoMACMus		
CoMACMsu		
CoMACM-		
CoMACMu-		
CoMACMus-		
CoMACMsu-		
CoMACM, rnd		
CoMACMu, rnd		
CoMACMus, rnd		
CoMACMsu, rnd		
CoMACMR		
CoMACMRu		
CoMACMRus		
CoMACMRsu		
CoMACMR, rnd		
CoMACMRu, rnd		
CoMACMRus, rnd		
CoMACMRsu, rnd		
CoADD	Rw_n, Rw_m [IDX_i⊗], [Rw_m⊗] Rw_n, [Rw_m⊗]	No Yes Yes
CoADD2		
CoSUB		
CoSUB2		
CoSUBR		
CoSUB2R		
CoMAX		
CoMIN		

each bus cycle within this window must be terminated with the active level defined by this RDYPOL bit in the associated BUSCON register.

BUSCON0

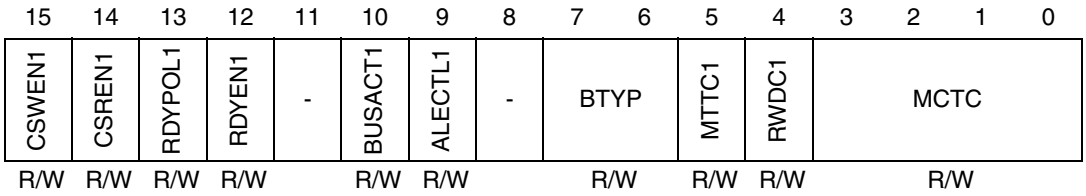


Address: 0xFF0Ch / 86h SFR

Reset: 0x0XX0h

Type: R/W

BUSCON1

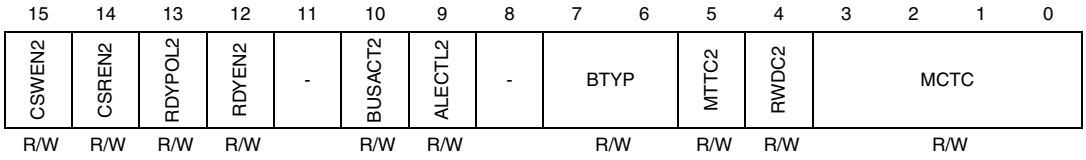


Address: 0xFF14h / 8Ah SFR

Reset: 0x0000h

Type: R/W

BUSCON2



Address: 0xFF16h / 8Bh SFR

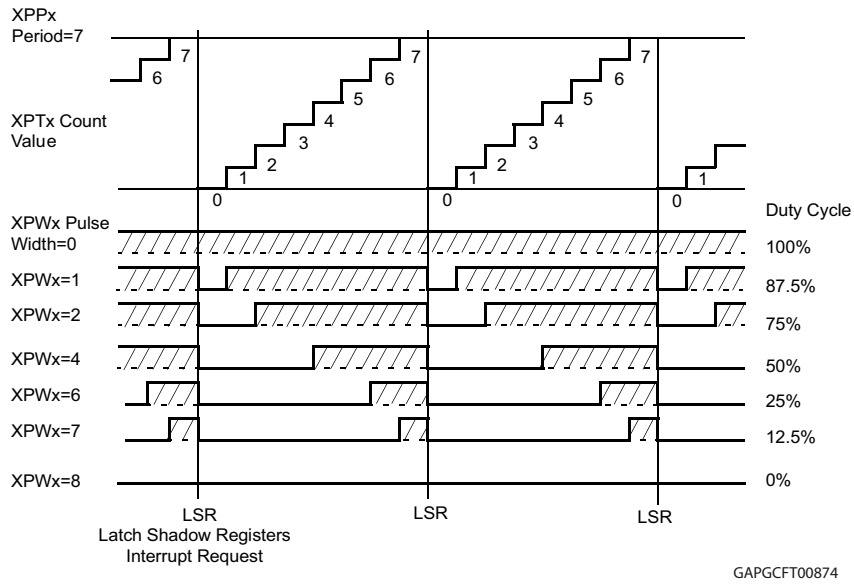
Reset: 0x0000h

Type: R/W

Table 8. Interrupt sources (continued)

Source of Interrupt or PEC service request	Request flag	Enable flag	Interrupt vector	Vector location	Trap number
CAPCOM Register 13	CC13IR	CC13IE	CC13INT	00'0074h	1Dh
CAPCOM Register 14	CC14IR	CC14IE	CC14INT	00'0078h	1Eh
CAPCOM Register 15	CC15IR	CC15IE	CC15INT	00'007Ch	1Fh
CAPCOM Register 16	CC16IR	CC16IE	CC16INT	00'00C0h	30h
CAPCOM Register 17	CC17IR	CC17IE	CC17INT	00'00C4h	31h
CAPCOM Register 18	CC18IR	CC18IE	CC18INT	00'00C8h	32h
CAPCOM Register 19	CC19IR	CC19IE	CC19INT	00'00CCh	33h
CAPCOM Register 20	CC20IR	CC20IE	CC20INT	00'00D0h	34h
CAPCOM Register 21	CC21IR	CC21IE	CC21INT	00'00D4h	35h
CAPCOM Register 22	CC22IR	CC22IE	CC22INT	00'00D8h	36h
CAPCOM Register 23	CC23IR	CC23IE	CC23INT	00'00DCh	37h
CAPCOM Register 24	CC24IR	CC24IE	CC24INT	00'00E0h	38h
CAPCOM Register 25	CC25IR	CC25IE	CC25INT	00'00E4h	39h
CAPCOM Register 26	CC26IR	CC26IE	CC26INT	00'00E8h	3Ah
CAPCOM Register 27	CC27IR	CC27IE	CC27INT	00'00ECh	3Bh
CAPCOM Register 28	CC28IR	CC28IE	CC28INT	00'00F0h	3Ch
CAPCOM Register 29	CC29IR	CC29IE	CC29INT	00'0110h	44h
CAPCOM Register 30	CC30IR	CC30IE	CC30INT	00'0114h	45h
CAPCOM Register 31	CC31IR	CC31IE	CC31INT	00'0118h	46h
CAPCOM Timer 0	T0IR	T0IE	T0INT	00'0080h	20h
CAPCOM Timer 1	T1IR	T1IE	T1INT	00'0084h	21h
CAPCOM Timer 7	T7IR	T7IE	T7INT	00'00F4h	3Dh
CAPCOM Timer 8	T8IR	T8IE	T8INT	00'00F8h	3Eh
GPT1 Timer 2	T2IR	T2IE	T2INT	00'0088h	22h
GPT1 Timer 3	T3IR	T3IE	T3INT	00'008Ch	23h
GPT1 Timer 4	T4IR	T4IE	T4INT	00'0090h	24h
GPT2 Timer 5	T5IR	T5IE	T5INT	00'0094h	25h
GPT2 Timer 6	T6IR	T6IE	T6INT	00'0098h	26h
GPT2 CAPREL Register	CRIR	CRIE	CRINT	00'009Ch	27h
A/D Conversion Complete	ADCIR	ADCIE	ADCINT	00'00A0h	28h
A/D Overrun Error	ADEIR	ADEIE	ADEINT	00'00A4h	29h
ASC0 Transmit	S0TIR	S0TIE	S0TINT	00'00A8h	2Ah
ASC0 Transmit Buffer	S0TBIR	S0TBIE	S0TBINT	00'011Ch	47h

Figure 20. Operation and output waveform in mode 0



Mode 1: symmetrical PWM generation (center aligned PWM)

Mode 1 is selected by setting the respective bit XPMx in register XPWMCON1 to '1'. In this mode the timer XPTx of the respective XPWM channel is counting up until it reaches the value in the associated period shadow register.

Upon the next count pulse the count direction is reversed and the timer starts counting down now with subsequent count pulses until it reaches the value 0000_H. Upon the next count pulse the count direction is reversed again and the count cycle is repeated with the following count pulses.

The XPWM output signal is switched to a high level when the timer contents are equal to or greater than the contents of the pulse width shadow register while the timer is counting up.

The signal is switched back to a low level when the respective timer has counted down to a value below the contents of the pulse width shadow register. So in mode 1 this PWM value controls both edges of the output signal.

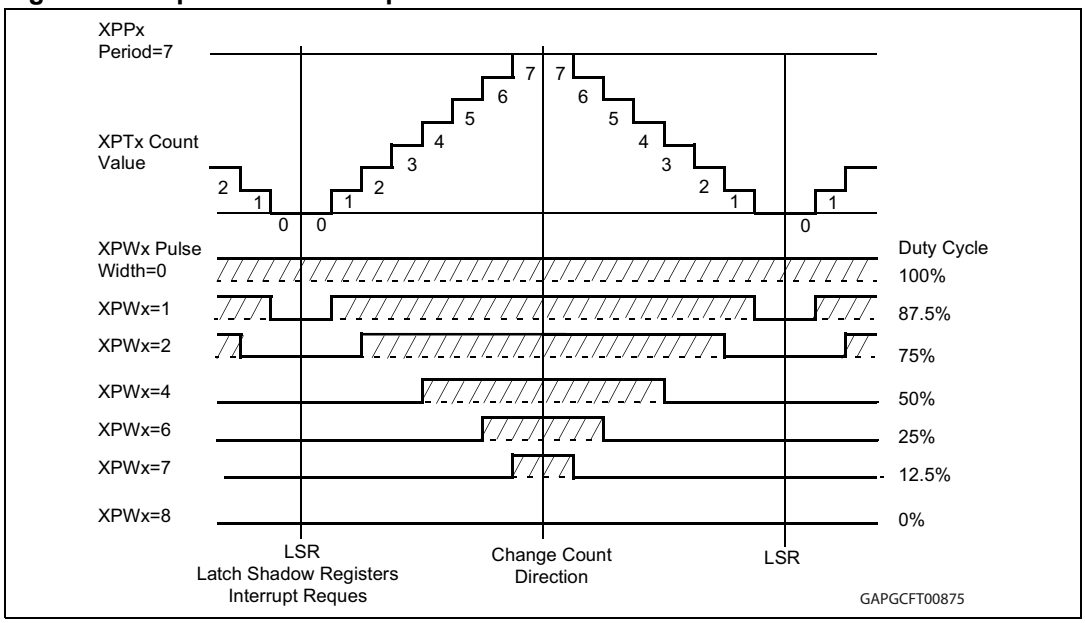
Note that in mode 1 the period of the PWM signal is twice the period of the timer:

$$PWM\_Period_{Mode1} = 2 * ([XPPx] + 1)$$

The figure below illustrates the operation and output waveforms of a XPWM channel in mode 1 for different values in the pulse width register.

This mode is referred to as Center Aligned PWM, because the value in the pulse width (shadow) register effects both edges of the output signal symmetrically.

Figure 21. Operation and output waveform in mode 1

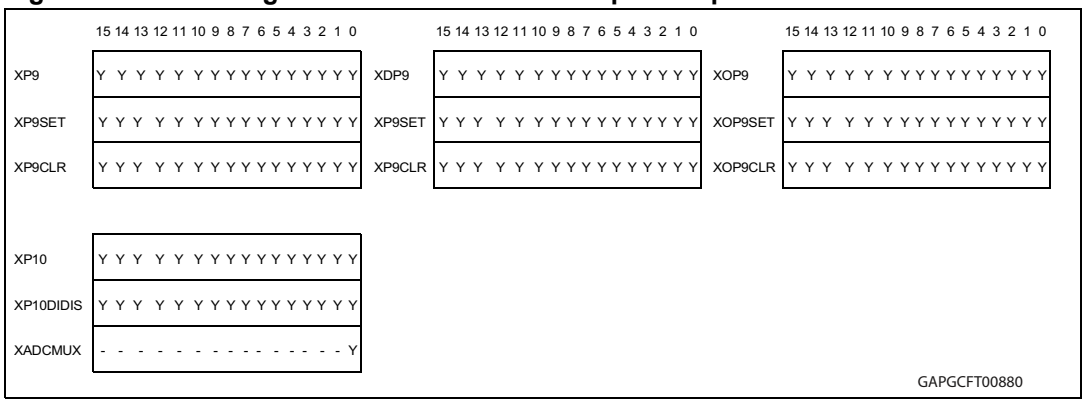


Burst mode

Burst mode is selected by setting bit PB01 in register XPWMCON1 to '1'. This mode combines the signals from XPWM channels 0 and 1 onto the port pin of channel 0. The output of channel 0 is replaced with the logical AND of channels 0 and 1. The output of channel 1 can still be used at its associated output pin (if enabled).
Each of the two channels can either operate in mode 0 or 1.

Note: It is guaranteed by design, that no spurious spikes will occur at the output pin of channel 0 in this mode. The output of the AND gate will be transferred to the output pin synchronously to internal clocks.
XORing of the PWM signal and the port output latch value is done after the ANDing of channel 0 and 1.

Figure 26. XBUS registers associated with the parallel ports



12.1 Introduction

12.1.1 Open drain mode

In the ST10F280 some ports provide Open Drain Control. This makes it possible to switch the output driver of a port pin from a push/pull configuration to an open drain configuration. In push/pull mode a port output driver has an upper and a lower transistor, thus it can actively drive the line either to a high or a low level. In open drain mode the upper transistor is always switched off, and the output driver can only actively drive the line to a low level. When writing a '1' to the port latch, the lower transistor is switched off and the output enters a high-impedance state. The high level must then be provided by an external pull-up device. With this feature, it is possible to connect several port pins together to a Wired-AND configuration, saving external glue logic and/or additional software overhead for enabling/disabling output signals.

This feature is implemented for ports P2, P3, P4, P6, P7 and P8 (see respective sections), and is controlled through the respective Open Drain Control Registers ODPx. These registers allow the individual bit-wise selection of the open drain mode for each port line. If the respective control bit ODPx.y is '0' (default after reset), the output driver is in the push/pull mode. If ODPx.y is '1', the open drain configuration is selected. Note that all ODPx registers are located in the ESFR space.

Figure 27. Output drivers in push/pull mode and in open drain mode

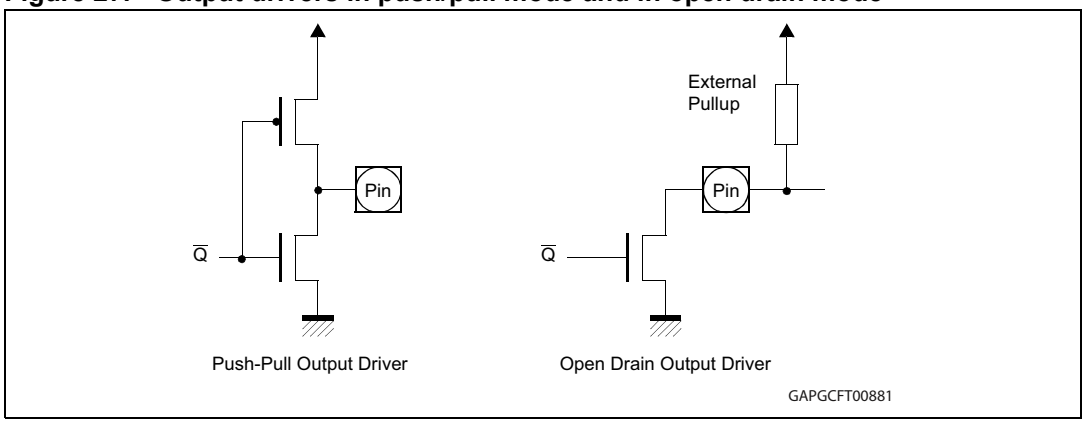
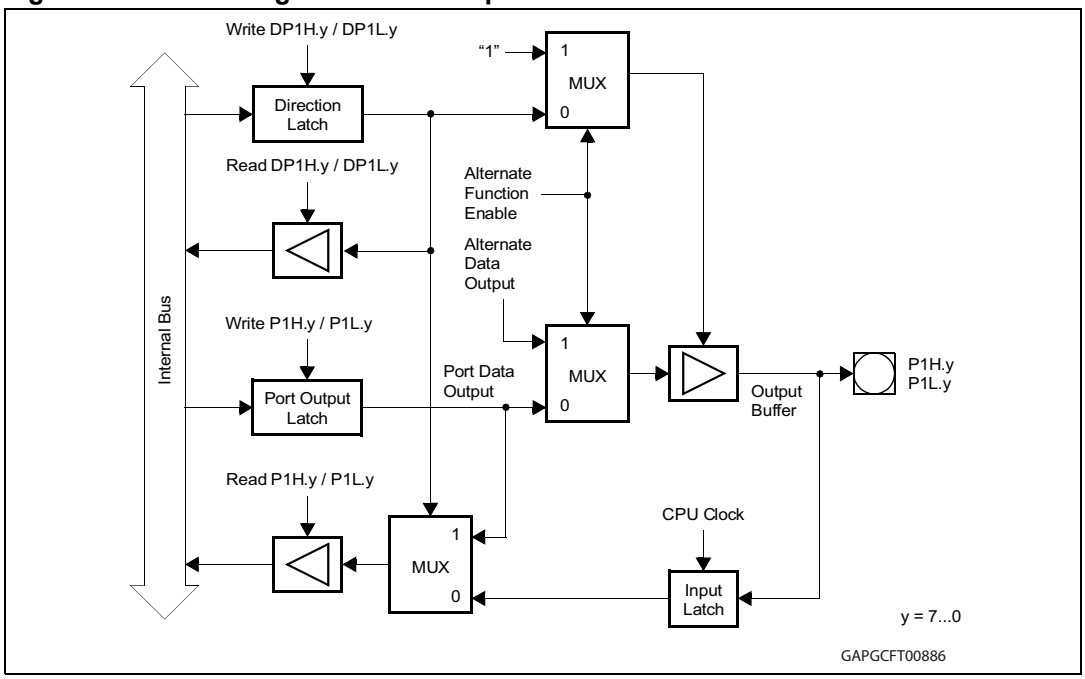


Figure 32. Block diagram of a Port 1 pin



12.4 Port 2

If this 16-bit port is used for general purpose I/O, the direction of each line can be configured via the corresponding direction register DP2. Each port line can be switched into push/pull or open drain mode via the open drain control register ODP2.

P2

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P2.15	P2.14	P2.13	P2.12	P2.11	P2.10	P2.9	P2.8	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: 0xFFC0h / E0h SFR

Reset: 0x0000h

Type: R/W

P2.y Port data register P2 bit y

Figure 39. Block diagram of a Port 4 pin

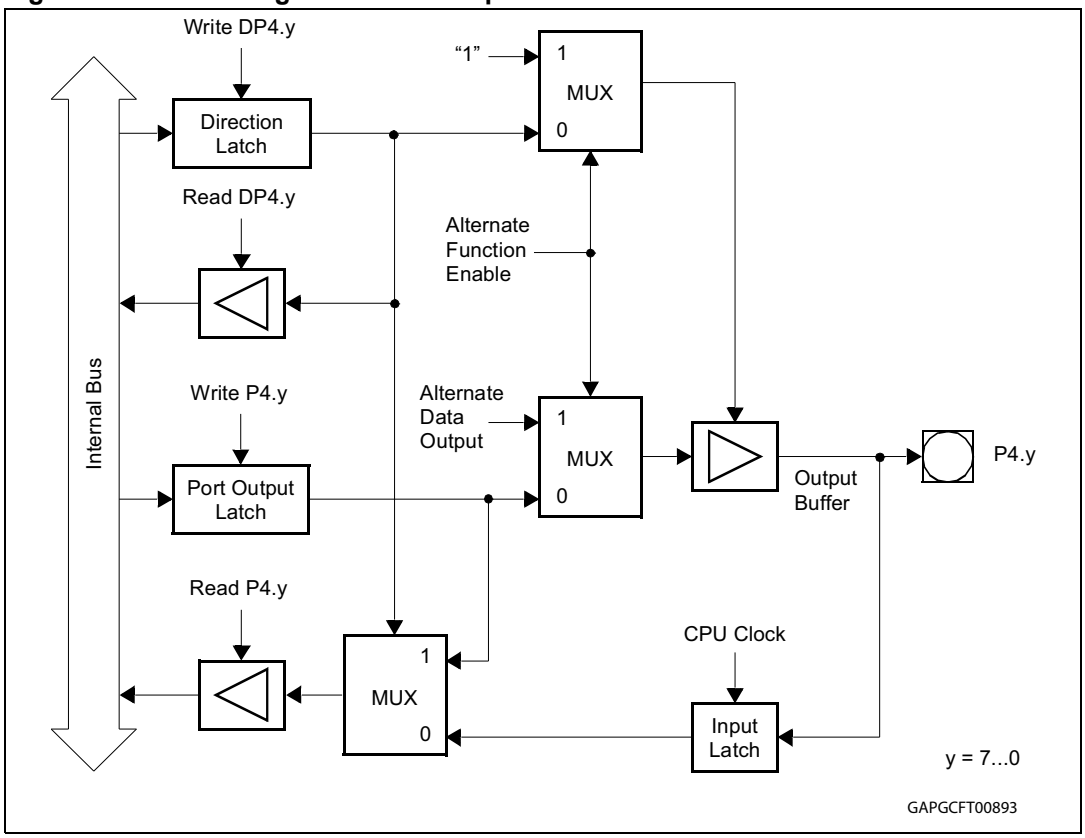
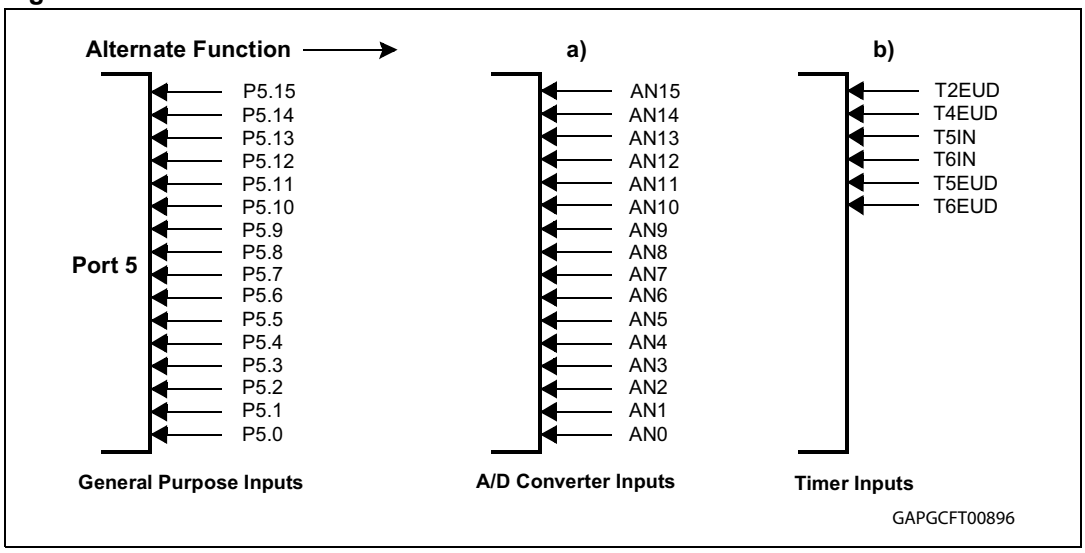
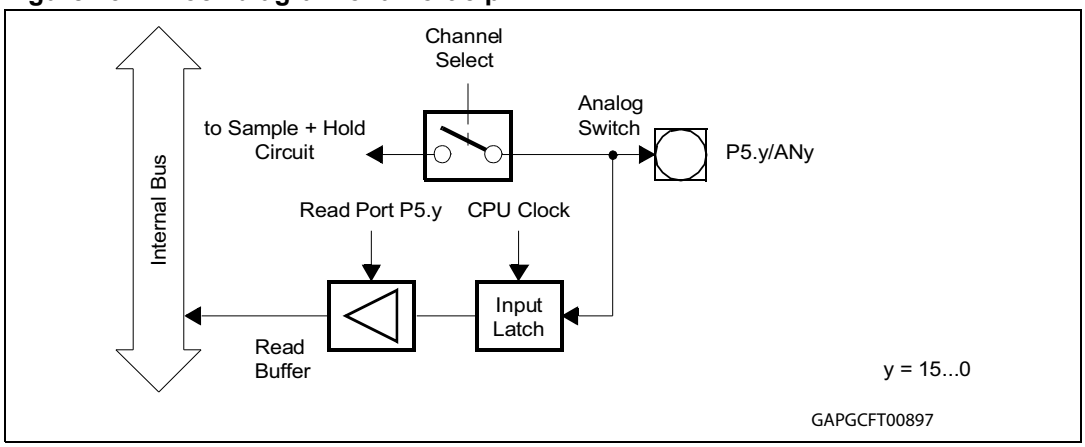


Figure 42. Port 5 I/O and alternate functions



Port 5 pins have a special port structure (see *Figure 43*), first because it is an input only port, and second because the analog input channels are directly connected to the pins rather than to the input latches.

Figure 43. Block diagram of a Port 5 pin



Registers

The XTCVR register input is linked to several sources:

- XTSVR register (start value) for reload when the period is finished, or for load when the timer is starting.
- Incrementer output when the 'up' mode is selected,
- Decrementer output when the 'down' mode is selected.
- The selection between the sources is made through the XTCR control register.

When starting the timer, by setting TEN bit of TCR to '1', XTCVR will be loaded with XTSVR value on the first rising edge of the counting clock. That's to say that for counting from 0000h to 0009h for example, 10 counting clock rising edges are required.

The XTCVR register output is continuously compared to the XTEVR register to detect the end of the counting period. When the registers are equal, several actions are made depending on the XTCR control register content :

- The output XADCINJ is conditionally generated,
- XTCVR is loaded with XTSVR or stops or continues to count (see Table).

XTEVR, XTSVR and all TCR bits except TEN must not be modified while the timer is counting, ie while TEN bit of TCR = '1'. The timer behaviour is not guaranteed if this rule is not respected. It implies that the timer can be configured only when stopped (TEN = '0'). When programming the timer, XTEVR, XTSVR and XTCR bits except TEN can be modified, with TEN = '0'; then the timer is started by modifying only TEN bit of TCR. To stop the timer, only TEN bit should be modified, from '1' to '0'.

Timer output (XADCINJ)

The XADCINJ output is the result of the (XTCVR = XTEVR) flag after differentiation. The duration of the output lasts two cycles (50ns at 40MHz).

Figure 54. XADCINJ timer output

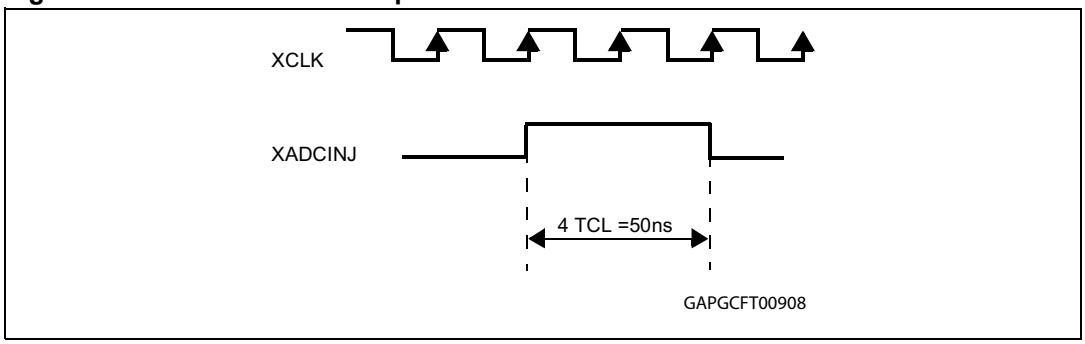
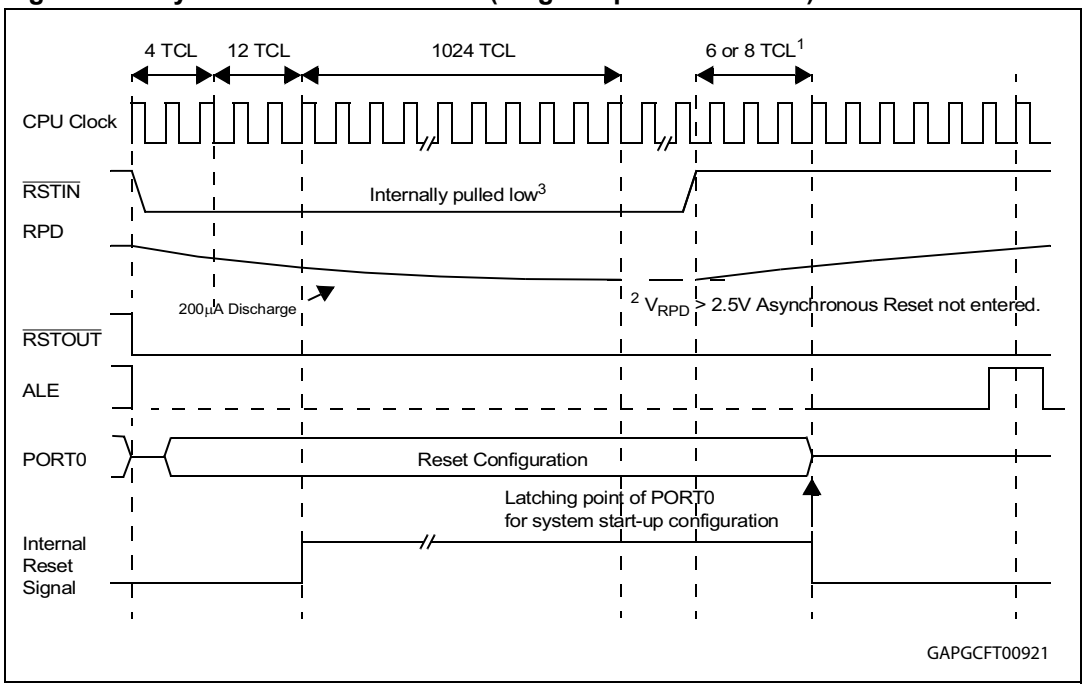


Figure 67. Synchronous warm reset (long low pulse on $\overline{\text{RSTIN}}$)



1. $\overline{\text{RSTIN}}$ rising edge to internal latch of PORT0 is 3 CPU (6 TCL) clock cycles if the PLL is bypassed and the prescaler is on ($f_{CPU} = f_{XTAL} / 2$), else it is 4 CPU clock cycles (8 TCL).
2. If during the reset condition ($\overline{\text{RSTIN}}$ low), V_{RPD} voltage drops below the threshold voltage (about 2.5V for 5V operation), the asynchronous reset is then immediately entered.
3. $\overline{\text{RSTIN}}$ pin is pulled low if bit BDRSTEN (bit 5 of SYSCON register) was previously set by soft-ware. Bit BDRSTEN is cleared after reset.

17.3 Software reset

The reset sequence can be triggered at any time using the protected instruction SRST (software reset). This instruction can be executed deliberately within a program, for example to leave bootstrap loader mode, or upon a hardware trap that reveals a system failure.

Upon execution of the SRST instruction, the internal reset sequence (1024 TCL) is started. The microcontroller behaviour is the same as for a Short Hardware reset, except that only P0.12...P0.6 bit are latched at the end of the reset sequence, while P0.5...P0.2 bit are cleared.

17.4 Watchdog timer reset

When the watchdog timer is not disabled during the initialization or when it is not regularly serviced during program execution it will overflow and it will trigger the reset sequence.

Unlike hardware and software resets, the watchdog reset completes a running external bus cycle if this bus cycle either does not use $\overline{\text{READY}}$, or if $\overline{\text{READY}}$ is sampled active (low) after the programmed wait states. When $\overline{\text{READY}}$ is sampled inactive (high) after the programmed wait states the running external bus cycle is aborted. Then the internal reset sequence is started. At the end of the internal reset sequence (1024 TCL), only P0.12...P0.6 bit are latched, while previously latched values of P0.5...P0.2 are cleared.

SYSCON

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STKSZ			ROMS1	SGTDIS	ROMEN	BYTDIS	CLKEN	WRCFG	CSCFG	PWDCFG	OWDDIS	BDRSTEN	XPEN	VISIBLE	XPER-SHARE
R/W			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: 0xFF12H / 89h SFR

Reset: 0x0XX0h

Type: R/W

PWDCFG Power Down Mode Configuration Control

0: Power Down Mode can only be entered during PWRDN instruction execution if $\overline{\text{NMI}}$ pin is low, otherwise the instruction has no effect. To exit Power Down Mode, an external reset must occurs by asserting the $\overline{\text{RSTIN}}$ pin.

1: Power Down Mode can only be entered during PWRDN instruction execution if all enabled FastExternal Interrupt (EXxIN) pins are in their inactive level. Exiting this mode can be done by asserting one enabled EXxIN pin.

Note: Register SYSCON cannot be changed after execution of the EINIT instruction.

18.2.1 Protected power down mode

This mode is selected by clearing the bit PWDCFG in register SYSCON to '0'.

In this mode, the Power Down mode can only be entered if the $\overline{\text{NMI}}$ (Non Maskable Interrupt) pin is externally pulled low while the PWRDN instruction is executed.

This feature can be used in conjunction with an external power failure signal which pulls the $\overline{\text{NMI}}$ pin low when a power failure is imminent. The microcontroller will enter the $\overline{\text{NMI}}$ trap routine which can save the internal state into RAM. After the internal state has been saved, the trap routine may set a flag or write a certain bit pattern into specific RAM locations, and then execute the PWRDN instruction. If the $\overline{\text{NMI}}$ pin is still low at this time, Power Down mode will be entered, otherwise program execution continues. During power down the voltage delivered by the on-chip voltage regulator automatically lowers the internal logic supply down to 2.5 V, saving the power while the contents of the internal RAM and all registers will still be preserved.

Exiting power down mode

In this mode, the only way to exit Power Down mode is with an external hardware reset.

The initialization routine (executed upon reset) can check the identification flag or bit pattern within RAM to determine whether the controller was initially switched on, or whether it was properly restarted from Power Down mode.

18.2.2 Interruptable power down mode

This mode is selected by setting the bit PWDCFG in register SYSCON to '1'.

Figure 81. External memory cycle: multiplexed bus, with / without read / write delay, extended ALE

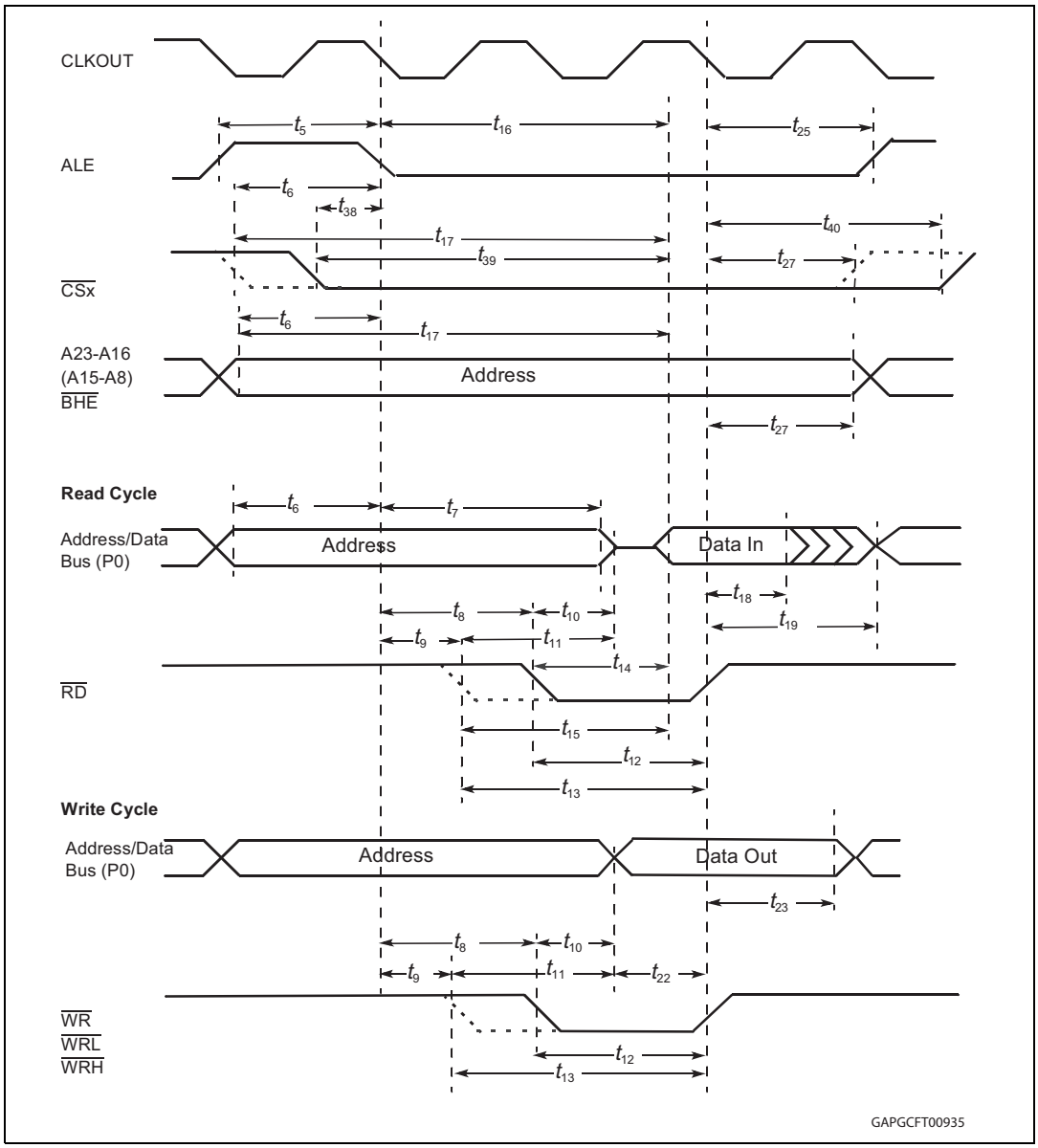
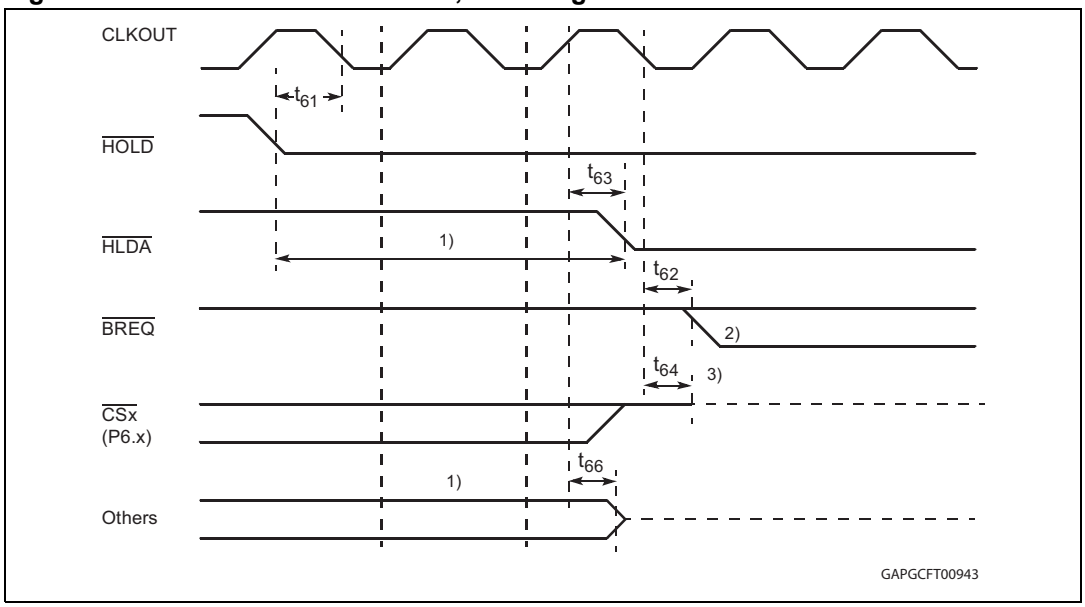


Table 51. External bus arbitration (continued)

Symbol		Parameter	Maximum CPU Clock = 40MHz		Variable CPU Clock 1/2 TCL = 1 to 40MHz		Unit
			Min.	Max.	Min.	Max.	
t_{64}	CC	$\overline{CSx}$ release (1)	–	15	–	15	ns
t_{65}	CC	$\overline{CSx}$ drive	-4	15	-4	15	ns
t_{66}	CC	Other signals release(1)	–	15	–	15	ns
t_{67}	CC	Other signals drive	-4	15	-4	15	ns

1. Partially tested, guaranteed by design characterization

Figure 89. External bus arbitration, releasing the bus



1. The ST10F280 will complete the currently running bus cycle before granting bus access.
2. This is the first possibility for $\overline{BREQ}$ to become active.
3. The $\overline{CS}$ outputs will be resistive high (pull-up) after t_{64}.

22 Ordering information

Table 55. Device summary

Order codes	Package	Packing	Temperature range
ST10F280	PBGA 208 (23 x 23 x 1.96 mm)	Tray	-40°C to +125°C
ST10F280-Q3TR		Tape and reel	