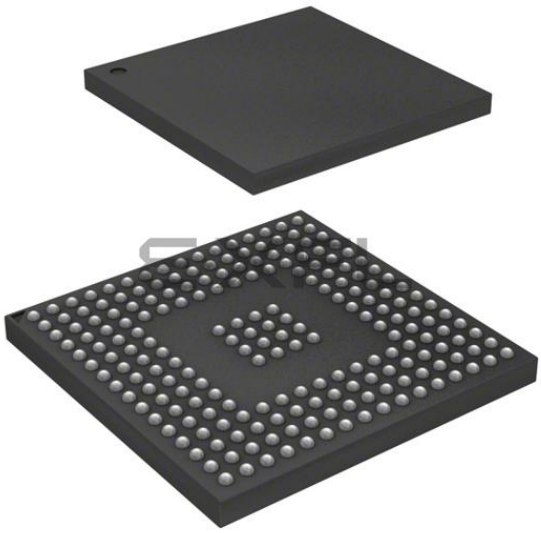

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ST10
Core Size	16-Bit
Speed	40MHz
Connectivity	ASC, CANbus, EBI/EMI, SSC
Peripherals	POR, PWM, WDT
Number of I/O	143
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	18K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 32x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	208-BGA
Supplier Device Package	208-PBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/st10f280

Table 1. Ball description (continued)

Symbol	Ball number	Type	Function
P7.0 – P7.7		I/O	Port 7 is an 8-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 7 outputs can be configured as push/pull or open drain drivers. The input threshold of Port 7 is selectable (TTL or special). The following Port 7 pins also serve for alternate functions:
	J4	O	P7.0 POUT0 PWM Channel 0 Output
	J3	O	P7.1 POUT1 PWM Channel 1 Output
	J2	O	P7.2 POUT2 PWM Channel 2 Output
	J1	O	P7.3 POUT3 PWM Channel 3 Output
	K2	I/O	P7.4 CC28IO CAPCOM2: CC28 Capture Input / Compare Output
	K3	I/O	P7.5 CC29IO CAPCOM2: CC29 Capture Input / Compare Output
	K4	I/O	P7.6 CC30IO CAPCOM2: CC30 Capture Input / Compare Output
	L2	I/O	P7.7 CC31IO CAPCOM2: CC31 Capture Input / Compare Output
XP10.0 – XP10.15		I	XPort 10 is a 16-bit input-only port with Schmitt-Trigger characteristics. The pins of XPort10 also serve as the analog input channels (up to 16) for the A/D converter, where XP10.X equals ANx (Analog input channel x).
	M4	I	XP10.0
	M3	I	XP10.1
	M2	I	XP10.2
	M1	I	XP10.3
	N4	I	XP10.4
	N3	I	XP10.5
	N2	I	XP10.6
	N1	I	XP10.7
	P4	I	XP10.8
	P3	I	XP10.9
	P2	I	XP10.10
	P1	I	XP10.11
	R2	I	XP10.12
	R1	I	XP10.13
	T1	I	XP10.14
	U1	I	XP10.15

Table 1. Ball description (continued)

Symbol	Ball number	Type	Function
P4.0 – P4.7		I/O	Port 4 is an 8-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. The input threshold is selectable (TTL or special). P4.6 & P4.7 outputs can be configured as push-pull or open-drain drivers. In case of an external bus configuration, Port 4 can be used to output the segment address lines:
	N16	O	P4.0 A16 Least Significant Segment Address Line
	M15	O	P4.1 A17 Segment Address Line
	L14	O	P4.2 A18 Segment Address Line
	M16	O	P4.3 A19 Segment Address Line
	L15	O I	P4.4 A20 Segment Address Line CAN2_RxD CAN2 Receive Data Input
	L16	O I	P4.5 A21 Segment Address Line CAN1_RxD CAN1 Receive Data Input
	K14	O O	P4.6 A22 Segment Address Line, CAN_TxD CAN1_TxD CAN1 Transmit Data Output
	K15	O O	P4.7 A23 Most Significant Segment Address Line CAN2_TxD CAN2 Transmit Data Output
RD	J14	O	External Memory Read Strobe. $\overline{RD}$ is activated for every external instruction or data read access.
$\overline{WR}/\overline{WRL}$	J15	O	External Memory Write Strobe. In $\overline{WR}$-mode this pin is activated for every external data write access. In $\overline{WRL}$-mode this pin is activated for low byte data write accesses on a 16-bit bus, and for every data write access on an 8-bit bus. See WRCFG in register SYSCON for mode selection.
READY/ $\overline{READY}$	J16	I	Ready Input. The active level is programmable. When the Ready function is enabled, the selected inactive level at this pin during an external memory access will force the insertion of memory cycle time waitstates until the pin returns to the selected active level.
ALE	J17	O	Address Latch Enable Output. Can be used for latching the address into external memory or an address latch in the multiplexed bus modes.
EA	H17	I	External Access Enable pin. A low level at this pin during and after Reset forces the ST10F280 to begin instruction execution out of external memory. A high level forces execution out of the internal Flash Memory.

Table 1. Ball description (continued)

Symbol	Ball number	Type	Function
XPORT9.0 - XPORT9.15		I/O	XPort 9 is a 16-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. XPort 9 outputs can be configured as push/pull or open drain drivers.
	D15	I/O	XPORT9.0
	C16	I/O	XPORT9.1
	D14	I/O	XPORT9.2
	C15	I/O	XPORT9.3
	B16	I/O	XPORT9.4
	D13	I/O	XPORT9.5
	C14	I/O	XPORT9.6
	B15	I/O	XPORT9.7
	A15	I/O	XPORT9.8
	B14	I/O	XPORT9.9
	C13	I/O	XPORT9.10
	D12	I/O	XPORT9.11
	B13	I/O	XPORT9.12
	C12	I/O	XPORT9.13
	D11	I/O	XPORT9.14
	B12	I/O	XPORT9.15

Table 1. Ball description (continued)

Symbol	Ball number	Type	Function
V_{SS}	A1 A4 A8 A11 A13 A16 A17 B3 B5 B6 B8 B9 B17 D5 D6 F1 F17 G4 H1 K16 K17 L1 L4 N15 N17 R17 T15 T16 U7 U10 U13 U14 U16 U17	-	Digital ground.

bit data bus (byte accesses are possible). Two waitstates give an access time of 100 ns at 40MHz CPU clock. No tristate waitstate is used.

XPORT9, XTIMER, XPORT10, XADCMUX: Address range 00'C000h 00'C3FFh is reserved for the XPORT9, XPORT10, XTIMER and XADCMUX peripherals access. The XPORT9, XTIMER, XPORT10, XADCMUX are enabled by setting XPEN bit 2 of the SYSCON register and the bit 3 of the new XPERCON register. Accesses to the XPORT9, XTIMER, XPORT10 and XADCMUX modules use a 16-bit demultiplexed bus mode without waitstate or read/write delay (50ns access at 40MHz CPU clock). Byte and word access is allowed.

4.1 Visibility of XBUS peripherals

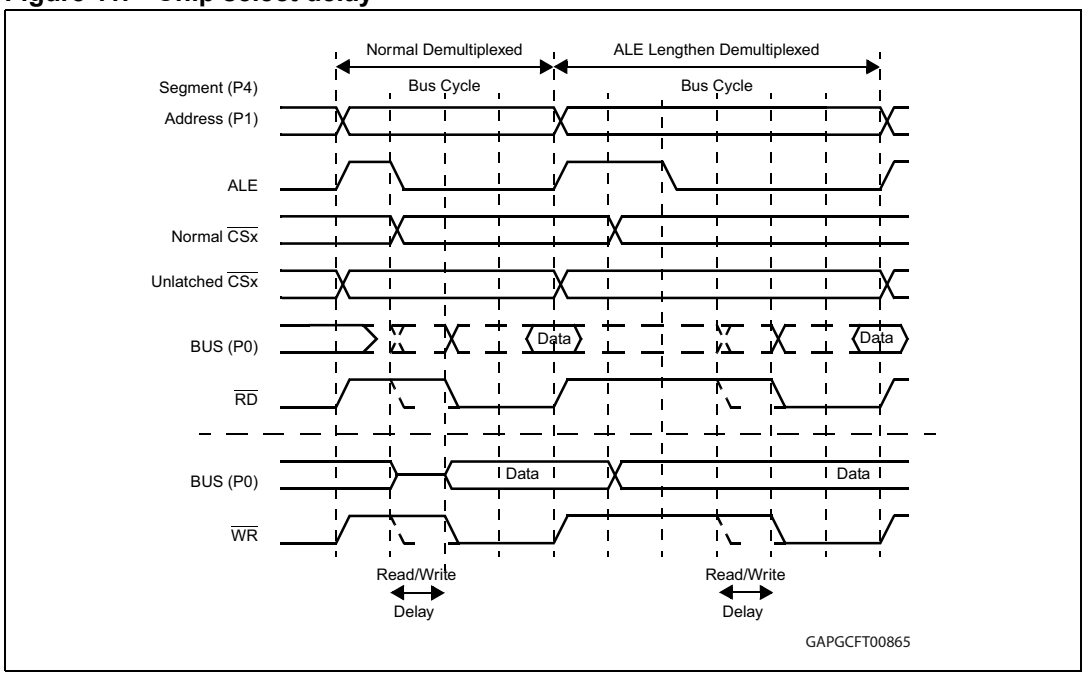
The XBUS peripherals can be separately selected for being visible to the user by means of corresponding selection bits in the XPERCON register. If not selected (not activated with XPERCON bit) before the global enabling with XPEN-bit in SYSCON register, the corresponding address space, port pins and interrupts are not occupied by the peripheral, thus the peripheral is not visible and not available. SYSCON register is described in *Section 19.2: System configuration registers*.

7.1 Programmable chip select timing control

The ST10F280 allows the user to adjust the position of the CSx lines changes. By default (after reset), the CSx lines are changing half a CPU clock cycle (12.5 ns at f_{CPU} = 40MHz) after the rising edge of ALE.

With the CSCFG bit set in the SYSCON register, the CSx lines are changing with the rising edge of ALE, thus the CSx lines are changing at the same time the address lines are changing. See *Section 19.2: System configuration registers* for detailed description of SYSCON register.

Figure 11. Chip select delay

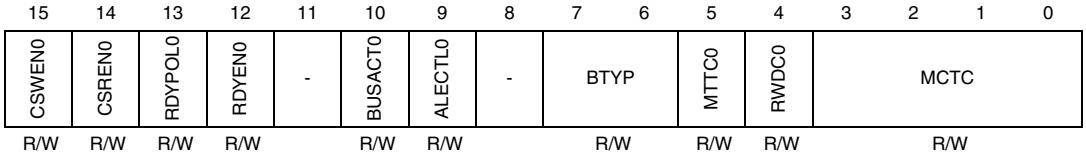


7.2 READY programmable polarity

The active level of the READY pin can be selected by software via the RDYPOL bit in the BUSCONx registers. When the READY function is enabled for a specific address window,

each bus cycle within this window must be terminated with the active level defined by this RDYPOL bit in the associated BUSCON register.

BUSCON0

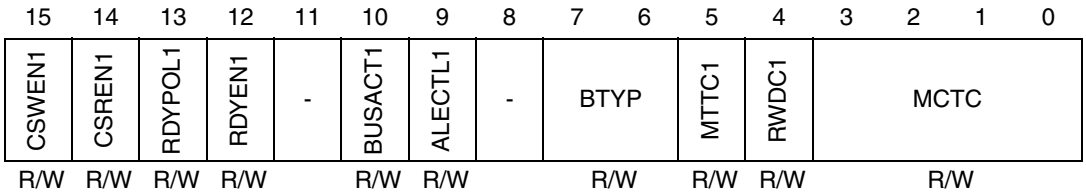


Address: 0xFF0Ch / 86h SFR

Reset: 0x0XX0h

Type: R/W

BUSCON1

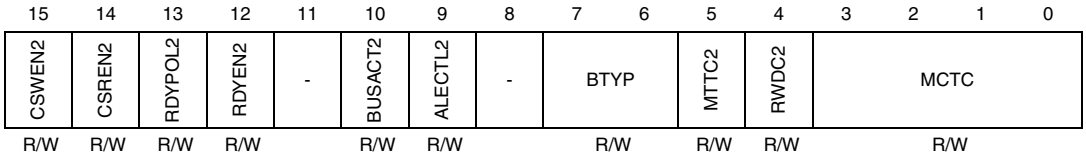


Address: 0xFF14h / 8Ah SFR

Reset: 0x0000h

Type: R/W

BUSCON2



Address: 0xFF16h / 8Bh SFR

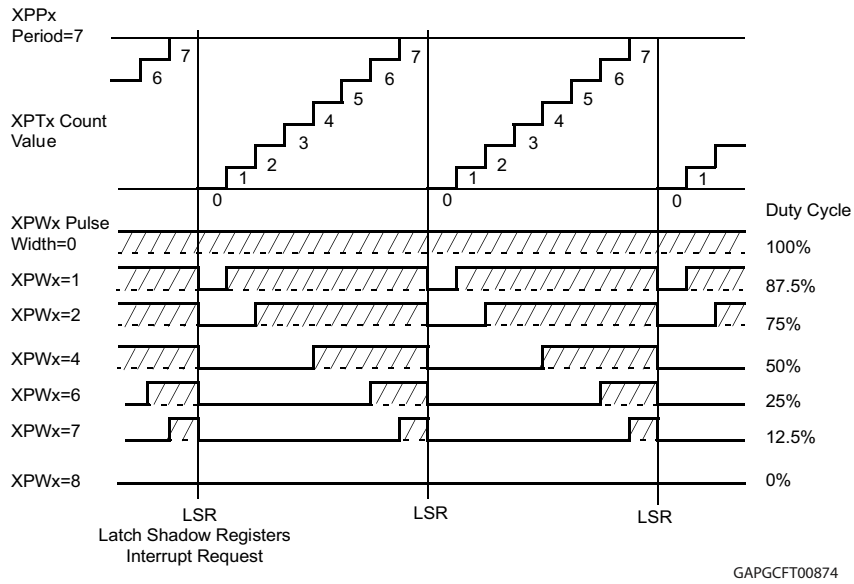
Reset: 0x0000h

Type: R/W

Table 8. Interrupt sources (continued)

Source of Interrupt or PEC service request	Request flag	Enable flag	Interrupt vector	Vector location	Trap number
CAPCOM Register 13	CC13IR	CC13IE	CC13INT	00'0074h	1Dh
CAPCOM Register 14	CC14IR	CC14IE	CC14INT	00'0078h	1Eh
CAPCOM Register 15	CC15IR	CC15IE	CC15INT	00'007Ch	1Fh
CAPCOM Register 16	CC16IR	CC16IE	CC16INT	00'00C0h	30h
CAPCOM Register 17	CC17IR	CC17IE	CC17INT	00'00C4h	31h
CAPCOM Register 18	CC18IR	CC18IE	CC18INT	00'00C8h	32h
CAPCOM Register 19	CC19IR	CC19IE	CC19INT	00'00CCh	33h
CAPCOM Register 20	CC20IR	CC20IE	CC20INT	00'00D0h	34h
CAPCOM Register 21	CC21IR	CC21IE	CC21INT	00'00D4h	35h
CAPCOM Register 22	CC22IR	CC22IE	CC22INT	00'00D8h	36h
CAPCOM Register 23	CC23IR	CC23IE	CC23INT	00'00DCh	37h
CAPCOM Register 24	CC24IR	CC24IE	CC24INT	00'00E0h	38h
CAPCOM Register 25	CC25IR	CC25IE	CC25INT	00'00E4h	39h
CAPCOM Register 26	CC26IR	CC26IE	CC26INT	00'00E8h	3Ah
CAPCOM Register 27	CC27IR	CC27IE	CC27INT	00'00ECh	3Bh
CAPCOM Register 28	CC28IR	CC28IE	CC28INT	00'00F0h	3Ch
CAPCOM Register 29	CC29IR	CC29IE	CC29INT	00'0110h	44h
CAPCOM Register 30	CC30IR	CC30IE	CC30INT	00'0114h	45h
CAPCOM Register 31	CC31IR	CC31IE	CC31INT	00'0118h	46h
CAPCOM Timer 0	T0IR	T0IE	T0INT	00'0080h	20h
CAPCOM Timer 1	T1IR	T1IE	T1INT	00'0084h	21h
CAPCOM Timer 7	T7IR	T7IE	T7INT	00'00F4h	3Dh
CAPCOM Timer 8	T8IR	T8IE	T8INT	00'00F8h	3Eh
GPT1 Timer 2	T2IR	T2IE	T2INT	00'0088h	22h
GPT1 Timer 3	T3IR	T3IE	T3INT	00'008Ch	23h
GPT1 Timer 4	T4IR	T4IE	T4INT	00'0090h	24h
GPT2 Timer 5	T5IR	T5IE	T5INT	00'0094h	25h
GPT2 Timer 6	T6IR	T6IE	T6INT	00'0098h	26h
GPT2 CAPREL Register	CRIR	CRIE	CRINT	00'009Ch	27h
A/D Conversion Complete	ADCIR	ADCIE	ADCINT	00'00A0h	28h
A/D Overrun Error	ADEIR	ADEIE	ADEINT	00'00A4h	29h
ASC0 Transmit	S0TIR	S0TIE	S0TINT	00'00A8h	2Ah
ASC0 Transmit Buffer	S0TBIR	S0TBIE	S0TBINT	00'011Ch	47h

Figure 20. Operation and output waveform in mode 0



Mode 1: symmetrical PWM generation (center aligned PWM)

Mode 1 is selected by setting the respective bit XPMx in register XPWMCON1 to '1'. In this mode the timer XPTx of the respective XPWM channel is counting up until it reaches the value in the associated period shadow register.

Upon the next count pulse the count direction is reversed and the timer starts counting down now with subsequent count pulses until it reaches the value 0000_H. Upon the next count pulse the count direction is reversed again and the count cycle is repeated with the following count pulses.

The XPWM output signal is switched to a high level when the timer contents are equal to or greater than the contents of the pulse width shadow register while the timer is counting up.

The signal is switched back to a low level when the respective timer has counted down to a value below the contents of the pulse width shadow register. So in mode 1 this PWM value controls both edges of the output signal.

Note that in mode 1 the period of the PWM signal is twice the period of the timer:

$$PWM\_Period_{Mode1} = 2 * ([XPPx] + 1)$$

The figure below illustrates the operation and output waveforms of a XPWM channel in mode 1 for different values in the pulse width register.

This mode is referred to as Center Aligned PWM, because the value in the pulse width (shadow) register effects both edges of the output signal symmetrically.

11.2.3 XPWM Control Registers

XPWMCON0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PIR3	PIR2	PIR1	PIR0	PIE3	PIE2	PIE1	PIE0	PTI3	PTI2	PTI1	PTI0	PTR3	PTR2	PTR1	PTR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: 0xEC00h

Reset: 0x0000h

Type: R/W

PTRx XPWM Timer x Run Control Bit
0: Timer XPTx is disconnected from its input clock
1: Timer XPTx is running

PTIx XPWM Timer x Input Clock Selection
0: Timer XPTx clocked with CLK_{CPU}
1: TimerX PTx clocked with CLK_{CPU} / 64

PIEx XPWM Channel x Interrupt Enable Flag
0: Interrupt from channel x disabled
1: Interrupt from channel x enabled

PIRx XPWM Channel x Interrupt Request Flag
0: No interrupt request from channel x
1: Channel x interrupt pending (must be reset via software)

Register XPWMCON0 controls the function of the timers of the four XPWM channels and the channel specific interrupts. Having the control bits organized in functional groups allows e.g. to start or stop all 4 XPWM timers simultaneously with one bitfield instruction. Note: This register is not bit-addressable.

XPWMCON1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PS3	PS2	-	PB01	-	-	-	-	PM3	PM2	PM1	PM0	PEN3	PEN2	PEN1	PEN0
R/W	R/W	-	R/W	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: 0xEC02h

Reset: 0x0000h

Type: R/W

PENx XPWM Channel x Output Enable Bit
0: Channel x output signal disabled, generate interrupt only
1: Channel x output signal enabled

PMx XPWM Channel x Mode Control Bit
0: Channel x operates in mode 0, edge aligned PWM
1: Channel x operates in mode 1, center aligned PWM

PB01 XPWM Channel 0/1 Burst Mode Control Bit
0: Channels 0 and 1 work independently in respective standard mode
1: Outputs of channels 0 and 1 are ANDed to XPWM0 in burst mode

PSx XPWM Channel x Single Shot Mode Control Bit
0: Channel x works in respective standard mode
1: Channel x operates in single shot mode

Register XPWMCON1 controls the operating modes and the outputs of the four XPWM channels. The basic operating mode for each channel (standard = edge aligned, or symmetrical = center aligned PWM mode) is selected by the mode bits XPMx. Burst mode (channels 0 and 1) and single shot mode (channel 2 or 3) are selected by separate control bits. The output signal of each XPWM channel is individually enabled by bit PENx. If the output is not enabled the respective pin can only be used to generate an interrupt request. Note: This register is not bit-addressable.

11.2.4 Interrupt request generation

Each of the four channels of the XPWM module can generate an individual interrupt request. Each of these “channel interrupts” can activate the common “module interrupt”, which actually interrupts the CPU. This common module interrupt is controlled by the XPWM Module Interrupt Control register XP2IC(Xperipherals 2 control register). The interrupt service routine can determine the active channel interrupt(s) from the channel specific interrupt request flags PIRx in register XPWMCON0. The interrupt request flag PIRx of a channel is set at the beginning of a new PWM cycle, i.e. upon loading the shadow registers. This indicates that registers XPPx and XPWx are now ready to receive a new value. If a channel interrupt is enabled via its respective PIEx bit, also the common interrupt request flag XP2IR in register XP2IC is set, provided that it is enabled via the common interrupt enable bit XP2IE.

Note: The channel interrupt request flags (PIRx in register XPWMCON0) are not automatically cleared by hardware upon entry into the interrupt service routine, so they must be cleared via software. The module interrupt request flag XP2IR is cleared by hardware upon entry into the service routine, regardless of how many channel interrupts were active. However, it

12.10 Port 8

If this 8-bit port is used for general purpose I/O, the direction of each line can be configured via the corresponding direction register DP8. Each port line can be switched into push/pull or open drain mode via the open drain control register ODP8.

P8

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	P8.7	P8.6	P8.5	P8.4	P8.3	P8.2	P8.1	P8.0
								R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: 0xFFD40h / EAh SFR

Reset: 0x--00h

Type: R/W

P8.y Port data register P8 bit y

DP8

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	DP8.7	DP8.6	DP8.5	DP8.4	DP8.3	DP8.2	DP8.1	DP8.0
								R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: 0xFFD6h / EBh SFR

Reset: 0x--00h

Type: R/W

DP8.y Port direction register DP8 bit y
DP8.y = 0: Port line P8.y is an input (high impedance)
DP8.y = 1: Port line P8.y is an output

ODP8

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	ODP8.7	ODP8.6	ODP8.5	ODP8.4	ODP8.3	ODP8.2	ODP8.1	ODP8.0
								R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: 0xF1D6h / EBh ESFR

Reset: 0x--00h

Type: R/W

ODP8.y Port 8 Open Drain control register bit y
ODP8.y = 0: Port line P8.y output driver in push-pull mode
ODP8.y = 1: Port line P8.y output driver in open drain mode

Registers

The XTCVR register input is linked to several sources:

- XTSVR register (start value) for reload when the period is finished, or for load when the timer is starting.
- Incrementer output when the 'up' mode is selected,
- Decrementer output when the 'down' mode is selected.
- The selection between the sources is made through the XTCR control register.

When starting the timer, by setting TEN bit of TCR to '1', XTCVR will be loaded with XTSVR value on the first rising edge of the counting clock. That's to say that for counting from 0000h to 0009h for example, 10 counting clock rising edges are required.

The XTCVR register output is continuously compared to the XTEVR register to detect the end of the counting period. When the registers are equal, several actions are made depending on the XTCR control register content :

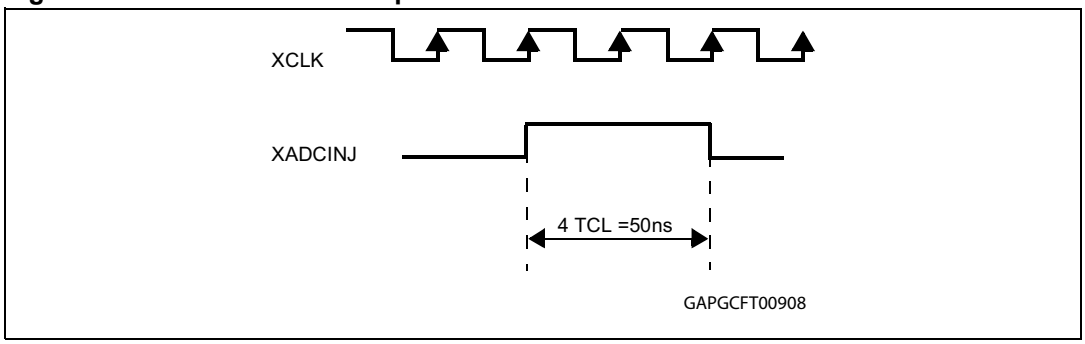
- The output XADCINJ is conditionally generated,
- XTCVR is loaded with XTSVR or stops or continues to count (see Table).

XTEVR, XTSVR and all TCR bits except TEN must not be modified while the timer is counting, ie while TEN bit of TCR = '1'. The timer behaviour is not guaranteed if this rule is not respected. It implies that the timer can be configured only when stopped (TEN = '0'). When programming the timer, XTEVR, XTSVR and XTCR bits except TEN can be modified, with TEN = '0'; then the timer is started by modifying only TEN bit of TCR. To stop the timer, only TEN bit should be modified, from '1' to '0'.

Timer output (XADCINJ)

The XADCINJ output is the result of the (XTCVR = XTEVR) flag after differentiation. The duration of the output lasts two cycles (50ns at 40MHz).

Figure 54. XADCINJ timer output



Upper Mask of Last Message

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID20...18			ID17...13					ID28...21							
R/W			R/W					R/W							

Address: 0xEF0Ch / EE0Ch XReg

Reset: 0xUUUUh

Type: R/W

Lower Mask of Last Message

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID4...0					0	0	0	ID12...5							
R/W					R	R	R	R/W							

Address: 0xEF0Eh / EE0Eh XReg

Reset: 0xUUUUh

Type: R, R/W

ID28...0 Identifier (29 bit)
Mask to filter the last incoming message (Nr. 15) with standard or extended identifier (as configured).

15.5 The message object

The message object is the primary means of communication between CPU and CAN controller. Each of the 15 message objects uses 15 consecutive bytes (see *Figure 60*) and starts at an address that is a multiple of 16.

Note: All message objects must be initialized by the CPU, even those which are not going to be used, before clearing the INIT bit.

Each element of the Message Control Register is made of two complementary bits.

This special mechanism allows the selective setting or resetting of specific elements (leaving others unchanged) without requiring read-modify-write cycles. None of these elements will be affected by reset.

The *Table 32* shows how to use and to interpret these 2 bit-fields.

Table 38. Special function registers listed by name (continued)

Name	Physical address	8-bit address	Description	Reset value
T6CON b	FF48h	A4h	GPT2 Timer 6 Control Register	0000h
T6IC b	FF68h	B4h	GPT2 Timer 6 Interrupt Control Register	- - 00h
T7	F050h E	28h	CAPCOM Timer 7 Register	0000h
T78CON b	FF20h	90h	CAPCOM Timer 7 and 8 Control Register	0000h
T7IC b	F17Ah E	BEh	CAPCOM Timer 7 Interrupt Control Register	- - 00h
T7REL	F054h E	2Ah	CAPCOM Timer 7 Reload Register	0000h
T8	F052h E	29h	CAPCOM Timer 8 Register	0000h
T8IC b	F17Ch E	BFh	CAPCOM Timer 8 Interrupt Control Register	- - 00h
T8REL	F056h E	2Bh	CAPCOM Timer 8 Reload Register	0000h
TFR b	FFACh	D6h	Trap Flag Register	0000h
WDT	FEAEh	57h	Watchdog Timer Register (read only)	0000h
WDTCON b	FFAEh	D7h	Watchdog Timer Control Register	00xxh(2)
XP0IC b	F186h E	C3h	CAN1 Module Interrupt Control Register	- - 00h(3)
XP1IC b	F18Eh E	C7h	CAN2 Module Interrupt Control Register	- - 00h(3)
XP2IC b	F196h E	CBh	XPWM Interrupt Control Register	- - 00h(3)
XP3IC b	F19Eh E	CFh	PLL unlock Interrupt Control Register	- - 00h(3)
XPERCON	F024h E	12h	XPER Configuration Register	- - 05h
ZEROS b	FF1Ch	8Eh	Constant Value 0's Register (read only)	0000h

1. The system configuration is selected during reset.
2. Bit WDTR indicates a watchdog timer triggered reset.
3. The XPnIC Interrupt Control Registers control interrupt requests from integrated X-Bus peripherals. Some software controlled interrupt requests may be generated by setting the XPnIR bits (of XPnIC register) of the unused X-peripheral nodes.

Table 39. X registers listed by name

Name	Physical address	Description	Reset value
CAN1BTR	EF04h	CAN1 Bit Timing Register	XXXXh
CAN1CSR	EF00h	CAN1 Control/Status Register	XX01h
CAN1GMS	EF06h	CAN1 Global Mask Short	XFXXh
CAN1IR	EF02h	CAN1 Interrupt Register	- - XXh
CAN1LAR1--15	EF14--EFF4h	CAN1 Lower Arbitration register 1 to 15	XXXXh
CAN1LGML	EF0Ah	CAN1 Lower Global Mask Long	XXXXh
CAN1LMLM	EF0Eh	CAN1 Lower Mask Last Message	XXXXh
CAN1MCR1--15	EF10--EFF0h	CAN1 Message Control Register 1 to 15	XXXXh
CAN1MO1--15	EF1x--EFFxh	CAN1 Message Object 1 to 15	XXXXh

CLKSEL System Clock Selection
000: $f_{CPU} = 2.5 \times f_{OSC}$
001: $f_{CPU} = 0.5 \times f_{OSC}$
010: $f_{CPU} = 10 \times f_{OSC}$
011: $f_{CPU} = f_{OSC}$
100: $f_{CPU} = 5 \times f_{OSC}$
101: $f_{CPU} = 2 \times f_{OSC}$
110: $f_{CPU} = 3 \times f_{OSC}$
111: $f_{CPU} = 4 \times f_{OSC}$

EXICON

15 14	13 12	11 10	9 8	7 6	5 4	3 2	1 0
EXI7ES	EXI6ES	EXI5ES	EXI4ES	EXI3ES	EXI2ES	EXI1ES	EXI0ES
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: 0xF1C0h / E0h ESFR

Reset: 0x0000h

Type: R/W

EXIxES(x=7...0) External Interrupt x Edge Selection Field (x=7...0)
00: Fast external interrupts disabled: standard mode
EXxIN pin not taken in account for entering/exiting Power Down mode.
01: Interrupt on positive edge (rising)
Enter Power Down mode if EXiIN = '0', exit if EXxIN = '1' (referred as 'high' active level)
10: Interrupt on negative edge (falling)
Enter Power Down mode if EXiIN = '1', exit if EXxIN = '0' (referred as 'low' active level)
11: Interrupt on any edge (rising or falling)
Always enter Power Down mode, exit if EXxIN level changed.

EXISEL

15 14	13 12	11 10	9 8	7 6	5 4	3 2	1 0
EXI7SS	EXI6SS	EXI5SS	EXI4SS	EXI3SS	EXI2SS	EXI1SS	EXI0SS
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: 0xF1DAh / EDh ESFR

Reset: 0x0000h

Type: R/W

EXIxSS External Interrupt x Source Selection (x=7...0)
00: Input from associated Port 2 pin.
01: Input from "alternate source".
10: Input from Port 2 pin ORed with "alternate source".
11: Input from Port 2 pin ANDed with "alternate source".

Figure 85. External memory cycle: demultiplexed bus, with / without read / write delay, extended ALE

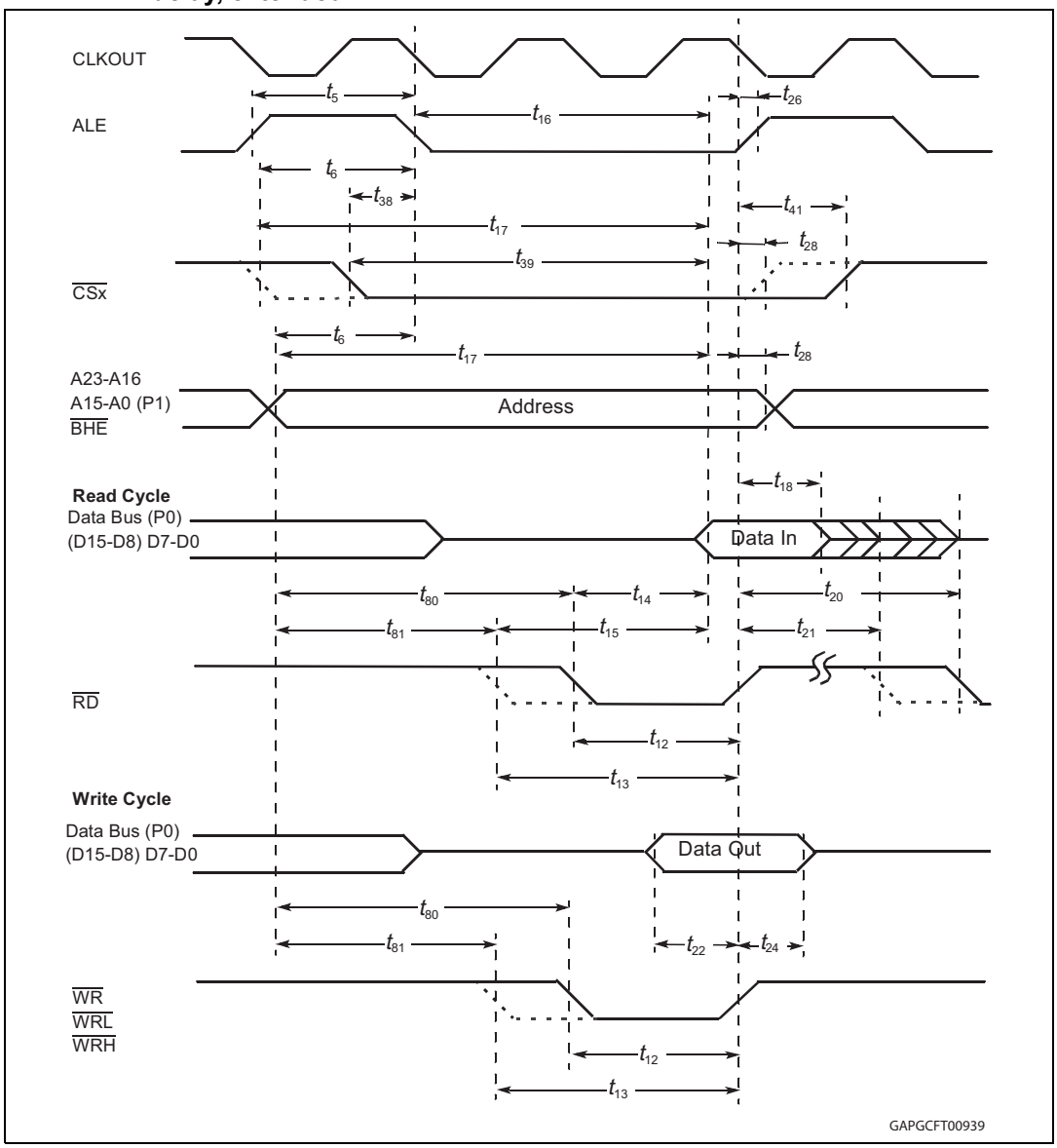


Figure 86. External memory cycle: demultiplexed bus, with / without read / write delay, normal ALE, read / write chip select

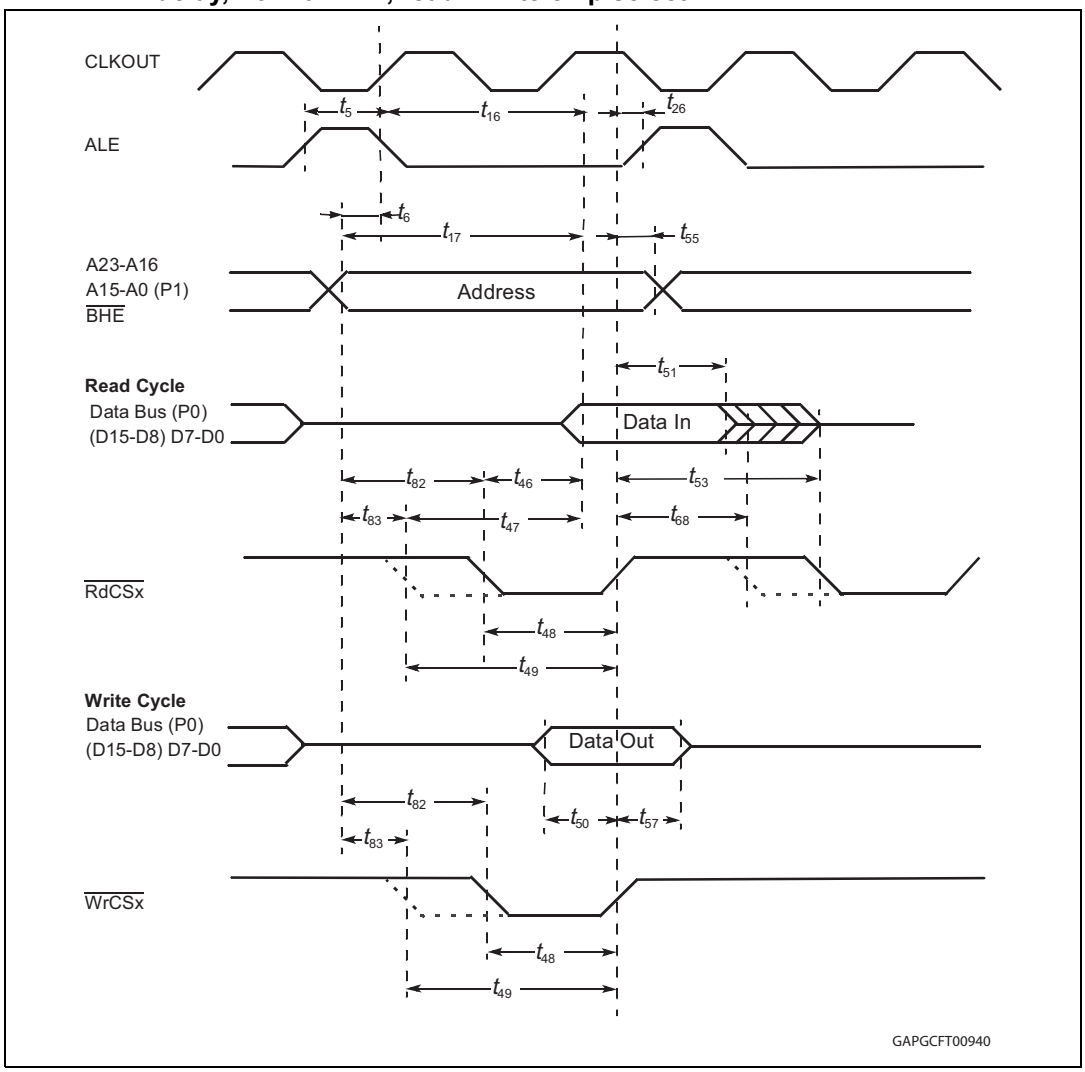
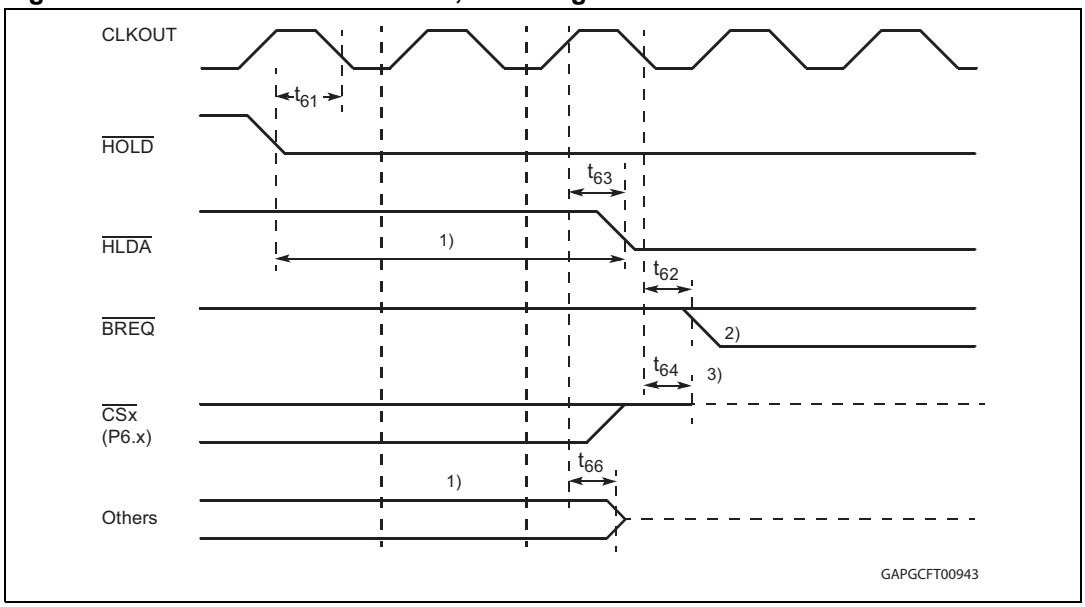


Table 51. External bus arbitration (continued)

Symbol		Parameter	Maximum CPU Clock = 40MHz		Variable CPU Clock 1/2 TCL = 1 to 40MHz		Unit
			Min.	Max.	Min.	Max.	
t_{64}	CC	$\overline{CSx}$ release (1)	–	15	–	15	ns
t_{65}	CC	$\overline{CSx}$ drive	-4	15	-4	15	ns
t_{66}	CC	Other signals release(1)	–	15	–	15	ns
t_{67}	CC	Other signals drive	-4	15	-4	15	ns

1. Partially tested, guaranteed by design characterization

Figure 89. External bus arbitration, releasing the bus



1. The ST10F280 will complete the currently running bus cycle before granting bus access.
2. This is the first possibility for $\overline{BREQ}$ to become active.
3. The $\overline{CS}$ outputs will be resistive high (pull-up) after t_{64}.