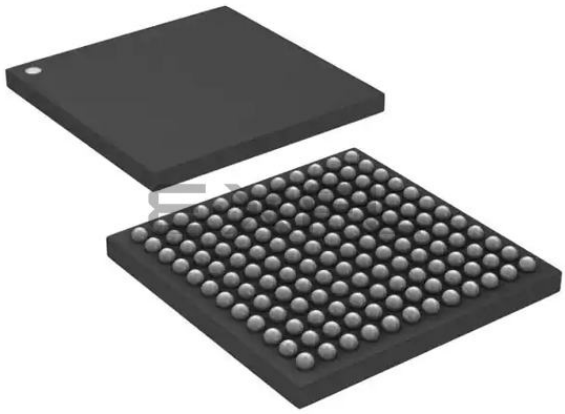

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM7®
Core Size	32-Bit Single-Core
Speed	36MHz
Connectivity	CANbus, I²C, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	112
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LFBGA
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/str730fz1h7

1 Scope

This datasheet provides the STR73x ordering information, mechanical and electrical device characteristics.

For complete information on the STR73xF microcontroller memory, registers and peripherals. please refer to the STR73x reference manual.

For information on programming, erasing and protection of the internal Flash memory please refer to the STR7 Flash programming reference manual.

For information on the ARM7TDMI core please refer to the ARM7TDMI technical reference manual.

1.1 Description

ARM core with embedded Flash & RAM

STR73xF family combines the high performance ARM7TDMI™ CPU with an extensive range of peripheral functions and enhanced I/O capabilities. All devices have on-chip high-speed single voltage Flash memory and high-speed RAM. The STR73xF family has an embedded ARM core and is therefore compatible with all ARM tools and software.

Extensive tools support

STMicroelectronics' 32-bit, ARM core-based microcontrollers are supported by a complete range of high-end and low-cost development tools to meet the needs of application developers. This extensive line of hardware/software tools includes starter kits and complete development packages all tailored for ST's ARM core-based MCUs.

The range of development packages includes third-party solutions that come complete with a graphical development environment and an in-circuit emulator/programmer featuring a JTAG application interface. These support a range of embedded operating systems (OS), while several royalty-free OSs are also available.

For more information, please refer to ST MCU site http://www.st.com/mcu

Figure 1 shows the general block diagram of the device family.

Flexible clock control

Two clock sources are used to drive the microcontroller, a main clock driven by an external crystal or ceramic resonator and an internal backup RC oscillator that operates at 2 MHz or 32 kHz. The embedded PLL can be configured to generate an internal system clock of up to 36 MHz. The PLL output frequency can be programmed using a wide selection of multipliers and dividers.

Voltage regulators

The STR73xF requires an external 4.5 to 5.5 V power supply. There are two internal Voltage Regulators for generating the 1.8 V power supply needed by the core and peripherals. The main VR is switched off and the Low Power VR switched on when the application puts the STR73xF in Low Power Wait for Interrupt (LPWFI) mode.

Low voltage detectors

The voltage regulator and Flash modules each have an embedded LVD that monitors the internal 1.8 V supply. If the voltage drops below a certain threshold, the LVD will reset the STR73xF.

Note: An external power-on reset must be provided ensure the microcontroller starts-up correctly.

2.1 On-chip peripherals

CAN interfaces

The three CAN modules are compliant with the CAN specification V2.0 part B (active). The bit rate can be programmed up to 1 MBaud. These are not available in the STR735 and STR736.

DMA

4 DMA controllers, each with 4 data streams manage memory to memory, peripheral to peripheral, peripheral to memory and memory to peripheral transfers. The DMA requests are connected to TIM timers, BSPI0, BSPI1, BSPI2 and ADC. One of the streams can be configured to be triggered by a software request, independently from any peripheral activity.

16-bit timers (TIM)

Each of the ten timers (six in 100-pin devices) have a 16-bit free-running counter with 7-bit prescaler, up to two input capture/output compare functions, a pulse counter function, and a PWM channel with selectable frequency. This provides a total of 16 independent PWMs (12 in 100-pin devices) when added with the PWM modules (see next paragraph).

PWM modules (PWM)

The six 16-bit PWM modules have independently programmable periods and duty-cycles, with 5+3 bit prescaler factor.

Timebase timers (TB)

The three 16-bit timebase timers with 8-bit prescaler for general purpose time triggering operations.

Real-time clock (RTC)

The RTC provides a set of continuously running counters driven by separate clock signal derived from the main oscillator. The RTC can be used as a general timebase or

3 Block diagram

Figure 1. STR730F/STR735F block diagram

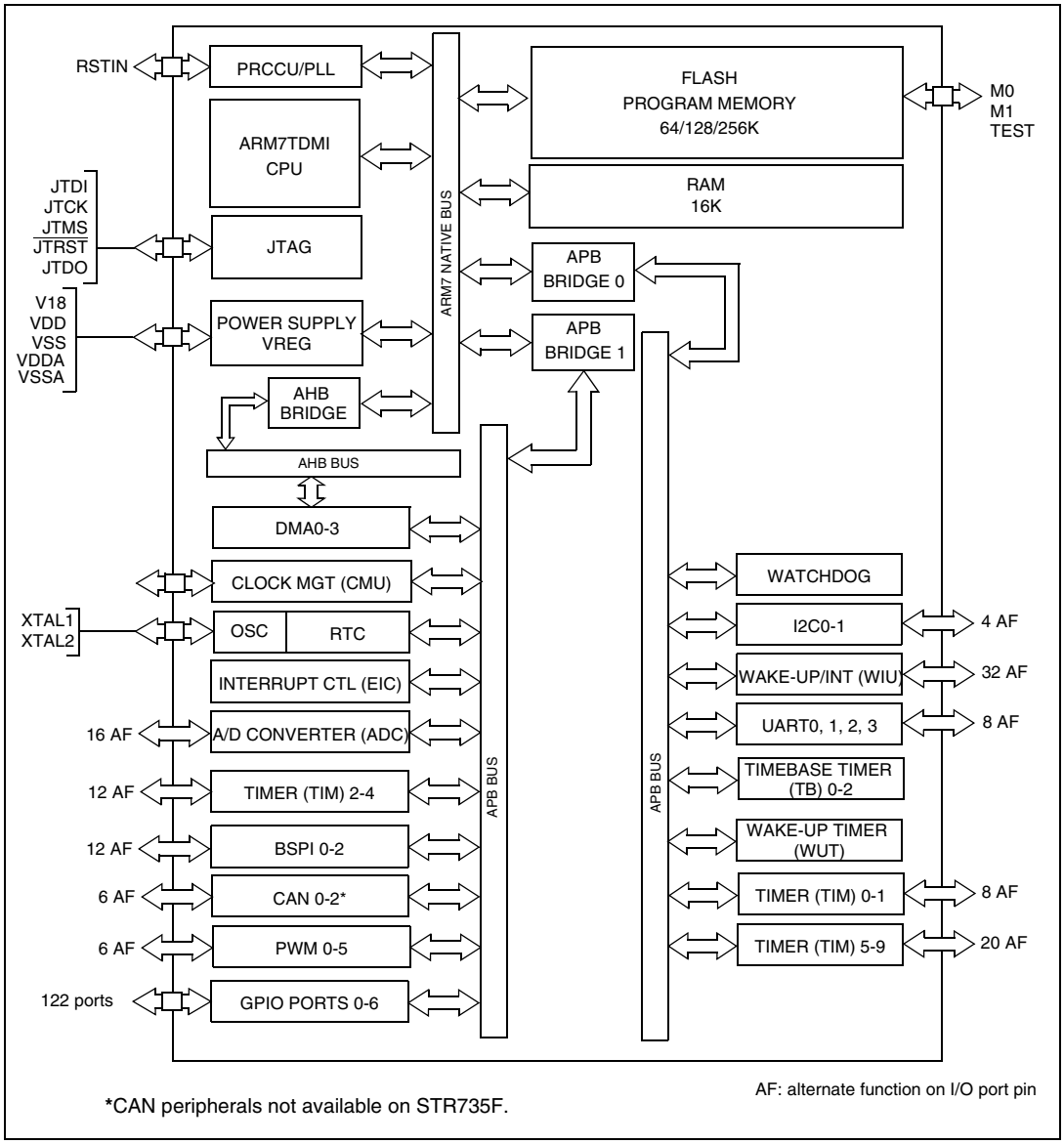
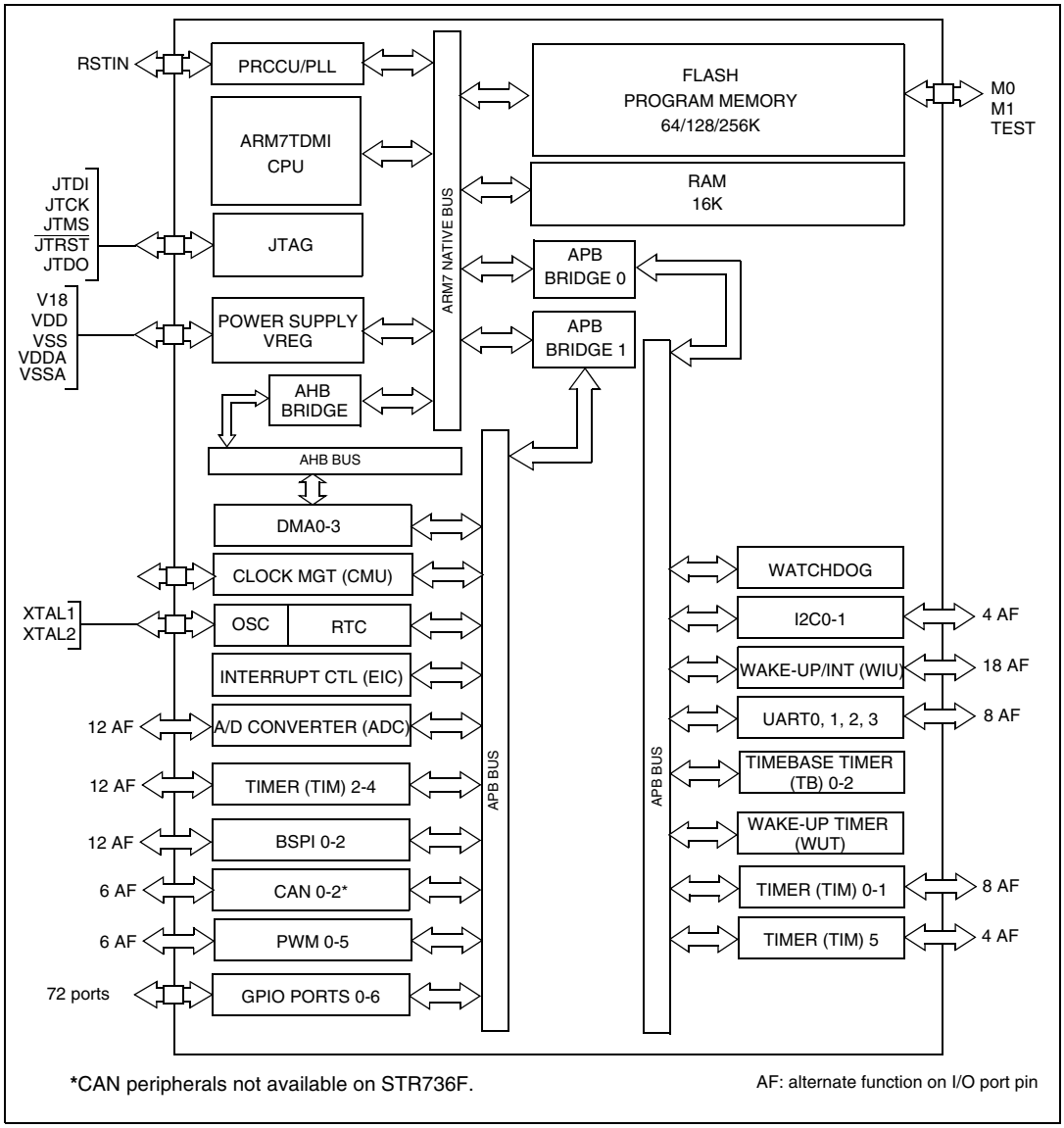


Figure 2. STR731F/STR736 block diagram



*CAN peripherals not available on STR736F.

AF: alternate function on I/O port pin

3.1 Related documentation

Available from www.arm.com:

ARM7TDMI technical reference manual

Available from http://www.st.com:

STR73x reference manual (RM0001)

STR7 Flash programming reference manual

STR73x software library user manual

For a list of related application notes refer to http://www.st.com.

Table 4. STR73xF pin description

Pin n°			Pin name	Type	Input			Output			Main function (after reset)	Alternate function
TQFP144	LFBGA144	TQFP100			Input Level	pu/pd	interrupt	Capability	OD	PP		
119	B8	84	P5.9/PWM5	I/O	T_T		INT7	2mA	X	X	Port 5.9	PWM5: PWM output (TQFP100 only)
120	C8	85	P5.10/RDI2	I/O	T_T		INT8	2mA	X	X	Port 5.10	UART2: receive data input
121	A12	86	P5.11/TDO2	I/O	T_T		INT9	2mA	X	X	Port 5.11	UART2: transmit data output
122	D8	87	P5.12	I/O	T_T		INT10	2mA	X	X	Port 5.12	
123	E8		P5.13	I/O	T_T		INT11	2mA	X	X	Port 5.13	
124	B7		P5.14	I/O	T_T		INT12	2mA	X	X	Port 5.14	
125	A7		P5.15	I/O	T_T		INT13	2mA	X	X	Port 5.15	
126	A6	88	V_{18}	S								1.8 V decoupling pin: a decoupling capacitor (recommended value: 100 nF) must be connected between this pin and nearest VSS pin.
127	C7	89	V_{SS}	S								Ground
128	D7	90	V_{DD}	S								Supply voltage (5 V)
129	E7	91	P6.0	I/O	T_T		WUP0	8mA	X	X	Port 6.0	
130	F7		P6.1	I/O	T_T		WUP1	2mA	X	X	Port 6.1	
131	B6	92	P6.2/RDI3	I/O	T_T		WUP2	2mA	X	X	Port 6.2	UART3: receive data input
132	C6		P6.3	I/O	T_T		WUP3	2mA	X	X	Port 6.3	
133	D6	93	P6.4/TDO3	I/O	T_T		WUP4	2mA	X	X	Port 6.4	UART3: transmit data output
134	E6		P6.5	I/O	T_T		WUP5	2mA	X	X	Port 6.5	
135	A5	94	P6.6	I/O	T_T		WUP6	2mA	X	X	Port 6.6	
136	B5		P6.7	I/O	T_T		WUP7	2mA	X	X	Port 6.7	
137	C5	95	P6.8/RDI0	I/O	T_T		WUP10	2mA	X	X	Port 6.8	UART0: receive data input
138	A3	96	P6.9/TDO0	I/O	T_T			2mA	X	X	Port 6.9	UART0: transmit data output
139	A2		P6.10	I/O	T_T		WUP8	2mA	X	X	Port 6.10	
140	D5	97	P6.11/MISO0	I/O	T_T			2mA	X	X	Port 6.11	BSPI0: master input/slave output
141	A4	98	P6.12/MOSI0	I/O	T_T			2mA	X	X	Port 6.12	BSPI0: master output/slave input
142	B4	99	P6.13/SCK0	I/O	T_T		WUP11	2mA	X	X	Port 6.13	BSPI0: serial clock
143	C4	100	P6.14/$\overline{SS}$0	I/O	T_T			2mA	X	X	Port 6.14	BSPI0: slave select
144	B3		P6.15	I/O	T_T		WUP9	2mA	X	X	Port 6.15	

3.3 Memory mapping

Figure 5 shows the various memory configurations of the STR73xF system. The system memory map (from 0x0000_0000 to 0xFFFF_FFFF) is shown on the left part of the figure, the right part shows maps of the Flash and APB areas. For flexibility the Flash or RAM addresses can be aliased to Block 0 addresses using the remapping feature

Most reserved memory spaces (gray shaded areas in *Figure 5*) are protected from access by the user code. When an access this memory space is attempted, an ABORT signal is generated. Depending on the type of access, the ARM processor will enter “prefetch abort” state (Exception vector 0x0000_000C) or “data abort” state (Exception vector 0x0000_0010). It is up to the application software to manage these abort exceptions.

Figure 5. Memory map

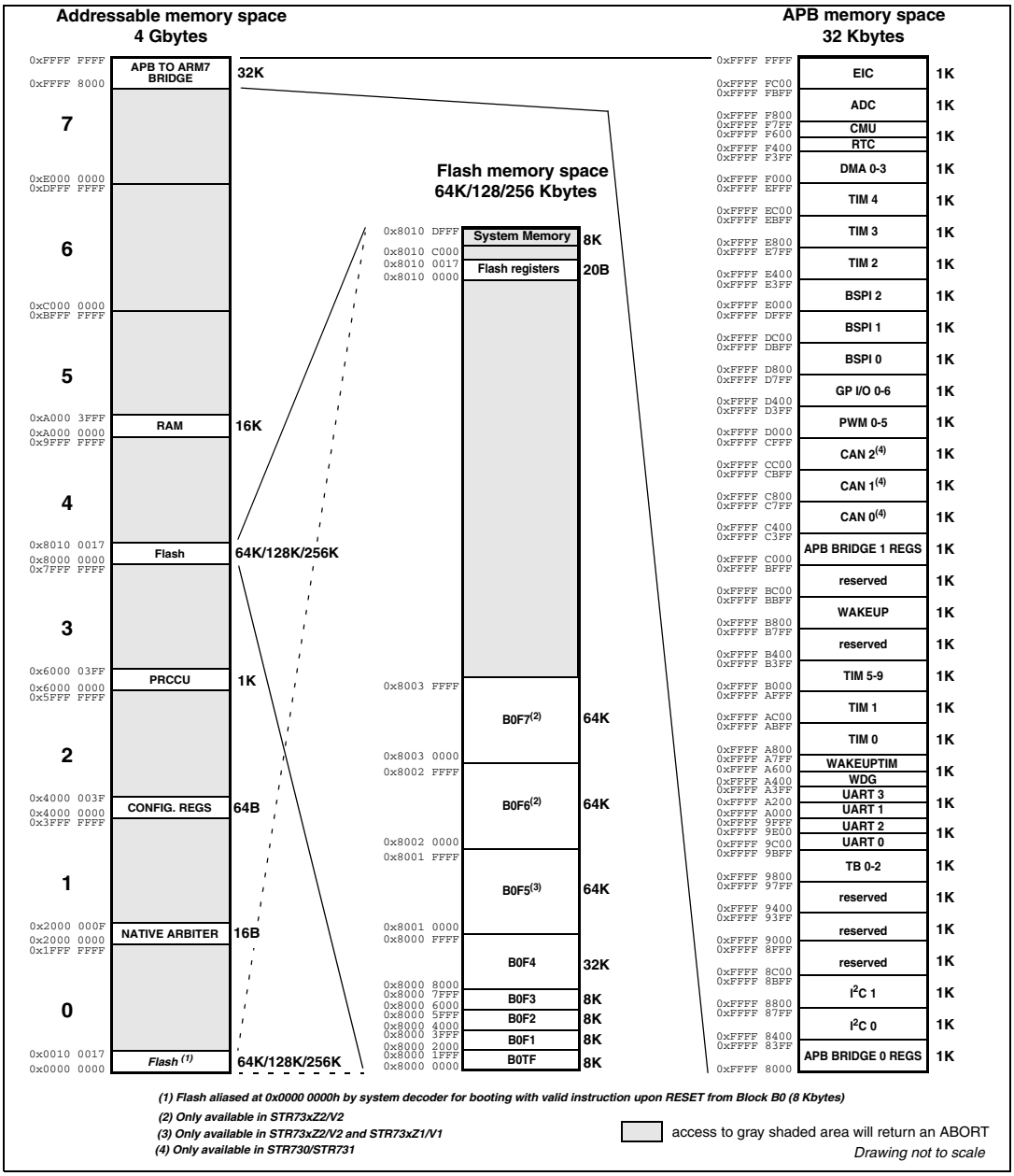


Table 7. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-55 to +150	°C
T_J	Maximum junction temperature (see *Section 5.2: Thermal characteristics on page 48*)		

Figure 8. STOP I_{DD} vs. VDD

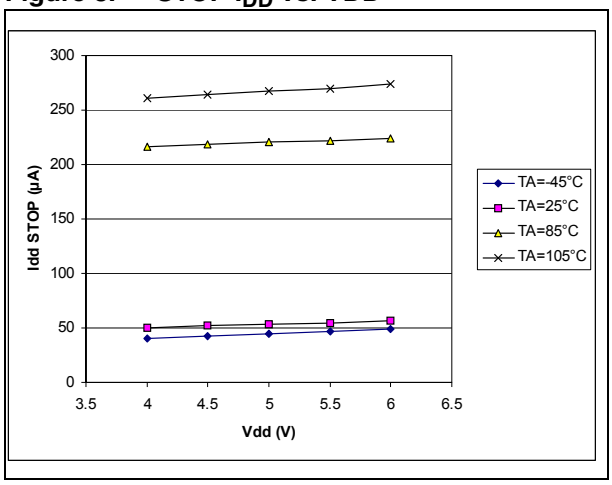


Figure 9. HALT I_{DD} vs. V_{DD}

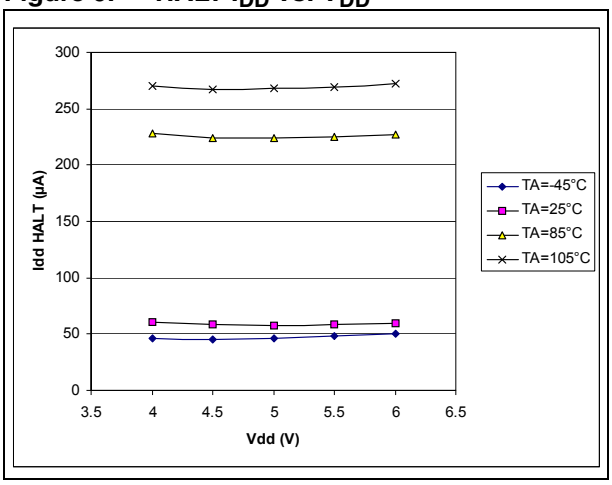


Figure 10. WFI I_{DD} vs. V_{DD}

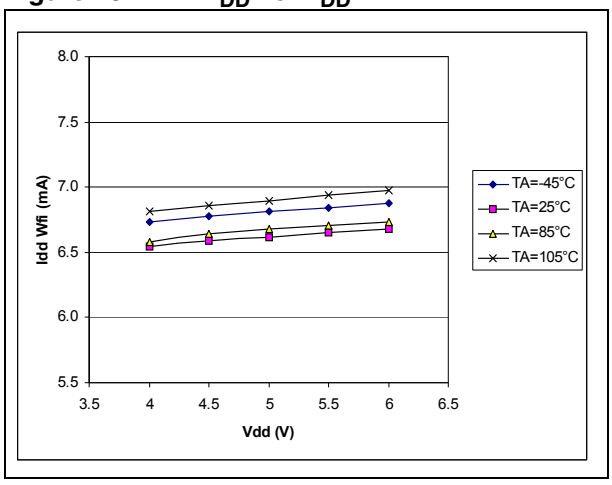
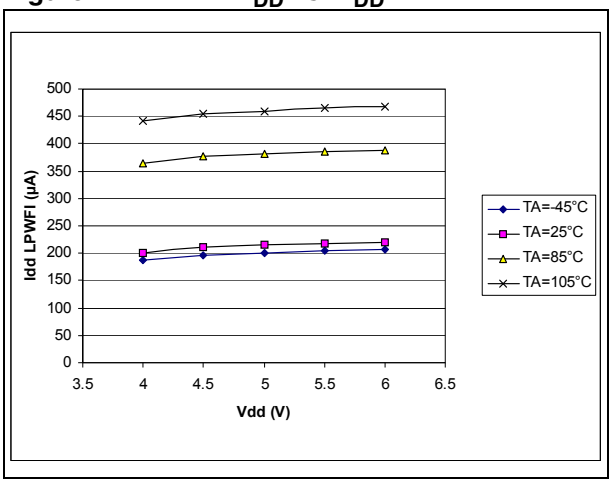


Figure 11. LPWFI I_{DD} vs. V_{DD}



Typical application current consumption

Table 11. Typical consumption in Run mode at 25°C and 85°C

Conditions		f_{MCLK} (MHz)	f_{ADC} (MHz)	Typical I_{DD} (mA)
V_{DD}= 5.5 V, RC oscillator off, PLL on, RTC enabled, 1 Timer (TIM) running, and ADC running in scan mode.	Code executing in RAM	10	10	20
		20		29
		36	9	42
	Code executing in Flash	10	10	22
		20		32
		36	9	48

Table 12. Typical consumption in Run and low power modes at 25°C

Mode	Conditions	f_{MCLK}	Typical I_{DD}
RUN	All peripherals on, RAM execution	36 MHz	76 mA
		24 MHz	56 mA
WFI	Main voltage regulator on, Flash on, EIC on, WIU on, GPIOs on.	36 MHz	33 mA
		24 MHz	31 mA
SLOW	PLL off, main voltage regulator on	4 MHz	11 mA
	CLOCK2/16, main voltage regulator on	250 kHz	8 mA
	CLOCK2/16, main voltage regulator off	250 kHz	3 mA
	RC oscillator running in low frequency, main crystal oscillator off, main voltage regulator off	29 kHz	2.5 mA
LPWFI	CLOCK2/16, main voltage regulator off, LP voltage regulator = 2 mA, Flash in power down mode.	250 kHz	528 µA
STOP	Main voltage regulator off, RTC on, RC oscillator off, LP voltage regulator = 6 mA	-	378 µA
	Main voltage regulator off, RTC off, RC oscillator off, LP voltage regulator = 6 mA	-	83 µA
	Main voltage regulator off, RTC off, RC oscillator off, LP voltage regulator = 4 mA	-	64 µA
	Main voltage regulator off, RTC off, RC oscillator off, LP voltage regulator = 2 mA	-	44 µA
HALT	RTC off, LP voltage regulator = 2 mA	-	44 µA

On-chip peripherals

Table 13. Peripheral current consumption at T_A= 25°C

Symbol	Parameter	Conditions	Typ	Unit
$I_{DD(RC)}$	RC (backup oscillator) supply current	High frequency	120	µA
		Low frequency	60	µA
$I_{DD(TIM)}$	TIM timer supply current [1]	f_{MCLK}=36 MHz	350	µA
$I_{DD(BSPI)}$	BSPI supply current [1]		1.1	mA
$I_{DD(UART)}$	UART supply current [1]		850	µA
$I_{DD(I2C)}$	I2C supply current [1]		430	µA
$I_{DD(ADC)}$	ADC supply current when converting [2]		5	mA
$I_{DD(EIC)}$	EIC supply current		2.88	mA
$I_{DD(CAN)}$	CAN supply current [1]		2.95	mA
$I_{DD(GPIO)}$	GPIO supply current		150	µA
$I_{DD(TB)}$	TB supply current		250	µA
$I_{DD(PWM)}$	PWM supply current		240	µA
$I_{DD(RTC)}$	RTC supply current		370	µA
$I_{DD(DMA)}$	DMA supply current		2.5	mA
$I_{DD(ARB)}$	Native arbiter supply current		180	µA
$I_{DD(AHB)}$	AHB arbiter supply current		570	µA
$I_{DD(WUT)}$	WUT supply current		300	µA
$I_{DD(WIU)}$	WIU supply current		460	µA

1. Data based on a differential I_{DD} measurement between the on-chip peripheral when kept under reset, not clocked and the on-chip peripheral when clocked and not kept under reset. This measurement does not include the pad toggling consumption.
2. Data based on a differential I_{DD} measurement between reset configuration and continuous A/D conversions.

Main oscillator characteristics

V_{DD} = 5 V ± 10%, T_A = -40° C to T_{Amax}, unless otherwise specified.

Table 14. Main oscillator characteristics

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
f_{OSC}	Oscillator frequency		4		8	MHz
g_m	Oscillator transconductance		1.5		4.2	mA/V
V_{OSC} 1)	Oscillation amplitude	f_{OSC} = 4 MHz, T_A= 25° C	-	2.4	-	V
		f_{OSC} = 8 MHz, T_A= 25° C		1.-		
V_{AV} 1)	Oscillator operating point	Sine wave middle, T_A= 25° C	-	0.77	-	v
t_{STUP} 1)	Oscillator start-up time	External crystal, V_{DD} = 5.5 V, f_{OSC} = 4 MHz, T_A=-40° C	-	-	12	ms
		External crystal, V_{DD} = 5.0 V, f_{OSC} = 4 MHz, T_A=25° C	-	5.5	-	ms
		External crystal, V_{DD} = 5.5 V, f_{OSC} = 6 MHz, T_A=-40° C	-	-	8	ms
		External crystal, V_{DD} = 5.0 V, f_{OSC} = 6 MHz, T_A=25° C	-	3.3	-	ms
		External crystal, V_{DD} = 5.5 V, f_{OSC} = 8 MHz, T_A=-40° C	-	-	7	ms
		External crystal, V_{DD} = 5.0 V, f_{OSC} = 8 MHz, T_A= 25° C	-	2.7	-	ms

Table 14. Main oscillator characteristics (continued)

Symbol	Parameter	Conditions		Value			Unit
				Min	Typ	Max	
R_F [1]	Feedback resistor	f_{OSC} = 4 MHz Cp[2] = 10 pF	C_1[3] = C_2 [4]= 10 pF	150	555	-	Ω
			$C_1 = C_2$ = 20 pF	490	1035	-	
			$C_1 = C_2$ = 30 pF	490	1030	-	
			$C_1 = C_2$ = 40 pF	380	850	-	
		f_{OSC} = 5 MHz Cp = 10 pF	$C_1 = C_2$ = 10 pF	160	470	-	
			$C_1 = C_2$ = 20 pF	415	800	-	
			$C_1 = C_2$ = 30 pF	340	735	-	
			$C_1 = C_2$ = 40 pF	260	580	-	
		f_{OSC} = 6 MHz Cp = 10 pF	$C_1 = C_2$ = 10 pF	160	415	-	
			$C_1 = C_2$ = 20 pF	325	640	-	
			$C_1 = C_2$ = 30 pF	250	550	-	
			$C_1 = C_2$ = 40 pF	180	420	-	
		f_{OSC} = 7 MHz Cp = 10 pF	$C_1 = C_2$ = 10 pF	160	375	-	
			$C_1 = C_2$ = 20 pF	260	525	-	
			$C_1 = C_2$ = 30 pF	185	420	-	
			$C_1 = C_2$ = 40 pF	135	315	-	
		f_{OSC} = 8 MHz Cp = 10 pF	$C_1 = C_2$ = 10 pF	155	340	-	
			$C_1 = C_2$ = 20 pF	210	435	-	
			$C_1 = C_2$ = 30 pF	145	335	-	
			$C_1 = C_2$ = 40 pF	100	245	-	

1. Min and max values are guaranteed by characterization, not tested in production.
2. C_P represents the total capacitance between XTAL1 and XTAL2, including the shunt capacitance of the external quartz crystal as well as the total board parasitic cross-capacitance between XTAL1 track and XTAL2 track.
3. C_1 represents the total capacitance between XTAL1 and ground, including the external capacitance tied to XTAL1 pin (C_L) as well as the total parasitic capacitance between XTAL1 track and ground (this includes application board track capacitance to ground and device pin capacitance).
4. C_2 represents the total capacitance between XTAL2 and ground, including the external capacitance tied to XTAL1 pin (C_L) as well as the total parasitic capacitance between XTAL2 track and ground (this includes application board track capacitance to ground and device pin capacitance).

PLL electrical characteristics

V_{DD} = 5 V ± 10%, T_A = -40° C to T_{Amax}, unless otherwise specified

Table 16. PLL characteristics

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
f_{PLLIN} (1)	PLL reference clock	FREF_RANGE = '0' FREF_RANGE = '1'	1.5 3.0		3.0 5.0	MHz
f_{PLLOUT}	PLL output clock	MX = "00" MX = "01" MX = "10" MX = "11"	20 x f_{PLLIN} 12 x f_{PLLIN} 28 x f_{PLLIN} 16 x f_{PLLIN}			MHz
f_{MCLK}	System clock	DX = 1..7	f_{PLLOUT}/DX		36	MHz
f_{FREE} (2)	PLL free running frequency	FREF_RANGE = '0', MX0 = '1' FREF_RANGE = '0', MX0 = '0' FREF_RANGE = '1', MX0 = '1' FREF_RANGE = '1', MX0 = '0'		120 240 240 480		kHz
t_{LOCK} (3)	PLL lock time	Stable oscillator (f_{PLLIN} = 4 MHz), stable V_{DD}		100	300	µs
Δt_{PKJIT}	PLL jitter (pk to pk)	f_{PLLIN} = 4 MHz (pulse generator)			1.5	ns

1. f_{PLLIN} is obtained from f_{OSC} directly or through an optional divider by 2.
2. Typical data are based on T_A=25°C, V_{DD}=5V
3. Max value is guaranteed by characterization, not tested in production.

Table 17. Low-power mode wake-up timing

Symbol	Parameter	Conditions	Typ	Unit
t_{WUHALT}	Wake-up from HALT mode		200	µs
t_{WUSTOP}	Wake-up from STOP mode	RC high frequency in STOP mode	180	µs
		RC low frequency in STOP mode	234	µs
$t_{WULPWFI}$ 1)	Wake-up from LPWFI mode	Main voltage regulator on RC oscillator off f_{OSC} = 4 MHz, f_{MCLK}= f_{OSC}/16 RAM or FLASH execution	27	µs
		Main voltage regulator on RC oscillator = high frequency Flash execution	46	µs
		Main voltage regulator on RC oscillator = low frequency Flash execution	3.6	ms

1. Flash memory programmed to enter Power Down mode during LPWFI.

Electromagnetic interference (EMI)

Based on a simple application running on the product (toggling 2 LEDs through the I/O ports), the product is monitored in terms of emission. This emission test is in line with the norm SAE J 1752/3 which specifies the board and the loading of each pin.

Table 20. EMI data

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{OSC4M}/f_{MCLK}]		Unit
				6/36 MHz	8/8 MHz	
S_{EMI}	Peak level	V_{DD}=5.0V, T_A=+25°C, All packages	0.1 MHz to 30 MHz	23	30	dBµV
			30 MHz to 130 MHz	37	34	
			130 MHz to 1 GHz	20	7	
			SAE EMI Level	4	3.5	-

Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU and DLU) using specific measurement methods, the product is stressed in order to determine its performance in terms of electrical sensitivity. For more details, refer to the application note AN1181.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts*(n+1) supply pin). Two models can be simulated: human body model and machine model. This test conforms to the JESD22-A114A/A115A standard.

Table 21. ESD Absolute Maximum ratings

Symbol	Ratings	Conditions	Maximum value [1]	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A=+25° C	2000	V
$V_{ESD(MM)}$	Electrostatic discharge voltage (machine model)		200	
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)		750 on corner pins, 500 on others	

Notes:

1. Data based on characterization results, not tested in production.

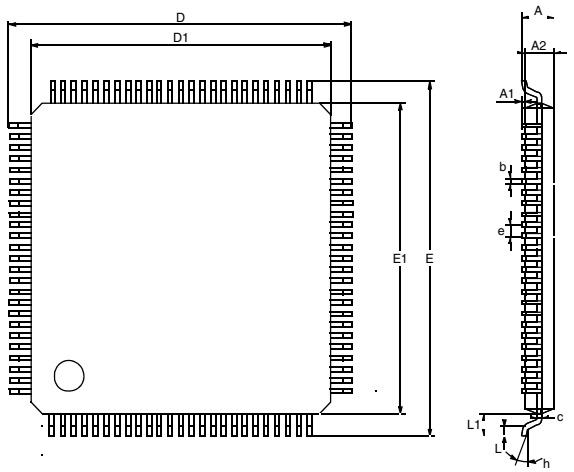
Static and dynamic latch-up

- **LU**: 3 complementary static tests are required on 10 parts to assess the latch-up performance. A supply overvoltage (applied to each power supply pin) and a current injection (applied to each input, output and configurable I/O pin) are performed on each

5 Package characteristics

5.1 Package mechanical data

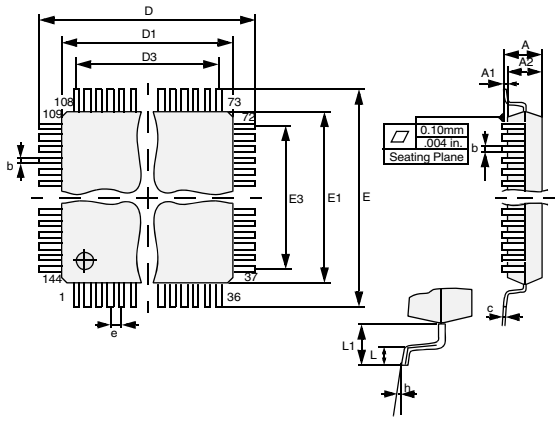
Figure 24. 100-pin thin quad flat package



Dim.	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A			1.60			0.0630
A1	0.05		0.15	0.0020		0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b	0.17	0.22	0.27	0.0067	0.0087	0.0106
C	0.09		0.20	0.0035		0.0079
D		16.00			0.6299	
D1		14.00			0.5512	
E		16.00			0.6299	
E1		14.00			0.5512	
e		0.50			0.0197	
h	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1		1.00			0.0394	
	Number of Pins					
N	100					

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 25. 144-pin thin quad flat package



Dim.	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A			1.60			0.0630
A1	0.05		0.15	0.0020		0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b	0.17	0.22	0.27	0.0067	0.0087	0.0106
c	0.09		0.20	0.0035		0.0079
D	21.80	22.00	22.20	0.8583	0.8661	0.8740
D1	19.80	20.00	20.20	0.7795	0.7874	0.7953
D3		17.50			0.6890	
E	21.80	22.00	22.20	0.8583	0.8661	0.8740
E1	19.80	20.00	20.20	0.7795	0.7874	0.7953
E3		17.50			0.6890	
e		0.50			0.0197	
K	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1		1.00			0.0394	
	Number of Pins					
N	144					

1. Values in inches are converted from mm and rounded to 4 decimal digits.

5.2 Thermal characteristics

The average chip-junction temperature, T_J, in degrees Celsius, may be calculated using the following equation:

$$T_J = T_A + (P_D \times \Theta_{JA}) \quad (1)$$

Where:

- T_A is the ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D is the sum of P_{INT} and $P_{I/O}$ ($P_D = P_{INT} + P_{I/O}$),
- P_{INT} is the product of I_{DD} and V_{DD}, expressed in Watts. This is the chip internal power,
- $P_{I/O}$ represents the power dissipation on input and output pins; user determined.

Most of the time for the applications $P_{I/O} < P_{INT}$ and may be neglected. On the other hand, $P_{I/O}$ may be significant if the device is configured to drive continuously external modules and/or memories.

An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is given by:

$$P_D = K / (T_J + 273°C) \quad (2)$$

Therefore (solving equations 1 and 2):

$$K = P_D \times (T_A + 273°C) + \Theta_{JA} \times P_D^2 \quad (3)$$

Where:

- K is a constant for the particular part, which may be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J may be obtained by solving equations (1) and (2) iteratively for any value of T_A

Table 28. Thermal characteristics

Symbol	Description	Package	Value (typical)	Unit
Θ_{JA}	Thermal resistance junction-ambient	LFBGA144	50	°C/W
		TQFP144	40	
		TQFP100	40	

7 Known limitations

7.1 Low power wait for interrupt mode

When the STR73x device is put in Low Power Wait For Interrupt mode (LPWFI), the Flash goes into low power mode or power down mode, depending on the setting of the PWD bit in the Flash Control Register 0 (default is '0', Low Power mode). This default mode can create excessive voltage conditions on the transistor gates and may affect the long term behavior of the Low Power mode circuitry.

Workaround

There is no workaround. If Low Power Wait For Interrupt mode is used, it is strongly suggested to configure the Flash to enter power down mode (bit PWD = '1').

7.2 PLL free running mode at high temperature

When the STR73x device is operated and an ambient temperature (T_A) of more than 55° C and the main system clock (f_{MCLK}) is sourced by the PLL in free running mode, the device may not work properly.

Workaround

At high temperature (more than 55° C), it is recommended to use the internal RC oscillator as a backup clock source rather than the PLL free running mode.

8 Revision history

Table 30. Document revision history

Date	Revision	Description of changes
19-Sep-2005	1	First release
02-Nov-2005	2	Removed Table 8 power consumption in LP modes Updated PLL frequency in *Section 1.1* and *Table 12*
08-Mar-2006	3	*Section 3.4: Preliminary power consumption data* updated *Section 3.5: DC electrical characteristics* updated *Section 7: Known limitations* added
04-Jun-2006	4	*Section 4: Electrical parameters* updated *Section 7: Known limitations* updated Added temperature range -40°C to 85°C in *Section 6: Order codes*
19-Jun-2006	5	Changed Flash data retention to 20 years at 85°C in *Table 18 on page 34*.
08-Sep-2006	6	Changed *Table 24: Output driving current on page 39* Added *Figure 14: VOL standard ports vs IOL @ VDD 5 V* thru *Figure 18: VOL P6.0 pin vs IOL @ VDD 5 V on page 40*. Added *Figure 20: NRSTIN RPU vs. VDD*
08-Jun-2008	7	Inch values rounded to 4 decimal digits in *Section 5.1: Package mechanical data* Modified BSPI speed in *Section 2.1: On-chip peripherals*

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