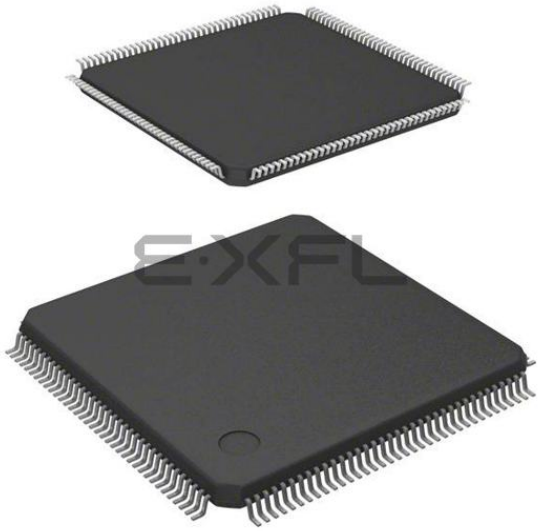

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM7®
Core Size	32-Bit Single-Core
Speed	36MHz
Connectivity	CANbus, I²C, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	112
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/str730fz1t6

1 Scope

This datasheet provides the STR73x ordering information, mechanical and electrical device characteristics.

For complete information on the STR73xF microcontroller memory, registers and peripherals. please refer to the STR73x reference manual.

For information on programming, erasing and protection of the internal Flash memory please refer to the STR7 Flash programming reference manual.

For information on the ARM7TDMI core please refer to the ARM7TDMI technical reference manual.

1.1 Description

ARM core with embedded Flash & RAM

STR73xF family combines the high performance ARM7TDMI™ CPU with an extensive range of peripheral functions and enhanced I/O capabilities. All devices have on-chip high-speed single voltage Flash memory and high-speed RAM. The STR73xF family has an embedded ARM core and is therefore compatible with all ARM tools and software.

Extensive tools support

STMicroelectronics' 32-bit, ARM core-based microcontrollers are supported by a complete range of high-end and low-cost development tools to meet the needs of application developers. This extensive line of hardware/software tools includes starter kits and complete development packages all tailored for ST's ARM core-based MCUs.

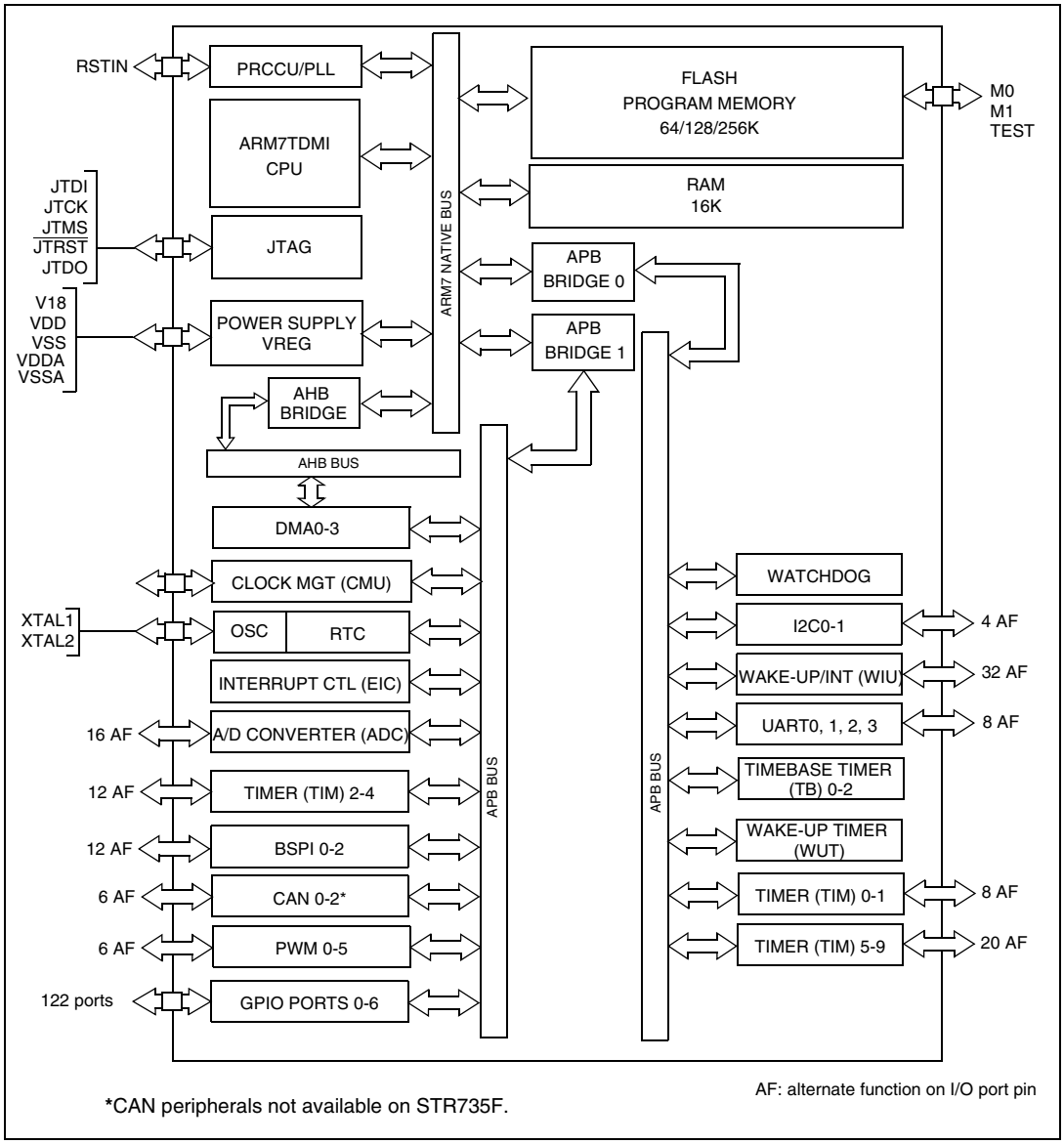
The range of development packages includes third-party solutions that come complete with a graphical development environment and an in-circuit emulator/programmer featuring a JTAG application interface. These support a range of embedded operating systems (OS), while several royalty-free OSs are also available.

For more information, please refer to ST MCU site http://www.st.com/mcu

Figure 1 shows the general block diagram of the device family.

3 Block diagram

Figure 1. STR730F/STR735F block diagram



3.2.2 STR730F/STR735F (LFBGA144)

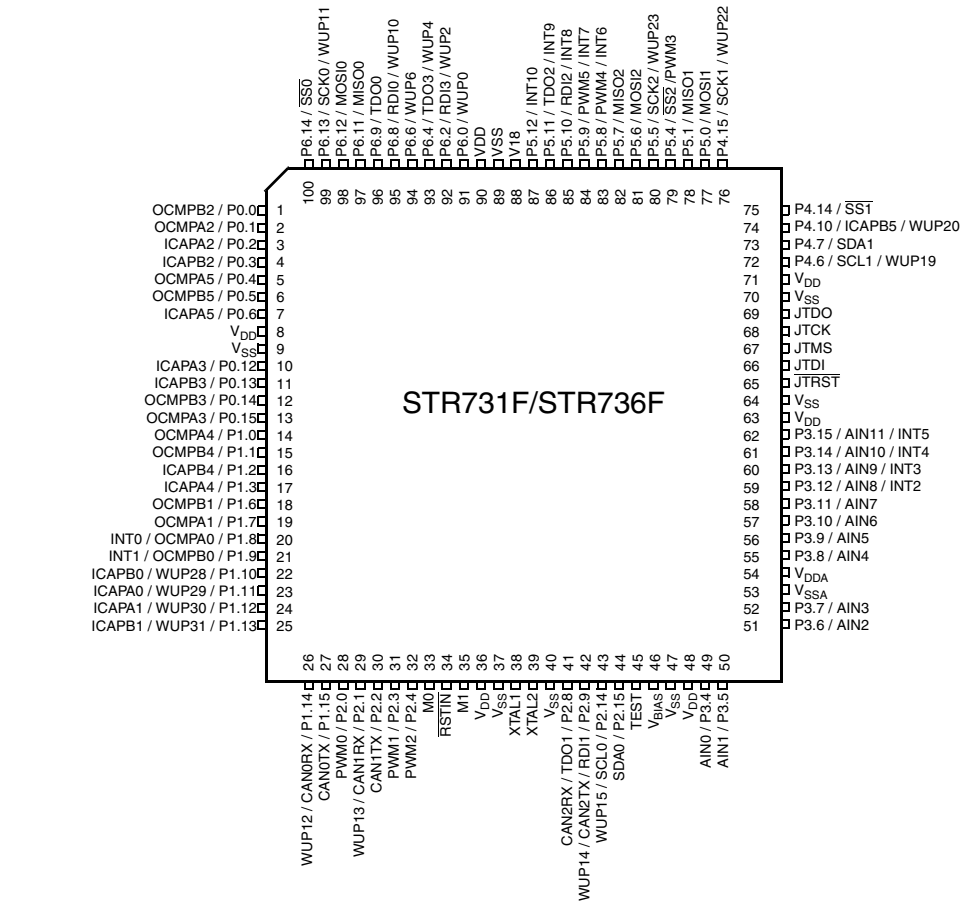
Table 3. STR730F/STR735F LFBGA ball connections

Ball	Name	Ball	Name	Ball	Name	Ball	Name
A1	P0.0 / OCMPB2	B1	P0.4 / OCMPA5	C1	P0.5 / OCMPB5	D1	V_{SS}
A2	P6.10 / WUP8	B2	P0.1 / OCMPA2	C2	P0.2 / ICAPA2	D2	V_{DD}
A3	P6.9 / TDO0	B3	P6.15 / WUP9	C3	P0.3 / ICAPB2	D3	P0.6 / ICAPA5
A4	P6.12 / MOSI0	B4	P6.13 / SCKO / WUP11	C4	P6.14 / SSO	D4	P0.7 /ICAPB5
A5	P6.6 / WUP6	B5	P6.7 / WUP7	C5	P6.8 / RDI0 / WUP10	D5	P6.11 / MISO0
A6	V_{18}	B6	P6.2 / WUP2 / RDI3	C6	P6.3 / WUP3	D6	P6.4 / WUP4 /TDO3
A7	P5.15 / INT13	B7	P5.14 / INT12	C7	V_{SS}	D7	VDD
A8	P5.8 / INT6	B8	P5.9 / INT7	C8	P5.10 / INT8 / RDI2	D8	P5.12 / INT10
A9	P5.2 / OCMPA9	B9	P5.3 / OCMPB9	C9	P5.4 / SS2	D9	P5.5 / SCK2 / WUP23
A10	P5.7 / MISO2	B10	P5.0 / MOSI1	C10	P5.1 / MISO1	D10	P4.13 / ICAPB9
A11	P5.6 / MOSI2	B11	P4.15 / SCK1 / WUP22	C11	P4.14 / SS1	D11	P4.12 / ICAPA9 / WUP21
A12	P5.11 / TDO2 / INT9	B12	P4.8 / OCMPA8	C12	P4.7 / SDA1	D12	P4.11 / OCMPB8
E1	P0.8 / OCMPA6	F1	V_{DD}	G1	V_{SS}	H1	V_{DD}
E2	P0.9 / OCMPB6	F2	P0.13 / ICAPB3	G2	P1.2 / ICAPB4	H2	P1.8 / OCMPA0 / INT0
E3	P0.10 / OCMPA7	F3	P0.14 / OCMPB3	G3	P1.3 / ICAPA4	H3	P1.9 / OCMPB0 / INT1
E4	P0.11 / OCMPB7	F4	P0.15 / OCMPA3	G4	V_{SS}	H4	P1.10 / ICAPB0 / WUP28
E5	P0.12 / ICAPA3	F5	P1.0 / OCMPA4	G5	P1.5	H5	XTAL2
E6	P6.5 / WUP5	F6	P1.1 / OCMPB4	G6	P2.11 / WUP17	H6	P2.10 / WUP16
E7	P6.0 / WUP0	F7	P6.1 / WUP1	G7	P4.0 / ICAPA7 / WUP24	H7	P2.15 / SDA 0
E8	P5.13 / INT11	F8	P4.4 / CAN2TX[1)]	G8	VDD	H8	JTMS
E9	P4.10 / ICAPA6 / WUP20	F9	P4.3 / ICAPB8 / WUP27	G9	VSS	H9	VSS
E10	P4.9 / ICAPB6	F10	P4.2 / ICAPA8 / WUP26	G10	JTDO	H10	VDD
E11	P4.6 / SCL1 / WUP19	F11	P4.1 / ICAPB7 / WUP25	G11	JTCK	H11	P3.15 / AIN15 / INT5
E12	P4.5 / WUP18 / CAN2RX[1)]	F12	JTDI	G12	nJTRST	H12	P3.14 / AIN14 / INT4
J1	P1.4	K1	P1.6 / OCMPB1	L1	P1.7 / OCMPA1	M1	P1.14 / CAN0RX[1)] / WUP12
J2	P1.11 / ICAPA0 / WUP29	K2	P1.13 / ICAPB1 / WUP31	L2	P1.15 / CAN0TX[1)]	M2	P2.4 / PWM2
J3	P1.12 / ICAPA1 / WUP30	K3	P2.1 / CAN1RX[1)] / WUP13	L3	P2.0 / PWM0	M3	P2.5 / PWM3
J4	P2.7 / PWM5	K4	P2.6 / PWM4	L4	P2.3 / PWM1	M4	P2.2 / CAN1TX[1)]
J5	V_{DD}	K5	M1	L5	RSTIN	M5	M0
J6	P2.9 / RDI1 / WUP14	K6	P2.8 / TDO1	L6	V_{SS}	M6	V_{SS}
J7	P2.14 / SCL 0 / WUP15	K7	P2.13 / INT15	L7	P2.12 / INT14	M7	XTAL1
J8	P3.1 / AIN1	K8	P3.0 / AIN0	L8	VBIAS	M8	TST
J9	P3.13 / AIN13 / INT3	K9	P3.4 / AIN4	L9	P3.3 / AIN3	M9	P3.2 / AIN2
J10	P3.12 / AIN12 / INT2	K10	V_{DDA}	L10	P3.5 / AIN5	M10	V_{SS}
J11	P3.9 / AIN9	K11	V_{SSA}	L11	P3.7 / AIN7	M11	V_{DD}
J12	P3.8 / AIN8	K12	P3.11 / AIN11	L12	P3.10 / AIN10	M12	P3.6 / AIN6

Note: CAN alternate functions not available on STR735F.

3.2.3 STR731F/STR736F (TQFP100)

Figure 4. STR731F/STR736F pin configuration (top view)



Note: CAN alternate functions not available on STR736F.

Table 4. STR73xF pin description

Pin n°			Pin name	Type	Input			Output			Main function (after reset)	Alternate function
TQFP144	LFBGA144	TQFP100			Input Level	pu/pd	interrupt	Capability	OD	PP		
19	F3	12	P0.14/OCMPB3	I/O	T_T			2mA	X	X	Port 0.14	TIM3: output compare B output
20	F4	13	P0.15/OCMPA3	I/O	T_T			2mA	X	X	Port 0.15	TIM3: output compare A output
21	F5	14	P1.0/OCMPA4	I/O	T_T			2mA	X	X	Port 1.0	TIM4: output compare A output
22	F6	15	P1.1/OCMPB4	I/O	T_T			2mA	X	X	Port 1.1	TIM4: output compare B output
23	G2	16	P1.2/ICAPB4	I/O	T_T			2mA	X	X	Port 1.2	TIM4: input capture B input
24	G3	17	P1.3/ICAPA4	I/O	T_T			2mA	X	X	Port 1.3	TIM4: input capture A input
25	G4		V_{SS}	S							Ground	
26	H1		V_{DD}	S							Supply voltage (5 V)	
27	J1		P1.4	I/O	T_T			2mA	X	X	Port 1.4	
28	G5		P1.5	I/O	T_T			2mA	X	X	Port 1.5	
29	K1	18	P1.6/OCMPB1	I/O	T_T			2mA	X	X	Port 1.6	TIM1: output compare B output
30	L1	19	P1.7/OCMPA1	I/O	T_T			2mA	X	X	Port 1.7	TIM1: output compare A output
31	H2	20	P1.8/OCMPA0	I/O	T_T		INT0	2mA	X	X	Port 1.8	TIM0: output compare A output
32	H3	21	P1.9/OCMPB0	I/O	T_T		INT1	2mA	X	X	Port 1.9	TIM0: output compare B output
33	H4	22	P1.10/ICAPB0	I/O	T_T		WUP28	2mA	X	X	Port 1.10	TIM0: input capture B input
34	J2	23	P1.11/ICAPA0	I/O	T_T		WUP29	2mA	X	X	Port 1.11	TIM0: input capture A input
35	J3	24	P1.12/ICAPA1	I/O	T_T		WUP30	2mA	X	X	Port 1.12	TIM1: input capture A input
36	K2	25	P1.13/ICAPB1	I/O	T_T		WUP31	2mA	X	X	Port 1.13	TIM1: input capture B input
37	M1	26	P1.14/CAN0RX	I/O	T_T		WUP12	2mA	X	X	Port 1.14	CAN0: receive data input
38	L2	27	P1.15/CAN0TX	I/O	T_T			2mA	X	X	Port 1.15	CAN0: transmit data output
39	L3	28	P2.0/PWM0	I/O	T_T			2mA	X	X	Port 2.0	PWM0: PWM output
40	K3	29	P2.1/CAN1RX	I/O	T_T		WUP13	2mA	X	X	Port 2.1	CAN1: receive data input
41	M4	30	P2.2/CAN1TX	I/O	T_T			2mA	X	X	Port 2.2	CAN1: transmit data output
42	L4	31	P2.3/PWM1	I/O	T_T			2mA	X	X	Port 2.3	PWM1: PWM output
43	M2	32	P2.4/PWM2	I/O	T_T			2mA	X	X	Port 2.4	PWM2: PWM output
44	M3		P2.5/PWM3	I/O	T_T			2mA	X	X	Port 2.5	PWM3: PWM output
45	K4		P2.6/PWM4	I/O	T_T			2mA	X	X	Port 2.6	PWM4: PWM output
46	J4		P2.7/PWM5	I/O	T_T			2mA	X	X	Port 2.7	PWM5: PWM output
47	M5	33	M0	I	T_T	pd					BOOT: mode selection 0 input	
48	L5	34	RSTIN	I	C_T	pu					Reset input	
49	K5	35	M1	I	T_T	pd					BOOT: mode selection 1 input	

Table 4. STR73xF pin description

Pin n°			Pin name	Type	Input			Output			Main function (after reset)	Alternate function
TQFP144	LFBGA144	TQFP100			Input Level	pu/pd	interrupt	Capability	OD	PP		
73	M12	51	P3.6/AIN6	I/O	T_T			2mA	X	X	Port 3.6	ADC: analog input 6 (AIN2 in TQFP100)
74	L11	52	P3.7/AIN7	I/O	T_T			2mA	X	X	Port 3.7	ADC: analog input 7 (AIN3 in TQFP100)
75	K11	53	V_{SSA}	S							Reference ground for A/D converter	
76	K10	54	V_{DDA}	S							Reference voltage for A/D converter	
77	J12	55	P3.8/AIN8	I/O	T_T			2mA	X	X	Port 3.8	ADC: analog input 8 (AIN4 in TQFP100)
78	J11	56	P3.9/AIN9	I/O	T_T			2mA	X	X	Port 3.9	ADC: analog input 9 (AIN5 in TQFP100)
79	L12	57	P3.10/AIN10	I/O	T_T			2mA	X	X	Port 3.10	ADC: analog input 10 (AIN6 in TQFP100)
80	K12	58	P3.11/AIN11	I/O	T_T			2mA	X	X	Port 3.11	ADC: analog input 11 (AIN7 in TQFP100)
81	J10	59	P3.12/AIN12	I/O	T_T		INT2	2mA	X	X	Port 3.12	ADC: analog input 12 (AIN8 in TQFP100)
82	J9	60	P3.13/AIN13	I/O	T_T		INT3	2mA	X	X	Port 3.13	ADC: analog input 13 (AIN9 in TQFP100)
83	H12	61	P3.14/AIN14	I/O	T_T		INT4	2mA	X	X	Port 3.14	ADC: analog input 14 (AIN10 in TQFP100)
84	H11	62	P3.15/AIN15	I/O	T_T		INT5	2mA	X	X	Port 3.15	ADC: analog input 15 (AIN11 in TQFP100)
85	H10	63	V_{DD}	S							Supply voltage (5 V)	
86	H9	64	V_{SS}	S							Ground	
87	G12	65	JTRST	I	T_T	pu						JTAG reset Input
88	F12	66	JTDI	I	T_T	pu						JTAG data input
89	H8	67	JTMS	I	T_T	pu						JTAG mode selection Input
90	G11	68	JTCK	I	T_T	pd						JTAG clock Input
91	G10	69	JTDO	O				4mA				JTAG data output. **Note:** Reset state = HiZ
92	G9	70	V_{SS}	S								Ground
93	G8	71	V_{DD}	S								Supply voltage (5 V)
94	G7		P4.0/ICAPA7	I/O	T_T		WUP24	2mA	X	X	Port 4.0	TIM7: input capture A input
95	F11		P4.1/ICAPB7	I/O	T_T		WUP25	2mA	X	X	Port 4.1	TIM7: input capture B input
96	F10		P4.2/ICAPA8	I/O	T_T		WUP26	2mA	X	X	Port 4.2	TIM8: input capture A input

Table 4. STR73xF pin description

Pin n°			Pin name	Type	Input			Output			Main function (after reset)	Alternate function
TQFP144	LFBGA144	TQFP100			Input Level	pu/pd	interrupt	Capability	OD	PP		
119	B8	84	P5.9/PWM5	I/O	T_T		INT7	2mA	X	X	Port 5.9	PWM5: PWM output (TQFP100 only)
120	C8	85	P5.10/RDI2	I/O	T_T		INT8	2mA	X	X	Port 5.10	UART2: receive data input
121	A12	86	P5.11/TDO2	I/O	T_T		INT9	2mA	X	X	Port 5.11	UART2: transmit data output
122	D8	87	P5.12	I/O	T_T		INT10	2mA	X	X	Port 5.12	
123	E8		P5.13	I/O	T_T		INT11	2mA	X	X	Port 5.13	
124	B7		P5.14	I/O	T_T		INT12	2mA	X	X	Port 5.14	
125	A7		P5.15	I/O	T_T		INT13	2mA	X	X	Port 5.15	
126	A6	88	V_{18}	S								1.8 V decoupling pin: a decoupling capacitor (recommended value: 100 nF) must be connected between this pin and nearest VSS pin.
127	C7	89	V_{SS}	S								Ground
128	D7	90	V_{DD}	S								Supply voltage (5 V)
129	E7	91	P6.0	I/O	T_T		WUP0	8mA	X	X	Port 6.0	
130	F7		P6.1	I/O	T_T		WUP1	2mA	X	X	Port 6.1	
131	B6	92	P6.2/RDI3	I/O	T_T		WUP2	2mA	X	X	Port 6.2	UART3: receive data input
132	C6		P6.3	I/O	T_T		WUP3	2mA	X	X	Port 6.3	
133	D6	93	P6.4/TDO3	I/O	T_T		WUP4	2mA	X	X	Port 6.4	UART3: transmit data output
134	E6		P6.5	I/O	T_T		WUP5	2mA	X	X	Port 6.5	
135	A5	94	P6.6	I/O	T_T		WUP6	2mA	X	X	Port 6.6	
136	B5		P6.7	I/O	T_T		WUP7	2mA	X	X	Port 6.7	
137	C5	95	P6.8/RDI0	I/O	T_T		WUP10	2mA	X	X	Port 6.8	UART0: receive data input
138	A3	96	P6.9/TDO0	I/O	T_T			2mA	X	X	Port 6.9	UART0: transmit data output
139	A2		P6.10	I/O	T_T		WUP8	2mA	X	X	Port 6.10	
140	D5	97	P6.11/MISO0	I/O	T_T			2mA	X	X	Port 6.11	BSPI0: master input/slave output
141	A4	98	P6.12/MOSI0	I/O	T_T			2mA	X	X	Port 6.12	BSPI0: master output/slave input
142	B4	99	P6.13/SCK0	I/O	T_T		WUP11	2mA	X	X	Port 6.13	BSPI0: serial clock
143	C4	100	P6.14/$\overline{SS}$0	I/O	T_T			2mA	X	X	Port 6.14	BSPI0: slave select
144	B3		P6.15	I/O	T_T		WUP9	2mA	X	X	Port 6.15	

4.2 Absolute maximum ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 5. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DD} - V_{SS}	External 5 V Supply voltage	-0.3	6.0	V
V_{SSA}	Reference ground for A/D converter	V_{SS}	V_{SS}	V
V_{DDA}- V_{SSA}	Reference voltage for A/D converter	-0.3	V_{DD}+0.3	V
V_{IN}	Input voltage on any pin	-0.3	V_{DD}+0.3	
$\lvert\Delta V_{DDx}\rvert$	Variations between different 5 V power pins	-	0.3	mV
$\lvert V_{SSX}$ - $V_{SS}\rvert$	Variations between all the different ground pins	-	0.3	
$V_{ESD(HBM)}$	Electrostatic discharge voltage (Human Body Model)	see *: Absolute maximum ratings (electrical sensitivity) on page 36*		
$V_{ESD(MM)}$	Electrostatic discharge voltage (Machine Model)			

Table 6. Current characteristics

Symbol	Ratings	Max.	Unit
I_{VDD}	Total current into V_{DD} power lines (source) 1)	100	mA
I_{VSS}	Total current out of V_{SS} ground lines (sink) 1)	100	
I_{IO}	Output current sunk by any I/O and control pin	10	
	Output current source by any I/O and control pin	10	
$I_{INJ(PIN)}$ 2) & 3)	Injected current on any other pin 4) &5)	±10	
$\Sigma I_{INJ(PIN)}$ 2)	Total injected current (sum of all I/O and control pins) 4)	±75	

1. All 5 V power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external 5 V supply
2. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$.
3. Negative injection disturbs the analog performance of the device. See note in *Section 4.3.6: 10-bit ADC characteristics on page 43*.
4. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values). These results are based on characterization with $\Sigma I_{INJ(PIN)}$ maximum current injection on four I/O port pins of the device.

5.) In 144-pin devices, only +10 mA on P0.3, P1.13, P3.6 and P4.13 pins (negative injection not allowed).

Figure 8. STOP I_{DD} vs. VDD

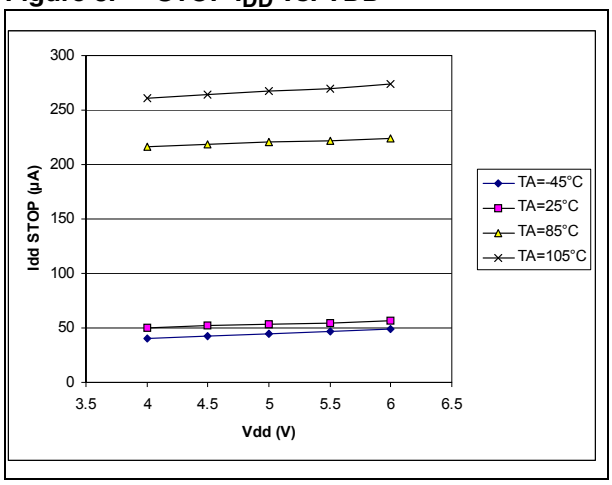


Figure 9. HALT I_{DD} vs. V_{DD}

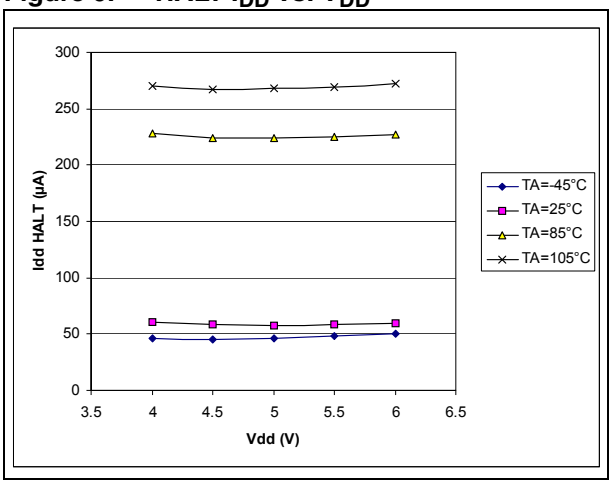


Figure 10. WFI I_{DD} vs. V_{DD}

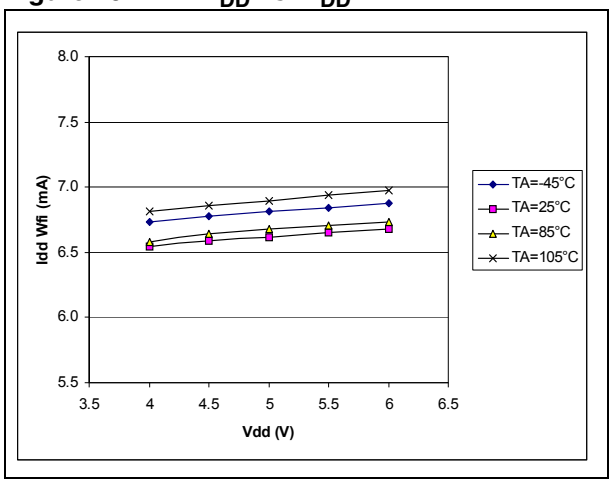
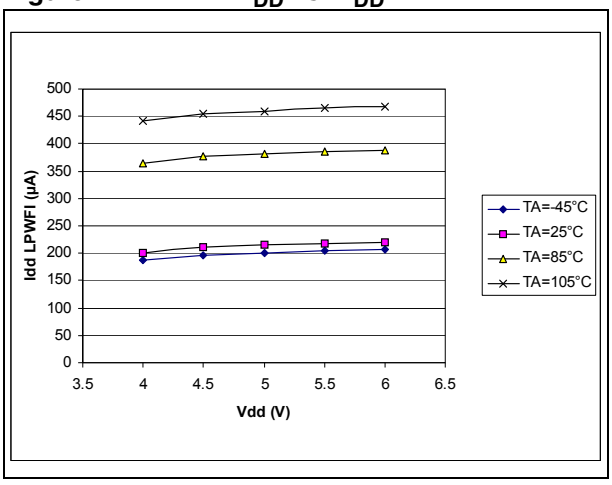


Figure 11. LPWFI I_{DD} vs. V_{DD}



On-chip peripherals

Table 13. Peripheral current consumption at T_A= 25°C

Symbol	Parameter	Conditions	Typ	Unit
$I_{DD(RC)}$	RC (backup oscillator) supply current	High frequency	120	µA
		Low frequency	60	µA
$I_{DD(TIM)}$	TIM timer supply current [1]	f_{MCLK}=36 MHz	350	µA
$I_{DD(BSPI)}$	BSPI supply current [1]		1.1	mA
$I_{DD(UART)}$	UART supply current [1]		850	µA
$I_{DD(I2C)}$	I2C supply current [1]		430	µA
$I_{DD(ADC)}$	ADC supply current when converting [2]		5	mA
$I_{DD(EIC)}$	EIC supply current		2.88	mA
$I_{DD(CAN)}$	CAN supply current [1]		2.95	mA
$I_{DD(GPIO)}$	GPIO supply current		150	µA
$I_{DD(TB)}$	TB supply current		250	µA
$I_{DD(PWM)}$	PWM supply current		240	µA
$I_{DD(RTC)}$	RTC supply current		370	µA
$I_{DD(DMA)}$	DMA supply current		2.5	mA
$I_{DD(ARB)}$	Native arbiter supply current		180	µA
$I_{DD(AHB)}$	AHB arbiter supply current		570	µA
$I_{DD(WUT)}$	WUT supply current		300	µA
$I_{DD(WIU)}$	WIU supply current		460	µA

1. Data based on a differential I_{DD} measurement between the on-chip peripheral when kept under reset, not clocked and the on-chip peripheral when clocked and not kept under reset. This measurement does not include the pad toggling consumption.
2. Data based on a differential I_{DD} measurement between reset configuration and continuous A/D conversions.

4.3.3 Memory characteristics

Flash memory

Table 18. Flash memory characteristics

Symbol	Parameter	Test Conditions	Value			Unit
			Min	Typ	Max[1)]	
t_{WP}	Word program (32-bit)			35	80	µs
t_{DWP}	Double word program(64-bit)			64	150	µs
t_{BP64}	Bank program (64 K)	Double word program		0.5	1.25	s
t_{BP128}	Bank program (128 K)	Double word program		1	2.5	s
t_{BP256}	Bank program (256 K)	Double word program		2	4.9	s
t_{SE8}	Sector erase (8 K)	Not preprogrammed Preprogrammed [2)]		0.6 0.5	0.9 0.8	s
t_{SE32}	Sector erase (32 K)	Not preprogrammed Preprogrammed[2)]		1.1 0.8	2 1.8	s
t_{SE64}	Sector erase (64 K)	Not preprogrammed preprogrammed [2)]		1.7 1.3	3.7 3.3	s
t_{RPD}[3)]	Recovery from power-down				20	µs
t_{PSL}[3)]	Program suspend latency				10	µs
t_{ESL}[3)]	Erase suspend latency				30	µs
t_{ESR}[3)]	Erase suspend rate	Min. time from erase resume to next erase suspend		20	20	ms
t_{SP}[3)]	Set protection			40	170	µs
t_{FPW}[3)]	First word program			1		ms
N_{END}	Endurance		10			kcycles
t_{RET}	Data retention	T_A = 85° C	20			Years

1. T_A = -45° C after 0 cycles, Guaranteed by characterization, not tested in production.
2. All bits programmed to 0.
3. Guaranteed by design, not tested in production.

sample. This test conforms to the EIA/JESD 78 IC latch-up standard. For more details, refer to the application note AN1181.

- **DLU**: Electrostatic discharges (one positive then one negative test) are applied to each pin of 3 samples when the micro is running to assess the latch-up performance in dynamic mode. Power supplies are set to the typical values, the oscillator is connected as near as possible to the pins of the micro and the component is put in reset mode. This test conforms to the IEC1000-4-2 and SAEJ1752/3 standards. For more details, refer to the application note AN1181.

Table 22. Electrical sensitivities

Symbol	Parameter	Conditions	Class [1]
LU	Static latch-up class	T_A=+25°C T_A=+85°C T_A=+105°C	A A A
DLU	Dynamic latch-up class	V_{DD}= 5.5 V, f_{OSC4M} = 4 MHz, f_{MCLK} = 32 MHz, T_A = +25° C	A

1. Class description: A Class is an STMicroelectronics internal specification. All its limits are higher than the JEDEC specifications, that means when a device belongs to Class A it exceeds the JEDEC standard. B Class strictly covers all the JEDEC criteria (international standard).

4.3.5 I/O port pin characteristics

General characteristics

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified.

Table 23. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Input low level voltage [1]	TTL ports			0.8	V
V_{IH}	Input high level voltage [1]		2.0			
$I_{INJ(PIN)}$	Injected current on any I/O pin				±10	mA
$\Sigma I_{INJ(PIN)}$ [2]	Total injected current (sum of all I/O and control pins)				±75	mA
I_{lkg}	Input leakage current [3]	$V_{SS} \leq V_{IN} \leq V_{DD}$			±1	µA
I_S	Static current consumption [4]	Floating input mode		200		µA
R_{PU}	Weak pull-up equivalent resistor[5]	$V_{IN}=V_{SS}$	55	120	220	kΩ
R_{PD}	Weak pull-down equivalent resistor[5]	$V_{IN}=V_{DD}$	55	120	220	kΩ
C_{IO}	I/O pin capacitance			5		pF

1. Data based on characterization results, not tested in production.
2. When the current limitation is not possible, the V_{IN} absolute maximum rating must be respected, otherwise refer to $I_{INJ(PIN)}$ specification. A positive injection is induced by $V_{IN}>V_{33}$ while a negative injection is induced by $V_{IN}<V_{SS}$. Refer to *Section 4.2 on page 22* for more details.
3. Leakage could be higher than max. if negative current is injected on adjacent pins.
4. Configuration not recommended, all unused pins must be kept at a fixed voltage: using the output mode of the I/O for example or an external pull-up or pull-down resistor. Data based on design simulation and/or technology characteristics, not tested in production.
6. The R_{PU} pull-up and R_{PD} pull-down equivalent resistor are based on a resistive transistor (corresponding I_{PU} and I_{PD} current characteristics described in *Figure 19*).

Output driving current

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified.

Table 24. Output driving current

I/O Type	Symbol	Parameter	Conditions	Min	Max	Unit
Standard	V_{OL} 1)	Output low level voltage for an I/O pin when 8 pins are sunk at same time	I_{IO}=+2 mA		0.4	V
	V_{OH} 2)	Output high level voltage for an I/O pin when 4 pins are sourced at same time	I_{IO}=-2 mA	V_{DD}-0.8		
Med. Current (JTDO)	V_{OL} 1)	Output low level voltage for an I/O pin	I_{IO}=+6 mA		0.4	
	V_{OH} 2)	Output high level voltage for an I/O pin	I_{IO}=-6 mA	V_{DD}-0.8		
High Current P6.0	V_{OL} 1)	Output low level voltage for an I/O pin	I_{IO}=+8 mA		0.4	
	V_{OH} 2)	Output high level voltage for an I/O pin	I_{IO}=-8 mA	V_{DD}-0.8		

1. The I_{IO} current sunk must always respect the absolute maximum rating specified in *Table 6* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
2. The I_{IO} current sourced must always respect the absolute maximum rating specified in *Table 6* and the sum of I_{IO} (I/O ports and control pins) must not exceed IV_{DD}.

Figure 13. V_{OH} standard ports vs I_{OH} @ V_{DD} 5V T_A -45° C

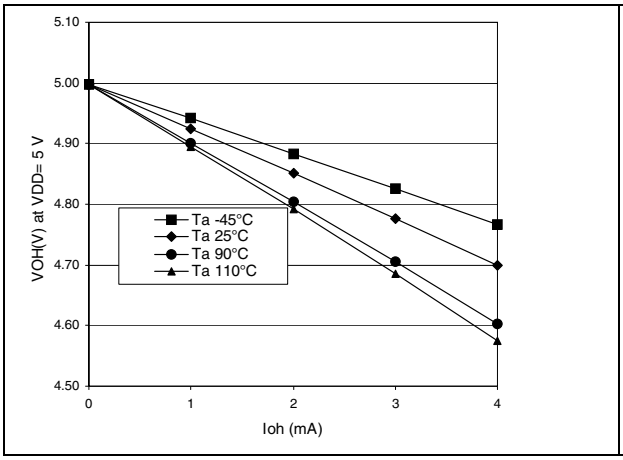


Figure 14. V_{OL} standard ports vs I_{OL} @ V_{DD} 5 V

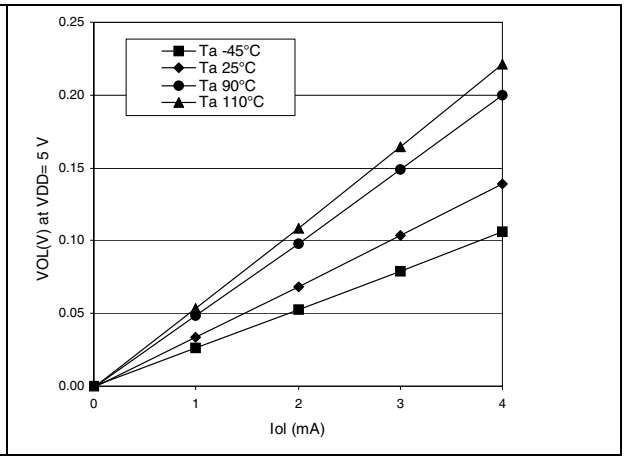


Figure 15. V_{OH} JTDO pin vs I_{OL} @ V_{DD} 5 V

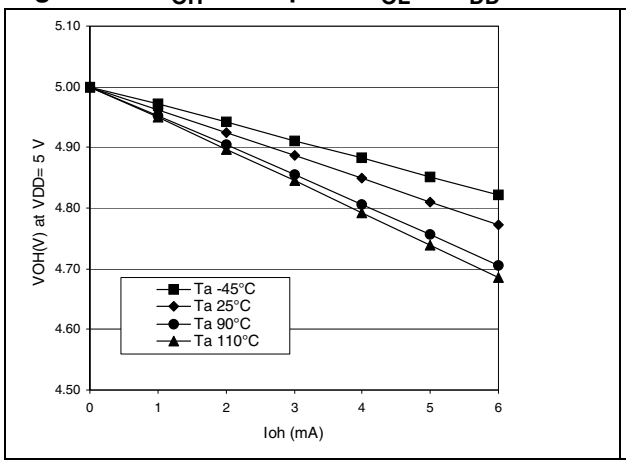


Figure 16. V_{OL} JTDO pin vs I_{OL} @ V_{DD} 5 V

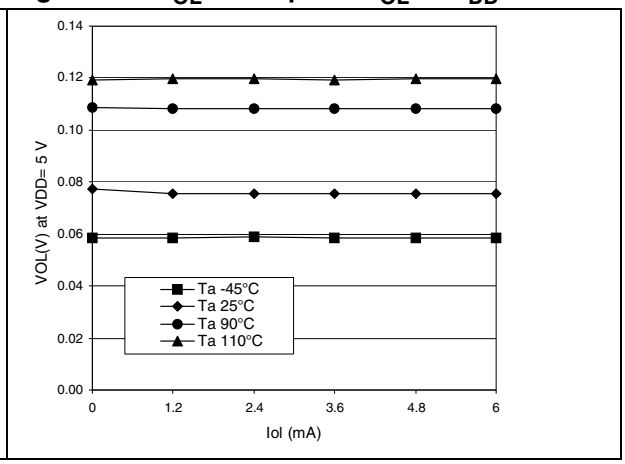


Figure 17. V_{OH} P6.0 pin vs I_{OL} @ V_{DD} 5 V

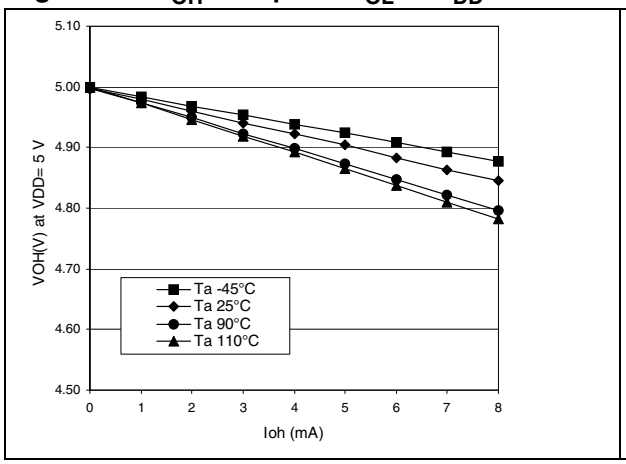


Figure 18. V_{OL} P6.0 pin vs I_{OL} @ V_{DD} 5 V

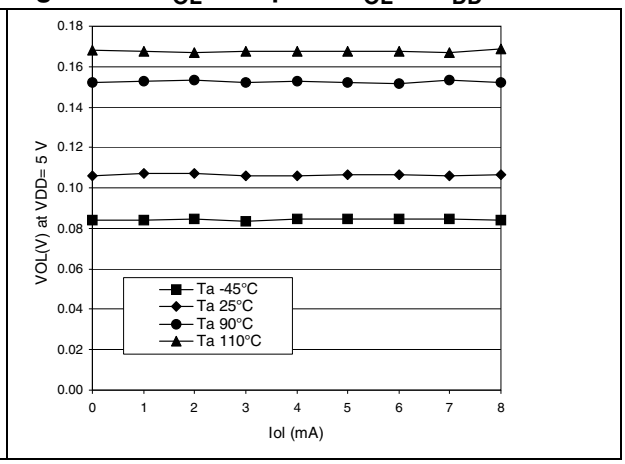


Table 27. ADC accuracy with f_{MCLK} = 20 MHz, f_{ADC}=10 MHz, R_{AIN} < 10 kΩ RAIN, V_{DDA}=5 V. This assumes that the ADC is calibrated[2)]

Symbol	Parameter	Conditions	Typ	Max	Unit
$\|E_T\|$	Total unadjusted error [1)]		1.0	2.0	LSB
$\|E_O\|$	Offset error [1)]		0.15	1.0	
$\|E_G\|$	Gain error [1)]		0.97	1.1	
$\|E_D\|$	Differential linearity error[1)]		0.7	1.0	
$\|E_L\|$	Integral linearity error [1)]		0.76	1.5	

1. ADC accuracy vs. negative injection current: Injecting negative current on any of the standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current. The effect of negative injection current on robust pins is specified in *Section 4.3.5*.
   Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 4.3.5* does not affect the ADC accuracy.
2. Calibration is needed once after each power-up.

Figure 21. ADC accuracy characteristics

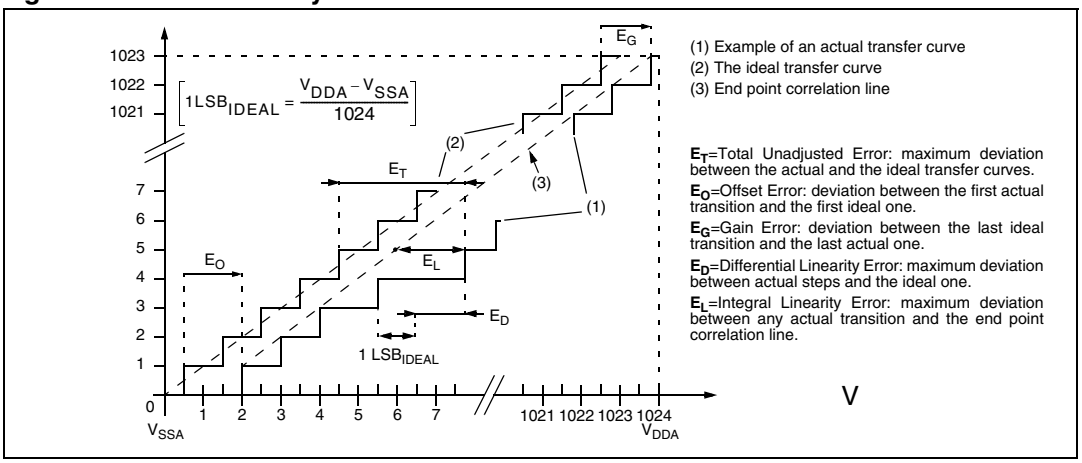
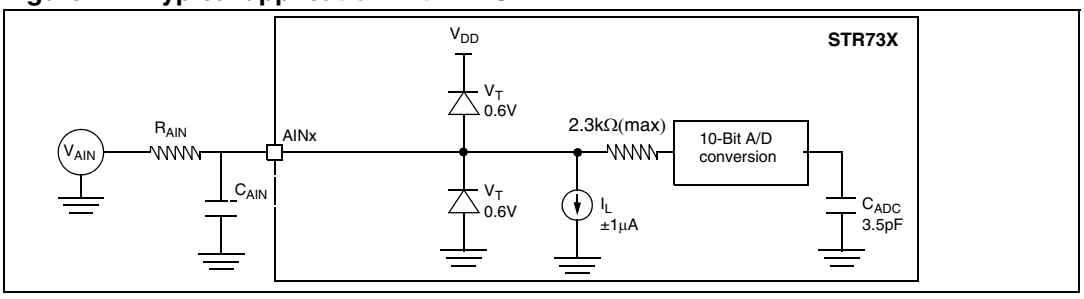


Figure 22. Typical application with ADC



5.2 Thermal characteristics

The average chip-junction temperature, T_J, in degrees Celsius, may be calculated using the following equation:

$$T_J = T_A + (P_D \times \Theta_{JA}) \quad (1)$$

Where:

- T_A is the ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D is the sum of P_{INT} and $P_{I/O}$ ($P_D = P_{INT} + P_{I/O}$),
- P_{INT} is the product of I_{DD} and V_{DD}, expressed in Watts. This is the chip internal power,
- $P_{I/O}$ represents the power dissipation on input and output pins; user determined.

Most of the time for the applications $P_{I/O} < P_{INT}$ and may be neglected. On the other hand, $P_{I/O}$ may be significant if the device is configured to drive continuously external modules and/or memories.

An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is given by:

$$P_D = K / (T_J + 273°C) \quad (2)$$

Therefore (solving equations 1 and 2):

$$K = P_D \times (T_A + 273°C) + \Theta_{JA} \times P_D^2 \quad (3)$$

Where:

- K is a constant for the particular part, which may be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J may be obtained by solving equations (1) and (2) iteratively for any value of T_A

Table 28. Thermal characteristics

Symbol	Description	Package	Value (typical)	Unit
Θ_{JA}	Thermal resistance junction-ambient	LFBGA144	50	°C/W
		TQFP144	40	
		TQFP100	40	

7 Known limitations

7.1 Low power wait for interrupt mode

When the STR73x device is put in Low Power Wait For Interrupt mode (LPWFI), the Flash goes into low power mode or power down mode, depending on the setting of the PWD bit in the Flash Control Register 0 (default is '0', Low Power mode). This default mode can create excessive voltage conditions on the transistor gates and may affect the long term behavior of the Low Power mode circuitry.

Workaround

There is no workaround. If Low Power Wait For Interrupt mode is used, it is strongly suggested to configure the Flash to enter power down mode (bit PWD = '1').

7.2 PLL free running mode at high temperature

When the STR73x device is operated and an ambient temperature (T_A) of more than 55° C and the main system clock (f_{MCLK}) is sourced by the PLL in free running mode, the device may not work properly.

Workaround

At high temperature (more than 55° C), it is recommended to use the internal RC oscillator as a backup clock source rather than the PLL free running mode.

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