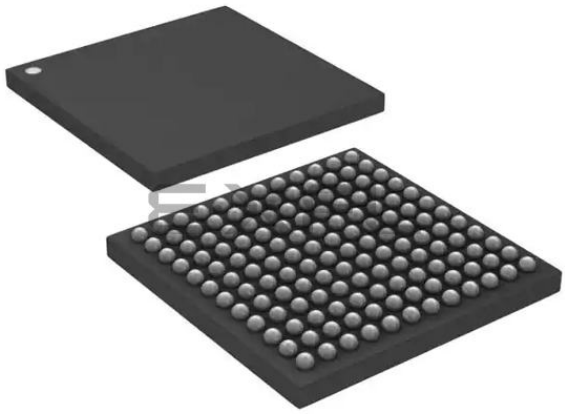

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM7®
Core Size	32-Bit Single-Core
Speed	36MHz
Connectivity	CANbus, I²C, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	112
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LFBGA
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/str730fz2h7

2 Overview

Table 2. Product overview

Features	STR730FZx		STR735FZx		STR731FVx			STR736FVx		
Flash memory - bytes	128K	256K	128K	256K	64K	128K	256K	64K	128K	256K
RAM - bytes	16 K				16 K					
Peripheral functions	10 TIM timers, 112 I/Os, 32 wake-up lines, 16 ADC				6 TIM timers, 72 I/Os, 18 wake-up lines, 12 ADC channels					
CAN peripherals	3		0		3			0		
Operating voltage	4.5 to 5.5 V									
Operating temperature	-40 to +85°C/-40 to +105° C									
Packages	**T**=TQFP144 20 x 20 **H**=LFBGA144 10 x10				**T**=TQFP100 14x14					

Package choice: reduced pin-count TQFP100 or feature-rich 144-pin TQFP or LFBGA

The STR73xF family is available in 3 packages. The TQFP144 and LFBGA144 versions have the full set of all features. The 100-pin version has fewer timers, I/Os and ADC channels. Refer to the Device Summary on Page 1 for a comparison of the I/Os available on each package.

The family includes versions with and without CAN.

High speed Flash memory

The Flash program memory is organized in 32-bit wide memory cells which can be used for storing both code and data constants. It is accessed by CPU with zero wait states @ 36 MHz.

The STR7 embedded Flash memory can be programmed using in-circuit programming or in-application programming.

The Flash memory endurance is 10K write/erase cycles and the data retention is 20 years @ 85° C.

IAP (in-application programming): IAP is the ability to re-program the Flash memory of a microcontroller while the user program is running.

ICP (in-circuit programming): ICP is the ability to program the Flash memory of a microcontroller using JTAG protocol while the device is mounted on the user application board.

The Flash memory can be protected against different types of unwanted access (read/write/erase). There are two types of protection:

- Sector write protection
- Flash debug protection (locks JTAG access)

Flexible power management

To minimize power consumption, you can program the STR73xF to switch to SLOW, WFI LPWFI, STOP or HALT modes depending on the current system activity in the application.

3.1 Related documentation

Available from www.arm.com:

ARM7TDMI technical reference manual

Available from http://www.st.com:

STR73x reference manual (RM0001)

STR7 Flash programming reference manual

STR73x software library user manual

For a list of related application notes refer to http://www.st.com.

3.2.2 STR730F/STR735F (LFBGA144)

Table 3. STR730F/STR735F LFBGA ball connections

Ball	Name	Ball	Name	Ball	Name	Ball	Name
A1	P0.0 / OCMPB2	B1	P0.4 / OCMPA5	C1	P0.5 / OCMPB5	D1	V_{SS}
A2	P6.10 / WUP8	B2	P0.1 / OCMPA2	C2	P0.2 / ICAPA2	D2	V_{DD}
A3	P6.9 / TDO0	B3	P6.15 / WUP9	C3	P0.3 / ICAPB2	D3	P0.6 / ICAPA5
A4	P6.12 / MOSI0	B4	P6.13 / SCKO / WUP11	C4	P6.14 / SSO	D4	P0.7 /ICAPB5
A5	P6.6 / WUP6	B5	P6.7 / WUP7	C5	P6.8 / RDI0 / WUP10	D5	P6.11 / MISO0
A6	V_{18}	B6	P6.2 / WUP2 / RDI3	C6	P6.3 / WUP3	D6	P6.4 / WUP4 /TDO3
A7	P5.15 / INT13	B7	P5.14 / INT12	C7	V_{SS}	D7	VDD
A8	P5.8 / INT6	B8	P5.9 / INT7	C8	P5.10 / INT8 / RDI2	D8	P5.12 / INT10
A9	P5.2 / OCMPA9	B9	P5.3 / OCMPB9	C9	P5.4 / SS2	D9	P5.5 / SCK2 / WUP23
A10	P5.7 / MISO2	B10	P5.0 / MOSI1	C10	P5.1 / MISO1	D10	P4.13 / ICAPB9
A11	P5.6 / MOSI2	B11	P4.15 / SCK1 / WUP22	C11	P4.14 / SS1	D11	P4.12 / ICAPA9 / WUP21
A12	P5.11 / TDO2 / INT9	B12	P4.8 / OCMPA8	C12	P4.7 / SDA1	D12	P4.11 / OCMPB8
E1	P0.8 / OCMPA6	F1	V_{DD}	G1	V_{SS}	H1	V_{DD}
E2	P0.9 / OCMPB6	F2	P0.13 / ICAPB3	G2	P1.2 / ICAPB4	H2	P1.8 / OCMPA0 / INT0
E3	P0.10 / OCMPA7	F3	P0.14 / OCMPB3	G3	P1.3 / ICAPA4	H3	P1.9 / OCMPB0 / INT1
E4	P0.11 / OCMPB7	F4	P0.15 / OCMPA3	G4	V_{SS}	H4	P1.10 / ICAPB0 / WUP28
E5	P0.12 / ICAPA3	F5	P1.0 / OCMPA4	G5	P1.5	H5	XTAL2
E6	P6.5 / WUP5	F6	P1.1 / OCMPB4	G6	P2.11 / WUP17	H6	P2.10 / WUP16
E7	P6.0 / WUP0	F7	P6.1 / WUP1	G7	P4.0 / ICAPA7 / WUP24	H7	P2.15 / SDA 0
E8	P5.13 / INT11	F8	P4.4 / CAN2TX[1)]	G8	VDD	H8	JTMS
E9	P4.10 / ICAPA6 / WUP20	F9	P4.3 / ICAPB8 / WUP27	G9	VSS	H9	VSS
E10	P4.9 / ICAPB6	F10	P4.2 / ICAPA8 / WUP26	G10	JTDO	H10	VDD
E11	P4.6 / SCL1 / WUP19	F11	P4.1 / ICAPB7 / WUP25	G11	JTCK	H11	P3.15 / AIN15 / INT5
E12	P4.5 / WUP18 / CAN2RX[1)]	F12	JTDI	G12	nJTRST	H12	P3.14 / AIN14 / INT4
J1	P1.4	K1	P1.6 / OCMPB1	L1	P1.7 / OCMPA1	M1	P1.14 / CAN0RX[1)] / WUP12
J2	P1.11 / ICAPA0 / WUP29	K2	P1.13 / ICAPB1 / WUP31	L2	P1.15 / CAN0TX[1)]	M2	P2.4 / PWM2
J3	P1.12 / ICAPA1 / WUP30	K3	P2.1 / CAN1RX[1)] / WUP13	L3	P2.0 / PWM0	M3	P2.5 / PWM3
J4	P2.7 / PWM5	K4	P2.6 / PWM4	L4	P2.3 / PWM1	M4	P2.2 / CAN1TX[1)]
J5	V_{DD}	K5	M1	L5	RSTIN	M5	M0
J6	P2.9 / RDI1 / WUP14	K6	P2.8 / TDO1	L6	V_{SS}	M6	V_{SS}
J7	P2.14 / SCL 0 / WUP15	K7	P2.13 / INT15	L7	P2.12 / INT14	M7	XTAL1
J8	P3.1 / AIN1	K8	P3.0 / AIN0	L8	VBIAS	M8	TST
J9	P3.13 / AIN13 / INT3	K9	P3.4 / AIN4	L9	P3.3 / AIN3	M9	P3.2 / AIN2
J10	P3.12 / AIN12 / INT2	K10	V_{DDA}	L10	P3.5 / AIN5	M10	V_{SS}
J11	P3.9 / AIN9	K11	V_{SSA}	L11	P3.7 / AIN7	M11	V_{DD}
J12	P3.8 / AIN8	K12	P3.11 / AIN11	L12	P3.10 / AIN10	M12	P3.6 / AIN6

Note: CAN alternate functions not available on STR735F.

Legend / Abbreviations for *Table 4*:

Type: I = input, O = output, S = supply, HiZ= high impedance,

In/Output level: T_T= TTL 0.8 V / 2 V with input trigger
C_T= CMOS $0.3V_{DD}/0.7V_{DD}$ with input trigger

Port and control configuration:

Input: pu/pd = with internal 100 kΩ weak pull-up or pull down

Output: OD = open drain (logic level)
PP = push-pull

Interrupts:

INTx = external interrupt line

WUPx = wake-up interrupt line

The reset state (during and just after the reset) of the I/O ports is input floating (Input tristate TTL mode). To avoid excess power consumption, unused I/O ports must be tied to ground.

Table 4. STR73xF pin description

Pin n°			Pin name	Type	Input			Output			Main function (after reset)	Alternate function
TQFP144	LFBGA144	TQFP100			Input Level	pu/pd	interrupt	Capability	OD	PP		
1	A1	1	P0.0/OCMPB2	I/O	T_T			2mA	X	X	Port 0.0	TIM2: output compare B output
2	B2	2	P0.1/OCMPA2	I/O	T_T			2mA	X	X	Port 0.1	TIM2: output compare A output
3	C2	3	P0.2/ICAPA2	I/O	T_T			2mA	X	X	Port 0.2	TIM2: input capture A input
4	C3	4	P0.3/ICAPB2	I/O	T_T			2mA	X	X	Port 0.3	TIM2: input capture B input
5	D1		V_{SS}	S							Ground	
6	D2		V_{DD}	S							Supply voltage (5 V)	
7	B1	5	P0.4/OCMPA5	I/O	T_T			2mA	X	X	Port 0.4	TIM5: output compare A output
8	C1	6	P0.5/OCMPB5	I/O	T_T			2mA	X	X	Port 0.5	TIM5: output compare B output
9	D3	7	P0.6/ICAPA5	I/O	T_T			2mA	X	X	Port 0.6	TIM5: input capture A input
10	D4		P0.7/ICAPB5	I/O	T_T			2mA	X	X	Port 0.7	TIM5: input capture B input
11	E1		P0.8/OCMPA6	I/O	T_T			2mA	X	X	Port 0.8	TIM6: output compare A output
12	E2		P0.9/OCMPB6	I/O	T_T			2mA	X	X	Port 0.9	TIM6: output compare B output
13	E3		P0.10/OCMPA7	I/O	T_T			2mA	X	X	Port 0.10	TIM7: output compare A output
14	E4		P0.11/OCMPB 7	I/O	T_T			2mA	X	X	Port 0.11	TIM7: output compare B output
15	F1	8	V_{DD}	S							Supply voltage (5 V)	
16	G1	9	V_{SS}	S							Ground	
17	E5	10	P0.12/ICAPA3	I/O	T_T			2mA	X	X	Port 0.12	TIM3: input capture A input
18	F2	11	P0.13/ICAPB3	I/O	T_T			2mA	X	X	Port 0.13	TIM3: input capture B input

Table 4. STR73xF pin description

Pin n°			Pin name	Type	Input			Output			Main function (after reset)	Alternate function	
TQFP144	LFBGA144	TQFP100			Input Level	pu/pd	interrupt	Capability	OD	PP			
50	J5	36	V_{DD}	S							Supply voltage (5 V)		
51	M6	37	V_{SS}	S							Ground		
52	M7	38	XTAL1	I							Oscillator amplifier circuit input and internal clock generator input.		
53	H5	39	XTAL2	O							Oscillator amplifier circuit output.		
54	L6	40	V_{SS}	S							Ground		
55	K6	41	P2.8/TDO1/CAN2RX	I/O	T_T			2mA	X	X	Port 2.8	UART1: transmit data output	CAN2: receive data input (TQFP100 only)
56	J6	42	P2.9/RDI1/CAN2TX	I/O	T_T		WUP14	2mA	X	X	Port 2.9	UART1: receive data input	CAN2: transmit data output (TQFP100 only)
57	H6		P2.10	I/O	T_T		WUP16	2mA	X	X	Port 2.10		
58	G6		P2.11	I/O	T_T		WUP17	2mA	X	X	Port 2.11		
59	L7		P2.12	I/O	T_T		INT14	2mA	X	X	Port 2.12		
60	K7		P2.13	I/O	T_T		INT15	2mA	X	X	Port 2.13		
61	J7	43	P2.14/SCL0	I/O	T_T		WUP15	2mA	X	X	Port 2.14	I2C0: serial clock	
62	H7	44	P2.15/SDA0	I/O	T_T			2mA	X	X	Port 2.15	I2C0: serial data	
63	M8	45	Test	I		pd					Reserved pin. Must be tied to ground		
64	L8	46	V_{BIAS}	S							Internal RC oscillator bias. A 1.3 MΩ external resistor has to be connected to this pin when a 32 kHZ RC oscillator frequency is used.		
65	M10	47	V_{SS}	S							Ground		
66	M11	48	V_{DD}	S							Supply voltage (5 V)		
67	K8		P3.0/AIN0	I/O	T_T			2mA	X	X	Port 3.0	ADC: analog input 0	
68	J8		P3.1/AIN1	I/O	T_T			2mA	X	X	Port 3.1	ADC: analog input 1	
69	M9		P3.2/AIN2	I/O	T_T			2mA	X	X	Port 3.2	ADC: analog input 2	
70	L9		P3.3/AIN3	I/O	T_T			2mA	X	X	Port 3.3	ADC: analog input 3	
71	K9	49	P3.4/AIN4	I/O	T_T			2mA	X	X	Port 3.4	ADC: analog input 4 (AIN0 in TQFP100)	
72	L10	50	P3.5/AIN5	I/O	T_T			2mA	X	X	Port 3.5	ADC: Analog input 5 (AIN1 in TQFP100)	

Table 4. STR73xF pin description

Pin n°			Pin name	Type	Input			Output			Main function (after reset)	Alternate function
TQFP144	LFBGA144	TQFP100			Input Level	pu/pd	interrupt	Capability	OD	PP		
73	M12	51	P3.6/AIN6	I/O	T_T			2mA	X	X	Port 3.6	ADC: analog input 6 (AIN2 in TQFP100)
74	L11	52	P3.7/AIN7	I/O	T_T			2mA	X	X	Port 3.7	ADC: analog input 7 (AIN3 in TQFP100)
75	K11	53	V_{SSA}	S							Reference ground for A/D converter	
76	K10	54	V_{DDA}	S							Reference voltage for A/D converter	
77	J12	55	P3.8/AIN8	I/O	T_T			2mA	X	X	Port 3.8	ADC: analog input 8 (AIN4 in TQFP100)
78	J11	56	P3.9/AIN9	I/O	T_T			2mA	X	X	Port 3.9	ADC: analog input 9 (AIN5 in TQFP100)
79	L12	57	P3.10/AIN10	I/O	T_T			2mA	X	X	Port 3.10	ADC: analog input 10 (AIN6 in TQFP100)
80	K12	58	P3.11/AIN11	I/O	T_T			2mA	X	X	Port 3.11	ADC: analog input 11 (AIN7 in TQFP100)
81	J10	59	P3.12/AIN12	I/O	T_T		INT2	2mA	X	X	Port 3.12	ADC: analog input 12 (AIN8 in TQFP100)
82	J9	60	P3.13/AIN13	I/O	T_T		INT3	2mA	X	X	Port 3.13	ADC: analog input 13 (AIN9 in TQFP100)
83	H12	61	P3.14/AIN14	I/O	T_T		INT4	2mA	X	X	Port 3.14	ADC: analog input 14 (AIN10 in TQFP100)
84	H11	62	P3.15/AIN15	I/O	T_T		INT5	2mA	X	X	Port 3.15	ADC: analog input 15 (AIN11 in TQFP100)
85	H10	63	V_{DD}	S							Supply voltage (5 V)	
86	H9	64	V_{SS}	S							Ground	
87	G12	65	JTRST	I	T_T	pu						JTAG reset Input
88	F12	66	JTDI	I	T_T	pu						JTAG data input
89	H8	67	JTMS	I	T_T	pu						JTAG mode selection Input
90	G11	68	JTCK	I	T_T	pd						JTAG clock Input
91	G10	69	JTDO	O				4mA				JTAG data output. **Note:** Reset state = HiZ
92	G9	70	V_{SS}	S								Ground
93	G8	71	V_{DD}	S								Supply voltage (5 V)
94	G7		P4.0/ICAPA7	I/O	T_T		WUP24	2mA	X	X	Port 4.0	TIM7: input capture A input
95	F11		P4.1/ICAPB7	I/O	T_T		WUP25	2mA	X	X	Port 4.1	TIM7: input capture B input
96	F10		P4.2/ICAPA8	I/O	T_T		WUP26	2mA	X	X	Port 4.2	TIM8: input capture A input

Table 4. STR73xF pin description

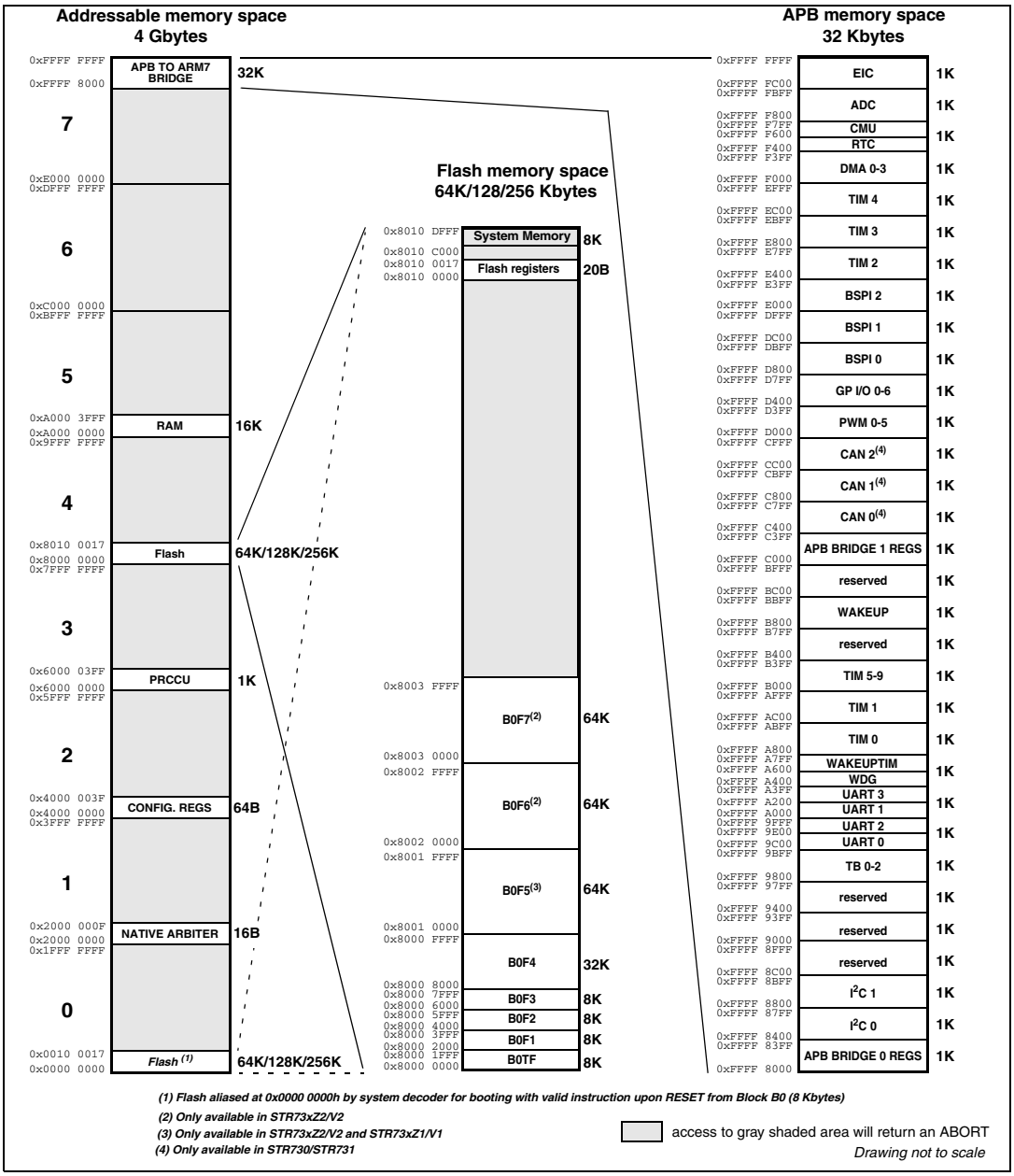
Pin n°			Pin name	Type	Input			Output			Main function (after reset)	Alternate function
TQFP144	LFBGA144	TQFP100			Input Level	pu/pd	interrupt	Capability	OD	PP		
119	B8	84	P5.9/PWM5	I/O	T_T		INT7	2mA	X	X	Port 5.9	PWM5: PWM output (TQFP100 only)
120	C8	85	P5.10/RDI2	I/O	T_T		INT8	2mA	X	X	Port 5.10	UART2: receive data input
121	A12	86	P5.11/TDO2	I/O	T_T		INT9	2mA	X	X	Port 5.11	UART2: transmit data output
122	D8	87	P5.12	I/O	T_T		INT10	2mA	X	X	Port 5.12	
123	E8		P5.13	I/O	T_T		INT11	2mA	X	X	Port 5.13	
124	B7		P5.14	I/O	T_T		INT12	2mA	X	X	Port 5.14	
125	A7		P5.15	I/O	T_T		INT13	2mA	X	X	Port 5.15	
126	A6	88	V_{18}	S								1.8 V decoupling pin: a decoupling capacitor (recommended value: 100 nF) must be connected between this pin and nearest VSS pin.
127	C7	89	V_{SS}	S								Ground
128	D7	90	V_{DD}	S								Supply voltage (5 V)
129	E7	91	P6.0	I/O	T_T		WUP0	8mA	X	X	Port 6.0	
130	F7		P6.1	I/O	T_T		WUP1	2mA	X	X	Port 6.1	
131	B6	92	P6.2/RDI3	I/O	T_T		WUP2	2mA	X	X	Port 6.2	UART3: receive data input
132	C6		P6.3	I/O	T_T		WUP3	2mA	X	X	Port 6.3	
133	D6	93	P6.4/TDO3	I/O	T_T		WUP4	2mA	X	X	Port 6.4	UART3: transmit data output
134	E6		P6.5	I/O	T_T		WUP5	2mA	X	X	Port 6.5	
135	A5	94	P6.6	I/O	T_T		WUP6	2mA	X	X	Port 6.6	
136	B5		P6.7	I/O	T_T		WUP7	2mA	X	X	Port 6.7	
137	C5	95	P6.8/RDI0	I/O	T_T		WUP10	2mA	X	X	Port 6.8	UART0: receive data input
138	A3	96	P6.9/TDO0	I/O	T_T			2mA	X	X	Port 6.9	UART0: transmit data output
139	A2		P6.10	I/O	T_T		WUP8	2mA	X	X	Port 6.10	
140	D5	97	P6.11/MISO0	I/O	T_T			2mA	X	X	Port 6.11	BSPI0: master input/slave output
141	A4	98	P6.12/MOSI0	I/O	T_T			2mA	X	X	Port 6.12	BSPI0: master output/slave input
142	B4	99	P6.13/SCK0	I/O	T_T		WUP11	2mA	X	X	Port 6.13	BSPI0: serial clock
143	C4	100	P6.14/$\overline{SS}$0	I/O	T_T			2mA	X	X	Port 6.14	BSPI0: slave select
144	B3		P6.15	I/O	T_T		WUP9	2mA	X	X	Port 6.15	

3.3 Memory mapping

Figure 5 shows the various memory configurations of the STR73xF system. The system memory map (from 0x0000_0000 to 0xFFFF_FFFF) is shown on the left part of the figure, the right part shows maps of the Flash and APB areas. For flexibility the Flash or RAM addresses can be aliased to Block 0 addresses using the remapping feature

Most reserved memory spaces (gray shaded areas in *Figure 5*) are protected from access by the user code. When an access this memory space is attempted, an ABORT signal is generated. Depending on the type of access, the ARM processor will enter “prefetch abort” state (Exception vector 0x0000_000C) or “data abort” state (Exception vector 0x0000_0010). It is up to the application software to manage these abort exceptions.

Figure 5. Memory map



4 Electrical parameters

4.1 Parameter conditions

Unless otherwise specified, all voltages are referred to V_{SS}.

4.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A=25° C and T_A=T_{Amax} (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3Σ).

4.1.2 Typical values

Unless otherwise specified, typical data are based on T_A=25° C and V_{DD}=5 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2Σ).

4.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

4.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 6*.

4.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 7*.

Figure 6. Pin loading conditions

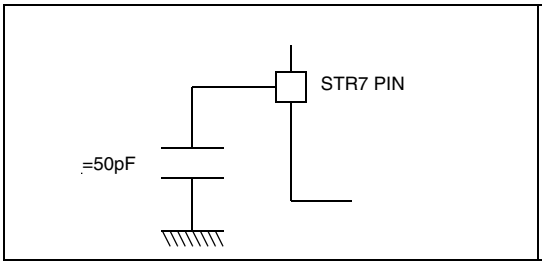
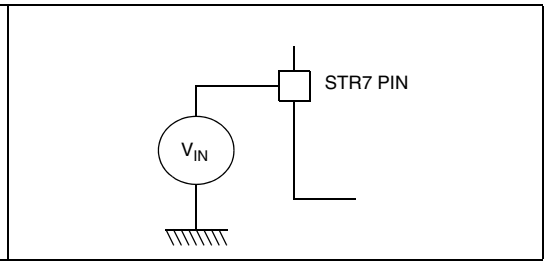


Figure 7. Pin input voltage



4.2 Absolute maximum ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 5. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DD} - V_{SS}	External 5 V Supply voltage	-0.3	6.0	V
V_{SSA}	Reference ground for A/D converter	V_{SS}	V_{SS}	V
V_{DDA}- V_{SSA}	Reference voltage for A/D converter	-0.3	V_{DD}+0.3	V
V_{IN}	Input voltage on any pin	-0.3	V_{DD}+0.3	
$\lvert\Delta V_{DDx}\rvert$	Variations between different 5 V power pins	-	0.3	mV
$\lvert V_{SSX}$ - $V_{SS}\rvert$	Variations between all the different ground pins	-	0.3	
$V_{ESD(HBM)}$	Electrostatic discharge voltage (Human Body Model)	see *: Absolute maximum ratings (electrical sensitivity) on page 36*		
$V_{ESD(MM)}$	Electrostatic discharge voltage (Machine Model)			

Table 6. Current characteristics

Symbol	Ratings	Max.	Unit
I_{VDD}	Total current into V_{DD} power lines (source) 1)	100	mA
I_{VSS}	Total current out of V_{SS} ground lines (sink) 1)	100	
I_{IO}	Output current sunk by any I/O and control pin	10	
	Output current source by any I/O and control pin	10	
$I_{INJ(PIN)}$ 2) & 3)	Injected current on any other pin 4) &5)	±10	
$\Sigma I_{INJ(PIN)}$ 2)	Total injected current (sum of all I/O and control pins) 4)	±75	

1. All 5 V power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external 5 V supply
2. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$.
3. Negative injection disturbs the analog performance of the device. See note in *Section 4.3.6: 10-bit ADC characteristics on page 43*.
4. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values). These results are based on characterization with $\Sigma I_{INJ(PIN)}$ maximum current injection on four I/O port pins of the device.

5.) In 144-pin devices, only +10 mA on P0.3, P1.13, P3.6 and P4.13 pins (negative injection not allowed).

4.3.1 Supply current characteristics

The current consumption is measured as described in *Figure 6* and *Figure 7*.

Total current consumption

The MCU is placed under the following conditions:

- All I/O pins in input mode with a static value at V_{DD} or V_{SS} (no load)
- All peripherals are disabled except if explicitly mentioned.

Subject to general operating conditions for V_{DD}, and T_A.

Table 10. Total current consumption

Symbol	Parameter	Conditions	Typ [1]	Max [2]	Unit
I_{DD}	RUN mode[3]	Formula, f_{MCLK} in MHz, RAM execution	7 + 1.9 f_{MCLK}		mA
		f_{MCLK} = 36 MHz, RAM execution	76		mA
		f_{MCLK} = 36 MHz, Flash execution	86		mA
	WFI mode	f_{OSC} = 4 MHz, f_{MCLK}= f_{OSC}/16 = 250 kHz Main voltage regulator ON, LP voltage regulator = 2 mA, RTC and WDG on, other modules off.	6.7	8	mA
	LPWFI mode	f_{RC} = high frequency (CMU_RCCTL= 0x8), f_{MCLK}= f_{RC} /16, LP voltage regulator = 2 mA, other modules off.	220	350	µA
	STOP mode	f_{OSC} = 4 MHz, RC oscillator on f_{RC} = high frequency (CMU_RCCTL= 0x0) LP voltage regulator = 6 mA, RTC and WUT ON, other modules off. Internal wake-up possible.	500	700	µA
		f_{RC} = high frequency (CMU_RCCTL= 0xF), LP voltage regulator = 2mA. WUT ON, other modules off. Internal wake-up possible.	150	220	
		LP voltage regulator = 2 mA, WIU on, Other modules off, external wake-up.	50	140	
	HALT mode	LP voltage regulator = 2 mA.	50	140	µA

1. Typical data are based on T_A=25° C, V_{DD}=5 V
2. Data based on characterization results, tested in production at V_{DD} max. and T_A = 25° C.
3. I/O in static configuration (not toggling). RUN mode is almost **independent of temperature**. On the contrary RUN mode current is **highly dependent on the application**. The I_{DDRUN} value can be significantly reduced by the application in the following ways: switch-off unused peripherals (default), reduce peripheral frequency through internal prescaler, fetch the most frequently-used functions from RAM and use low power mode when possible.

Figure 8. STOP I_{DD} vs. VDD

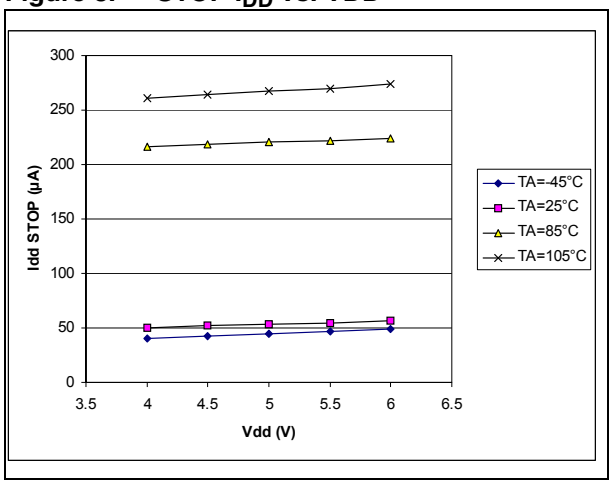


Figure 9. HALT I_{DD} vs. V_{DD}

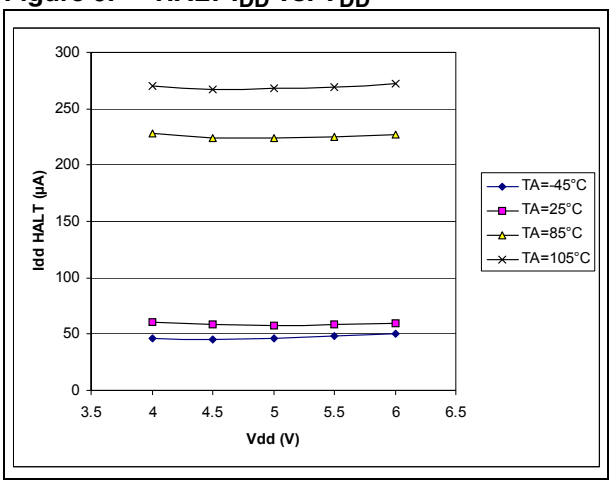


Figure 10. WFI I_{DD} vs. V_{DD}

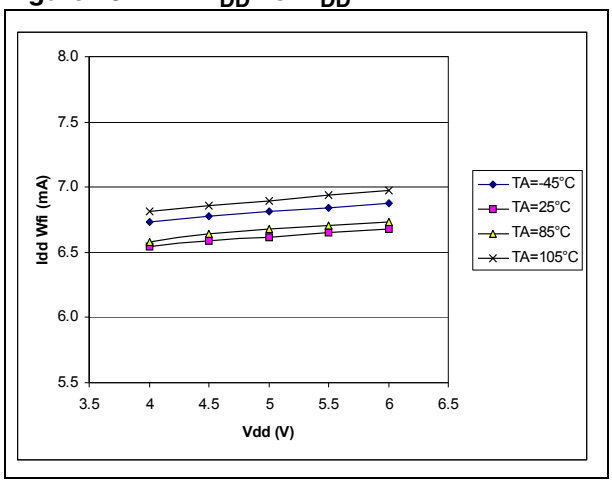
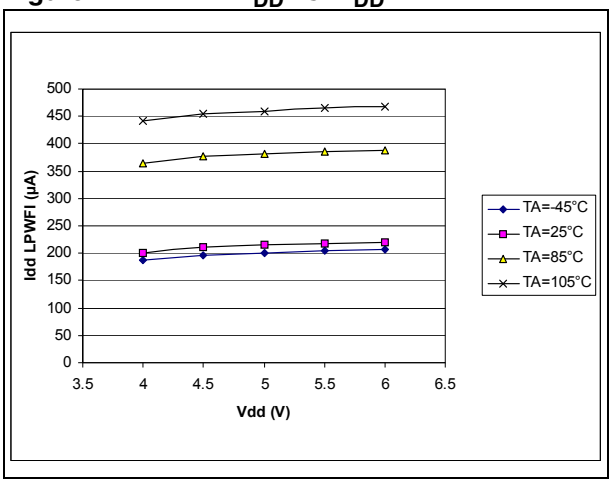


Figure 11. LPWFI I_{DD} vs. V_{DD}

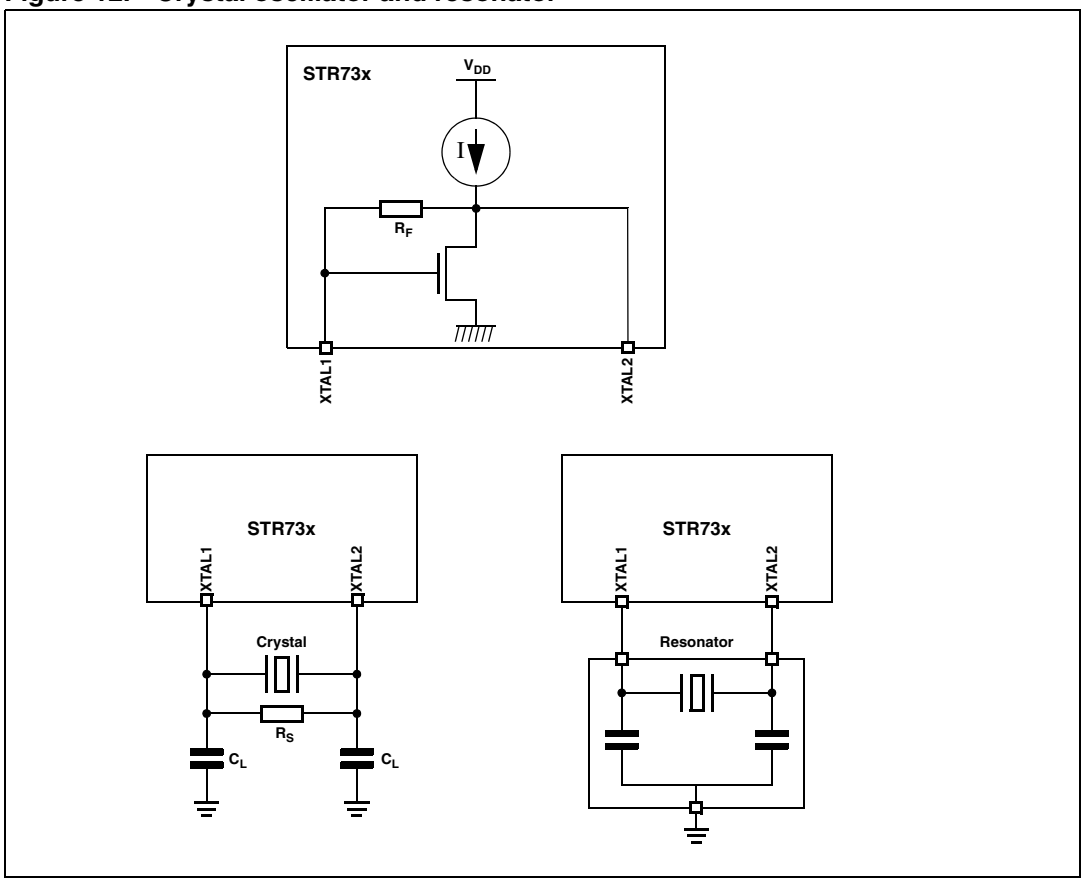


4.3.2 Clock and timing characteristics

Crystal / ceramic resonator oscillator

The STR73xF can operate with a crystal oscillator or resonator clock source. *Figure 12* describes a simple model of the internal oscillator driver as well as example of connection for an oscillator or a resonator.

Figure 12. Crystal oscillator and resonator



Note: 1 XTAL2 must not be used to directly drive external circuits.

2 For test or boot purpose, XTAL2 can be used as an high impedance input pin to provide an external clock to the device. XTAL1 should be grounded, and XTAL2 connected to a wave signal generator providing a 0 to VDD signal. Directly driving XTAL2 may results in deteriorated jitter and duty cycle.

4.3.3 Memory characteristics

Flash memory

Table 18. Flash memory characteristics

Symbol	Parameter	Test Conditions	Value			Unit
			Min	Typ	Max[1)]	
t_{WP}	Word program (32-bit)			35	80	µs
t_{DWP}	Double word program(64-bit)			64	150	µs
t_{BP64}	Bank program (64 K)	Double word program		0.5	1.25	s
t_{BP128}	Bank program (128 K)	Double word program		1	2.5	s
t_{BP256}	Bank program (256 K)	Double word program		2	4.9	s
t_{SE8}	Sector erase (8 K)	Not preprogrammed Preprogrammed [2)]		0.6 0.5	0.9 0.8	s
t_{SE32}	Sector erase (32 K)	Not preprogrammed Preprogrammed[2)]		1.1 0.8	2 1.8	s
t_{SE64}	Sector erase (64 K)	Not preprogrammed preprogrammed [2)]		1.7 1.3	3.7 3.3	s
t_{RPD}[3)]	Recovery from power-down				20	µs
t_{PSL}[3)]	Program suspend latency				10	µs
t_{ESL}[3)]	Erase suspend latency				30	µs
t_{ESR}[3)]	Erase suspend rate	Min. time from erase resume to next erase suspend		20	20	ms
t_{SP}[3)]	Set protection			40	170	µs
t_{FPW}[3)]	First word program			1		ms
N_{END}	Endurance		10			kcycles
t_{RET}	Data retention	T_A = 85° C	20			Years

1. T_A = -45° C after 0 cycles, Guaranteed by characterization, not tested in production.
2. All bits programmed to 0.
3. Guaranteed by design, not tested in production.

Electromagnetic interference (EMI)

Based on a simple application running on the product (toggling 2 LEDs through the I/O ports), the product is monitored in terms of emission. This emission test is in line with the norm SAE J 1752/3 which specifies the board and the loading of each pin.

Table 20. EMI data

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{OSC4M}/f_{MCLK}]		Unit
				6/36 MHz	8/8 MHz	
S_{EMI}	Peak level	V_{DD}=5.0V, T_A=+25°C, All packages	0.1 MHz to 30 MHz	23	30	dBµV
			30 MHz to 130 MHz	37	34	
			130 MHz to 1 GHz	20	7	
			SAE EMI Level	4	3.5	-

Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU and DLU) using specific measurement methods, the product is stressed in order to determine its performance in terms of electrical sensitivity. For more details, refer to the application note AN1181.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts*(n+1) supply pin). Two models can be simulated: human body model and machine model. This test conforms to the JESD22-A114A/A115A standard.

Table 21. ESD Absolute Maximum ratings

Symbol	Ratings	Conditions	Maximum value [1]	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A=+25° C	2000	V
$V_{ESD(MM)}$	Electrostatic discharge voltage (machine model)		200	
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)		750 on corner pins, 500 on others	

Notes:

1. Data based on characterization results, not tested in production.

Static and dynamic latch-up

- **LU**: 3 complementary static tests are required on 10 parts to assess the latch-up performance. A supply overvoltage (applied to each power supply pin) and a current injection (applied to each input, output and configurable I/O pin) are performed on each

4.3.5 I/O port pin characteristics

General characteristics

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified.

Table 23. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Input low level voltage [1]	TTL ports			0.8	V
V_{IH}	Input high level voltage [1]		2.0			
$I_{INJ(PIN)}$	Injected current on any I/O pin				±10	mA
$\Sigma I_{INJ(PIN)}$ [2]	Total injected current (sum of all I/O and control pins)				±75	mA
I_{lkg}	Input leakage current [3]	$V_{SS} \leq V_{IN} \leq V_{DD}$			±1	µA
I_S	Static current consumption [4]	Floating input mode		200		µA
R_{PU}	Weak pull-up equivalent resistor[5]	$V_{IN}=V_{SS}$	55	120	220	kΩ
R_{PD}	Weak pull-down equivalent resistor[5]	$V_{IN}=V_{DD}$	55	120	220	kΩ
C_{IO}	I/O pin capacitance			5		pF

1. Data based on characterization results, not tested in production.
2. When the current limitation is not possible, the V_{IN} absolute maximum rating must be respected, otherwise refer to $I_{INJ(PIN)}$ specification. A positive injection is induced by $V_{IN}>V_{33}$ while a negative injection is induced by $V_{IN}<V_{SS}$. Refer to *Section 4.2 on page 22* for more details.
3. Leakage could be higher than max. if negative current is injected on adjacent pins.
4. Configuration not recommended, all unused pins must be kept at a fixed voltage: using the output mode of the I/O for example or an external pull-up or pull-down resistor. Data based on design simulation and/or technology characteristics, not tested in production.
6. The R_{PU} pull-up and R_{PD} pull-down equivalent resistor are based on a resistive transistor (corresponding I_{PU} and I_{PD} current characteristics described in *Figure 19*).

Figure 15. V_{OH} JTDO pin vs I_{OL} @ V_{DD} 5 V

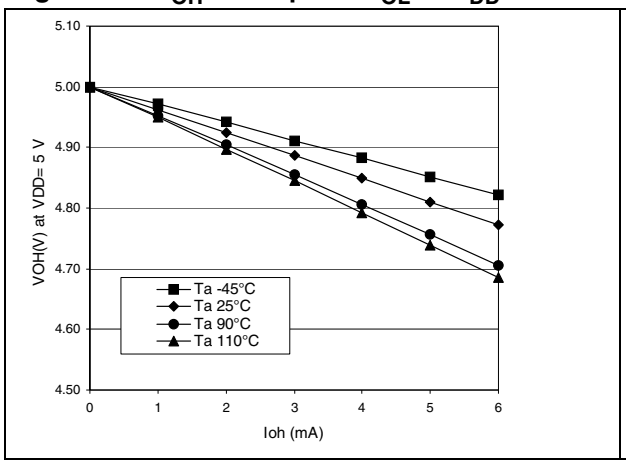


Figure 16. V_{OL} JTDO pin vs I_{OL} @ V_{DD} 5 V

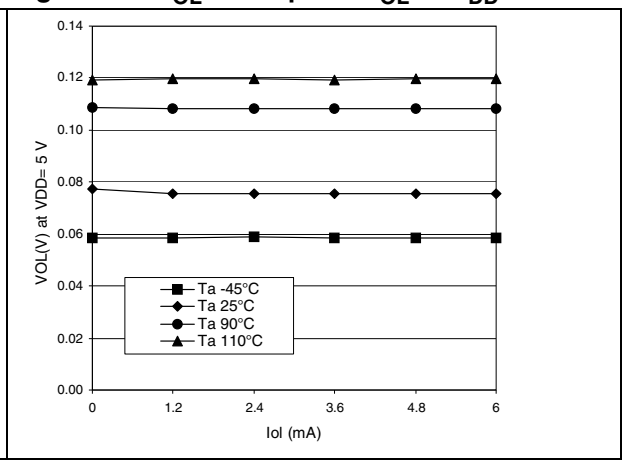


Figure 17. V_{OH} P6.0 pin vs I_{OL} @ V_{DD} 5 V

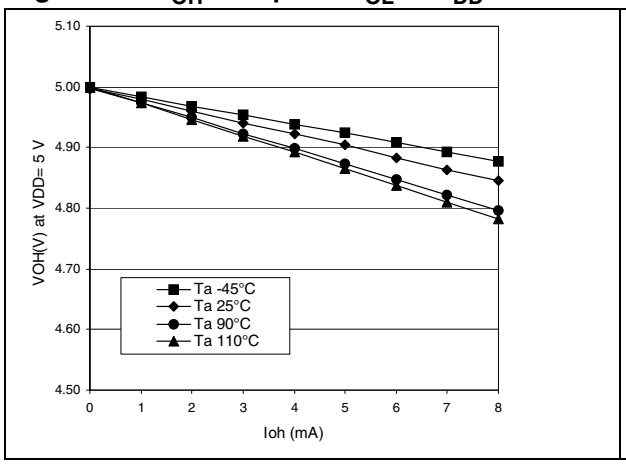
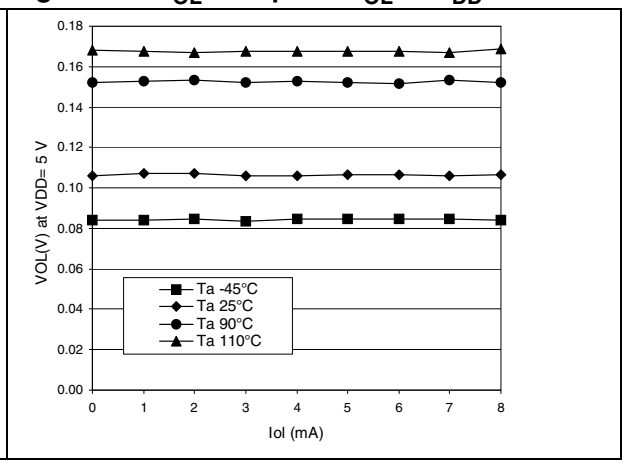


Figure 18. V_{OL} P6.0 pin vs I_{OL} @ V_{DD} 5 V



NRSTIN pin

The NRSTIN pin input driver is CMOS. A permanent pull-up is present which is the same as R_{PU} (see *: General characteristics on page 38*)

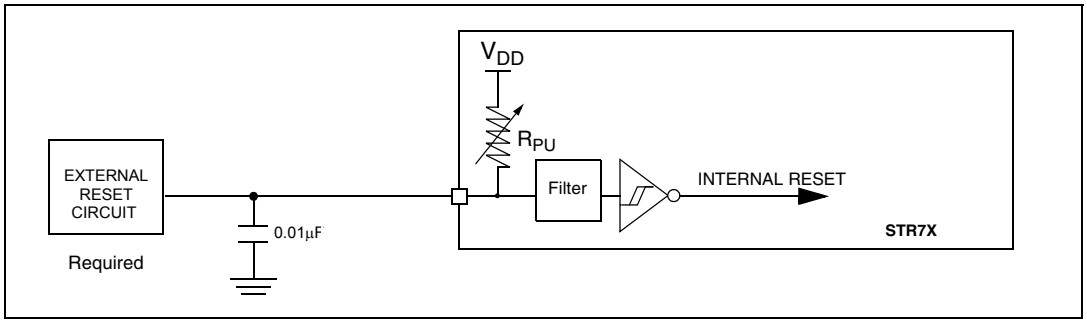
Subject to general operating conditions for V_{DD} and T_A unless otherwise specified.

Table 25. Reset pin characteristics

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
$V_{IL(NRSTIN)}$	NRSTIN Input low level voltage [1]				0.3 V_{DD}	V
$V_{IH(NRSTIN)}$	NRSTIN Input high level voltage [1]		0.7 V_{DD}			
$V_{hys(NRSTIN)}$	NRSTIN Schmitt trigger voltage hysteresis [2]			800		mV
$V_{F(RSTINn)}$	NRSTIN Input filtered pulse[3]				500	ns
$V_{NF(RSTINn)}$	NRSTIN Input not filtered pulse[3]		2			µs
$V_{RP(RSTINn)}$	NRSTIN removal after Power-up[3]		100			µs

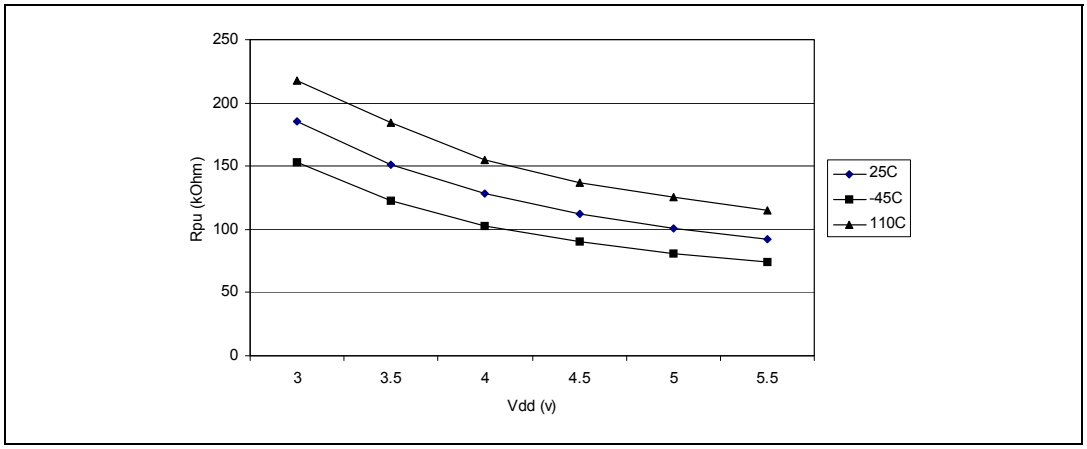
1. Data based on characterization results, not tested in production.
2. Hysteresis voltage between Schmitt trigger switching levels.
3. Data guaranteed by design, not tested in production.

Figure 19. Recommended NRSTIN pin protection[1]



1. The R_{PU} pull-up equivalent resistor is based on a resistive transistor.
2. The reset network protects the device against parasitic resets.
3. The user must ensure that the level on the NRSTIN pin can go below the $V_{IL(NRSTIN)}$ max. level specified in *Table 25*. Otherwise the reset will not be taken into account internally.

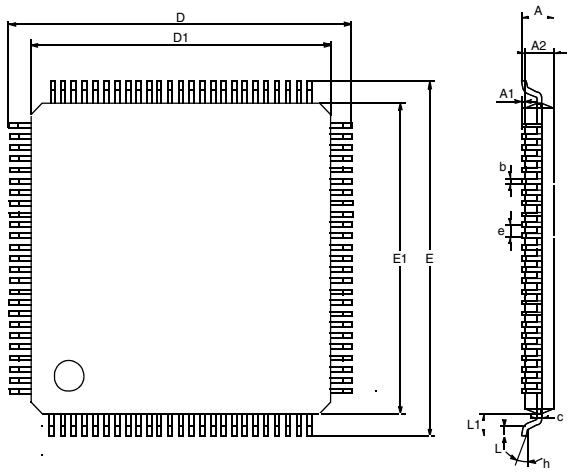
Figure 20. NRSTIN R_{PU} vs. V_{DD}



5 Package characteristics

5.1 Package mechanical data

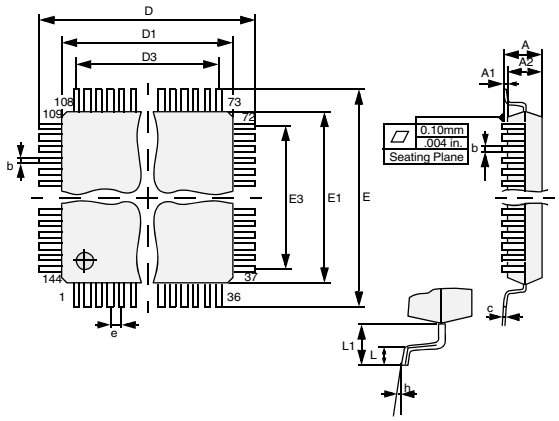
Figure 24. 100-pin thin quad flat package



Dim.	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A			1.60			0.0630
A1	0.05		0.15	0.0020		0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b	0.17	0.22	0.27	0.0067	0.0087	0.0106
C	0.09		0.20	0.0035		0.0079
D		16.00			0.6299	
D1		14.00			0.5512	
E		16.00			0.6299	
E1		14.00			0.5512	
e		0.50			0.0197	
h	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1		1.00			0.0394	
	Number of Pins					
N	100					

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 25. 144-pin thin quad flat package



Dim.	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A			1.60			0.0630
A1	0.05		0.15	0.0020		0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b	0.17	0.22	0.27	0.0067	0.0087	0.0106
c	0.09		0.20	0.0035		0.0079
D	21.80	22.00	22.20	0.8583	0.8661	0.8740
D1	19.80	20.00	20.20	0.7795	0.7874	0.7953
D3		17.50			0.6890	
E	21.80	22.00	22.20	0.8583	0.8661	0.8740
E1	19.80	20.00	20.20	0.7795	0.7874	0.7953
E3		17.50			0.6890	
e		0.50			0.0197	
K	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1		1.00			0.0394	
	Number of Pins					
N	144					

1. Values in inches are converted from mm and rounded to 4 decimal digits.