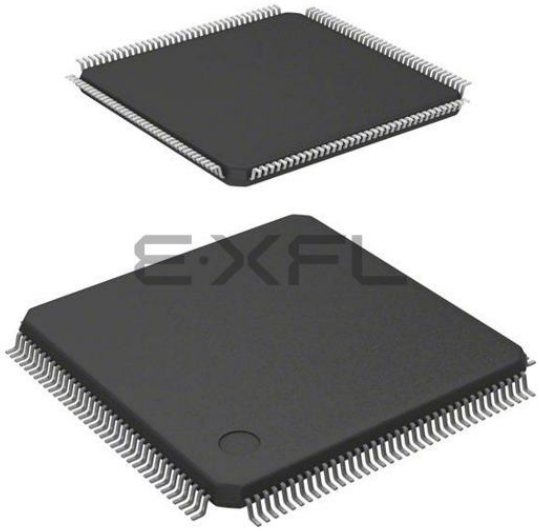

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM7®
Core Size	32-Bit Single-Core
Speed	36MHz
Connectivity	CANbus, I²C, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	112
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/str730fz2t7

Contents

1 Scope

This datasheet provides the STR73x ordering information, mechanical and electrical device characteristics.

For complete information on the STR73xF microcontroller memory, registers and peripherals. please refer to the STR73x reference manual.

For information on programming, erasing and protection of the internal Flash memory please refer to the STR7 Flash programming reference manual.

For information on the ARM7TDMI core please refer to the ARM7TDMI technical reference manual.

1.1 Description

ARM core with embedded Flash & RAM

STR73xF family combines the high performance ARM7TDMI™ CPU with an extensive range of peripheral functions and enhanced I/O capabilities. All devices have on-chip high-speed single voltage Flash memory and high-speed RAM. The STR73xF family has an embedded ARM core and is therefore compatible with all ARM tools and software.

Extensive tools support

STMicroelectronics' 32-bit, ARM core-based microcontrollers are supported by a complete range of high-end and low-cost development tools to meet the needs of application developers. This extensive line of hardware/software tools includes starter kits and complete development packages all tailored for ST's ARM core-based MCUs.

The range of development packages includes third-party solutions that come complete with a graphical development environment and an in-circuit emulator/programmer featuring a JTAG application interface. These support a range of embedded operating systems (OS), while several royalty-free OSs are also available.

For more information, please refer to ST MCU site http://www.st.com/mcu

Figure 1 shows the general block diagram of the device family.

3 Block diagram

Figure 1. STR730F/STR735F block diagram

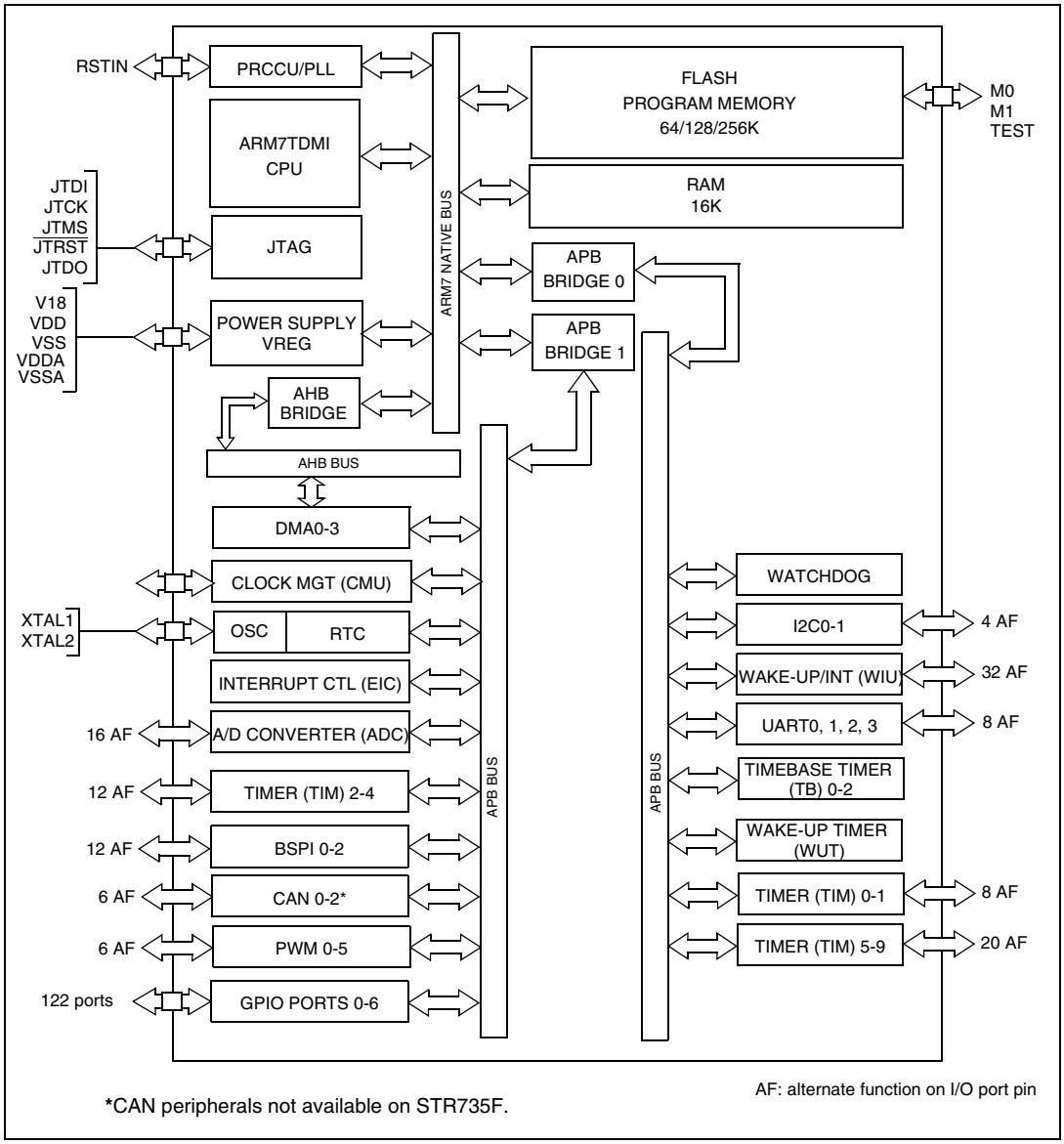
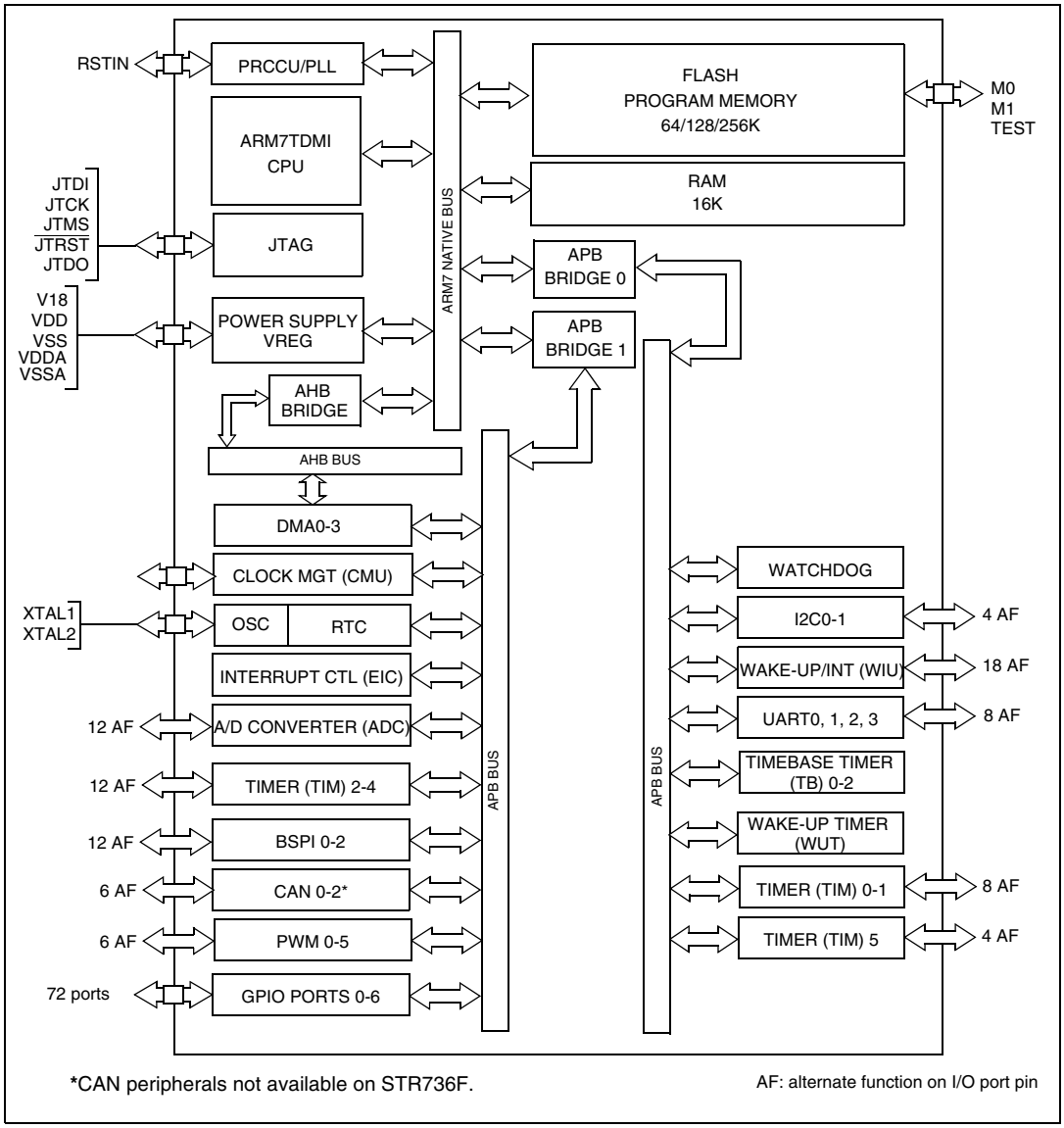


Figure 2. STR731F/STR736 block diagram



*CAN peripherals not available on STR736F.

AF: alternate function on I/O port pin

3.2.2 STR730F/STR735F (LFBGA144)

Table 3. STR730F/STR735F LFBGA ball connections

Ball	Name	Ball	Name	Ball	Name	Ball	Name
A1	P0.0 / OCMPB2	B1	P0.4 / OCMPA5	C1	P0.5 / OCMPB5	D1	V_{SS}
A2	P6.10 / WUP8	B2	P0.1 / OCMPA2	C2	P0.2 / ICAPA2	D2	V_{DD}
A3	P6.9 / TDO0	B3	P6.15 / WUP9	C3	P0.3 / ICAPB2	D3	P0.6 / ICAPA5
A4	P6.12 / MOSI0	B4	P6.13 / SCKO / WUP11	C4	P6.14 / SSO	D4	P0.7 /ICAPB5
A5	P6.6 / WUP6	B5	P6.7 / WUP7	C5	P6.8 / RDI0 / WUP10	D5	P6.11 / MISO0
A6	V_{18}	B6	P6.2 / WUP2 / RDI3	C6	P6.3 / WUP3	D6	P6.4 / WUP4 /TDO3
A7	P5.15 / INT13	B7	P5.14 / INT12	C7	V_{SS}	D7	VDD
A8	P5.8 / INT6	B8	P5.9 / INT7	C8	P5.10 / INT8 / RDI2	D8	P5.12 / INT10
A9	P5.2 / OCMPA9	B9	P5.3 / OCMPB9	C9	P5.4 / SS2	D9	P5.5 / SCK2 / WUP23
A10	P5.7 / MISO2	B10	P5.0 / MOSI1	C10	P5.1 / MISO1	D10	P4.13 / ICAPB9
A11	P5.6 / MOSI2	B11	P4.15 / SCK1 / WUP22	C11	P4.14 / SS1	D11	P4.12 / ICAPA9 / WUP21
A12	P5.11 / TDO2 / INT9	B12	P4.8 / OCMPA8	C12	P4.7 / SDA1	D12	P4.11 / OCMPB8
E1	P0.8 / OCMPA6	F1	V_{DD}	G1	V_{SS}	H1	V_{DD}
E2	P0.9 / OCMPB6	F2	P0.13 / ICAPB3	G2	P1.2 / ICAPB4	H2	P1.8 / OCMPA0 / INT0
E3	P0.10 / OCMPA7	F3	P0.14 / OCMPB3	G3	P1.3 / ICAPA4	H3	P1.9 / OCMPB0 / INT1
E4	P0.11 / OCMPB7	F4	P0.15 / OCMPA3	G4	V_{SS}	H4	P1.10 / ICAPB0 / WUP28
E5	P0.12 / ICAPA3	F5	P1.0 / OCMPA4	G5	P1.5	H5	XTAL2
E6	P6.5 / WUP5	F6	P1.1 / OCMPB4	G6	P2.11 / WUP17	H6	P2.10 / WUP16
E7	P6.0 / WUP0	F7	P6.1 / WUP1	G7	P4.0 / ICAPA7 / WUP24	H7	P2.15 / SDA 0
E8	P5.13 / INT11	F8	P4.4 / CAN2TX[1)]	G8	VDD	H8	JTMS
E9	P4.10 / ICAPA6 / WUP20	F9	P4.3 / ICAPB8 / WUP27	G9	VSS	H9	VSS
E10	P4.9 / ICAPB6	F10	P4.2 / ICAPA8 / WUP26	G10	JTDO	H10	VDD
E11	P4.6 / SCL1 / WUP19	F11	P4.1 / ICAPB7 / WUP25	G11	JTCK	H11	P3.15 / AIN15 / INT5
E12	P4.5 / WUP18 / CAN2RX[1)]	F12	JTDI	G12	nJTRST	H12	P3.14 / AIN14 / INT4
J1	P1.4	K1	P1.6 / OCMPB1	L1	P1.7 / OCMPA1	M1	P1.14 / CAN0RX[1)] / WUP12
J2	P1.11 / ICAPA0 / WUP29	K2	P1.13 / ICAPB1 / WUP31	L2	P1.15 / CAN0TX[1)]	M2	P2.4 / PWM2
J3	P1.12 / ICAPA1 / WUP30	K3	P2.1 / CAN1RX[1)] / WUP13	L3	P2.0 / PWM0	M3	P2.5 / PWM3
J4	P2.7 / PWM5	K4	P2.6 / PWM4	L4	P2.3 / PWM1	M4	P2.2 / CAN1TX[1)]
J5	V_{DD}	K5	M1	L5	RSTIN	M5	M0
J6	P2.9 / RDI1 / WUP14	K6	P2.8 / TDO1	L6	V_{SS}	M6	V_{SS}
J7	P2.14 / SCL 0 / WUP15	K7	P2.13 / INT15	L7	P2.12 / INT14	M7	XTAL1
J8	P3.1 / AIN1	K8	P3.0 / AIN0	L8	VBIAS	M8	TST
J9	P3.13 / AIN13 / INT3	K9	P3.4 / AIN4	L9	P3.3 / AIN3	M9	P3.2 / AIN2
J10	P3.12 / AIN12 / INT2	K10	V_{DDA}	L10	P3.5 / AIN5	M10	V_{SS}
J11	P3.9 / AIN9	K11	V_{SSA}	L11	P3.7 / AIN7	M11	V_{DD}
J12	P3.8 / AIN8	K12	P3.11 / AIN11	L12	P3.10 / AIN10	M12	P3.6 / AIN6

Note: CAN alternate functions not available on STR735F.

Legend / Abbreviations for *Table 4*:

Type: I = input, O = output, S = supply, HiZ= high impedance,

In/Output level: T_T= TTL 0.8 V / 2 V with input trigger
C_T= CMOS $0.3V_{DD}/0.7V_{DD}$ with input trigger

Port and control configuration:

Input: pu/pd = with internal 100 kΩ weak pull-up or pull down

Output: OD = open drain (logic level)
PP = push-pull

Interrupts:

INTx = external interrupt line

WUPx = wake-up interrupt line

The reset state (during and just after the reset) of the I/O ports is input floating (Input tristate TTL mode). To avoid excess power consumption, unused I/O ports must be tied to ground.

Table 4. STR73xF pin description

Pin n°			Pin name	Type	Input			Output			Main function (after reset)	Alternate function
TQFP144	LFBGA144	TQFP100			Input Level	pu/pd	interrupt	Capability	OD	PP		
1	A1	1	P0.0/OCMPB2	I/O	T_T			2mA	X	X	Port 0.0	TIM2: output compare B output
2	B2	2	P0.1/OCMPA2	I/O	T_T			2mA	X	X	Port 0.1	TIM2: output compare A output
3	C2	3	P0.2/ICAPA2	I/O	T_T			2mA	X	X	Port 0.2	TIM2: input capture A input
4	C3	4	P0.3/ICAPB2	I/O	T_T			2mA	X	X	Port 0.3	TIM2: input capture B input
5	D1		V_{SS}	S							Ground	
6	D2		V_{DD}	S							Supply voltage (5 V)	
7	B1	5	P0.4/OCMPA5	I/O	T_T			2mA	X	X	Port 0.4	TIM5: output compare A output
8	C1	6	P0.5/OCMPB5	I/O	T_T			2mA	X	X	Port 0.5	TIM5: output compare B output
9	D3	7	P0.6/ICAPA5	I/O	T_T			2mA	X	X	Port 0.6	TIM5: input capture A input
10	D4		P0.7/ICAPB5	I/O	T_T			2mA	X	X	Port 0.7	TIM5: input capture B input
11	E1		P0.8/OCMPA6	I/O	T_T			2mA	X	X	Port 0.8	TIM6: output compare A output
12	E2		P0.9/OCMPB6	I/O	T_T			2mA	X	X	Port 0.9	TIM6: output compare B output
13	E3		P0.10/OCMPA7	I/O	T_T			2mA	X	X	Port 0.10	TIM7: output compare A output
14	E4		P0.11/OCMPB 7	I/O	T_T			2mA	X	X	Port 0.11	TIM7: output compare B output
15	F1	8	V_{DD}	S							Supply voltage (5 V)	
16	G1	9	V_{SS}	S							Ground	
17	E5	10	P0.12/ICAPA3	I/O	T_T			2mA	X	X	Port 0.12	TIM3: input capture A input
18	F2	11	P0.13/ICAPB3	I/O	T_T			2mA	X	X	Port 0.13	TIM3: input capture B input

Table 4. STR73xF pin description

Pin n°			Pin name	Type	Input			Output			Main function (after reset)	Alternate function
TQFP144	LFBGA144	TQFP100			Input Level	pu/pd	interrupt	Capability	OD	PP		
19	F3	12	P0.14/OCMPB3	I/O	T_T			2mA	X	X	Port 0.14	TIM3: output compare B output
20	F4	13	P0.15/OCMPA3	I/O	T_T			2mA	X	X	Port 0.15	TIM3: output compare A output
21	F5	14	P1.0/OCMPA4	I/O	T_T			2mA	X	X	Port 1.0	TIM4: output compare A output
22	F6	15	P1.1/OCMPB4	I/O	T_T			2mA	X	X	Port 1.1	TIM4: output compare B output
23	G2	16	P1.2/ICAPB4	I/O	T_T			2mA	X	X	Port 1.2	TIM4: input capture B input
24	G3	17	P1.3/ICAPA4	I/O	T_T			2mA	X	X	Port 1.3	TIM4: input capture A input
25	G4		V_{SS}	S							Ground	
26	H1		V_{DD}	S							Supply voltage (5 V)	
27	J1		P1.4	I/O	T_T			2mA	X	X	Port 1.4	
28	G5		P1.5	I/O	T_T			2mA	X	X	Port 1.5	
29	K1	18	P1.6/OCMPB1	I/O	T_T			2mA	X	X	Port 1.6	TIM1: output compare B output
30	L1	19	P1.7/OCMPA1	I/O	T_T			2mA	X	X	Port 1.7	TIM1: output compare A output
31	H2	20	P1.8/OCMPA0	I/O	T_T		INT0	2mA	X	X	Port 1.8	TIM0: output compare A output
32	H3	21	P1.9/OCMPB0	I/O	T_T		INT1	2mA	X	X	Port 1.9	TIM0: output compare B output
33	H4	22	P1.10/ICAPB0	I/O	T_T		WUP28	2mA	X	X	Port 1.10	TIM0: input capture B input
34	J2	23	P1.11/ICAPA0	I/O	T_T		WUP29	2mA	X	X	Port 1.11	TIM0: input capture A input
35	J3	24	P1.12/ICAPA1	I/O	T_T		WUP30	2mA	X	X	Port 1.12	TIM1: input capture A input
36	K2	25	P1.13/ICAPB1	I/O	T_T		WUP31	2mA	X	X	Port 1.13	TIM1: input capture B input
37	M1	26	P1.14/CAN0RX	I/O	T_T		WUP12	2mA	X	X	Port 1.14	CAN0: receive data input
38	L2	27	P1.15/CAN0TX	I/O	T_T			2mA	X	X	Port 1.15	CAN0: transmit data output
39	L3	28	P2.0/PWM0	I/O	T_T			2mA	X	X	Port 2.0	PWM0: PWM output
40	K3	29	P2.1/CAN1RX	I/O	T_T		WUP13	2mA	X	X	Port 2.1	CAN1: receive data input
41	M4	30	P2.2/CAN1TX	I/O	T_T			2mA	X	X	Port 2.2	CAN1: transmit data output
42	L4	31	P2.3/PWM1	I/O	T_T			2mA	X	X	Port 2.3	PWM1: PWM output
43	M2	32	P2.4/PWM2	I/O	T_T			2mA	X	X	Port 2.4	PWM2: PWM output
44	M3		P2.5/PWM3	I/O	T_T			2mA	X	X	Port 2.5	PWM3: PWM output
45	K4		P2.6/PWM4	I/O	T_T			2mA	X	X	Port 2.6	PWM4: PWM output
46	J4		P2.7/PWM5	I/O	T_T			2mA	X	X	Port 2.7	PWM5: PWM output
47	M5	33	M0	I	T_T	pd					BOOT: mode selection 0 input	
48	L5	34	RSTIN	I	C_T	pu					Reset input	
49	K5	35	M1	I	T_T	pd					BOOT: mode selection 1 input	

Table 4. STR73xF pin description

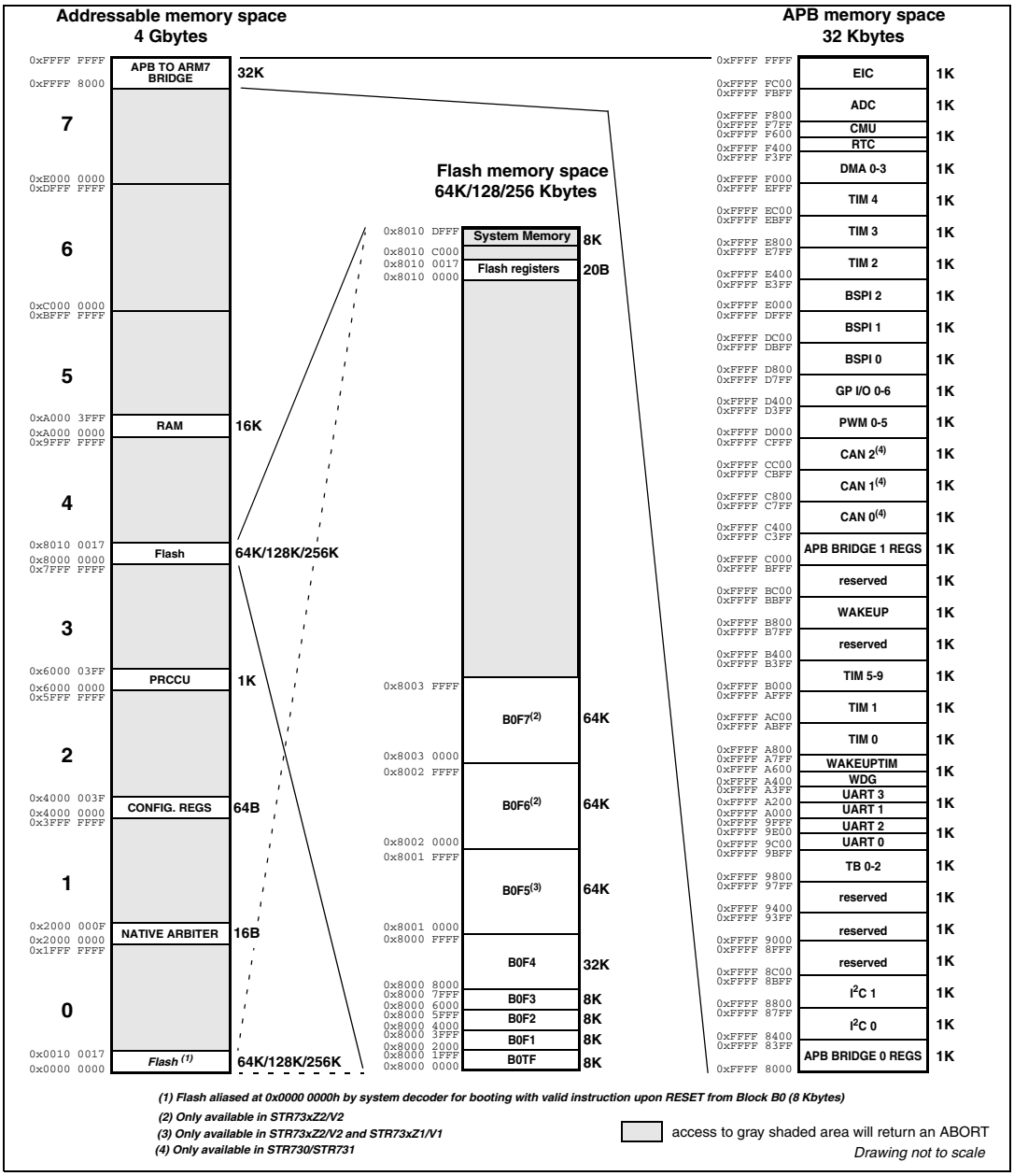
Pin n°			Pin name	Type	Input			Output			Main function (after reset)	Alternate function
TQFP144	LFBGA144	TQFP100			Input Level	pu/pd	interrupt	Capability	OD	PP		
73	M12	51	P3.6/AIN6	I/O	T_T			2mA	X	X	Port 3.6	ADC: analog input 6 (AIN2 in TQFP100)
74	L11	52	P3.7/AIN7	I/O	T_T			2mA	X	X	Port 3.7	ADC: analog input 7 (AIN3 in TQFP100)
75	K11	53	V_{SSA}	S							Reference ground for A/D converter	
76	K10	54	V_{DDA}	S							Reference voltage for A/D converter	
77	J12	55	P3.8/AIN8	I/O	T_T			2mA	X	X	Port 3.8	ADC: analog input 8 (AIN4 in TQFP100)
78	J11	56	P3.9/AIN9	I/O	T_T			2mA	X	X	Port 3.9	ADC: analog input 9 (AIN5 in TQFP100)
79	L12	57	P3.10/AIN10	I/O	T_T			2mA	X	X	Port 3.10	ADC: analog input 10 (AIN6 in TQFP100)
80	K12	58	P3.11/AIN11	I/O	T_T			2mA	X	X	Port 3.11	ADC: analog input 11 (AIN7 in TQFP100)
81	J10	59	P3.12/AIN12	I/O	T_T		INT2	2mA	X	X	Port 3.12	ADC: analog input 12 (AIN8 in TQFP100)
82	J9	60	P3.13/AIN13	I/O	T_T		INT3	2mA	X	X	Port 3.13	ADC: analog input 13 (AIN9 in TQFP100)
83	H12	61	P3.14/AIN14	I/O	T_T		INT4	2mA	X	X	Port 3.14	ADC: analog input 14 (AIN10 in TQFP100)
84	H11	62	P3.15/AIN15	I/O	T_T		INT5	2mA	X	X	Port 3.15	ADC: analog input 15 (AIN11 in TQFP100)
85	H10	63	V_{DD}	S							Supply voltage (5 V)	
86	H9	64	V_{SS}	S							Ground	
87	G12	65	JTRST	I	T_T	pu						JTAG reset Input
88	F12	66	JTDI	I	T_T	pu						JTAG data input
89	H8	67	JTMS	I	T_T	pu						JTAG mode selection Input
90	G11	68	JTCK	I	T_T	pd						JTAG clock Input
91	G10	69	JTDO	O				4mA				JTAG data output. **Note:** Reset state = HiZ
92	G9	70	V_{SS}	S								Ground
93	G8	71	V_{DD}	S								Supply voltage (5 V)
94	G7		P4.0/ICAPA7	I/O	T_T		WUP24	2mA	X	X	Port 4.0	TIM7: input capture A input
95	F11		P4.1/ICAPB7	I/O	T_T		WUP25	2mA	X	X	Port 4.1	TIM7: input capture B input
96	F10		P4.2/ICAPA8	I/O	T_T		WUP26	2mA	X	X	Port 4.2	TIM8: input capture A input

3.3 Memory mapping

Figure 5 shows the various memory configurations of the STR73xF system. The system memory map (from 0x0000_0000 to 0xFFFF_FFFF) is shown on the left part of the figure, the right part shows maps of the Flash and APB areas. For flexibility the Flash or RAM addresses can be aliased to Block 0 addresses using the remapping feature

Most reserved memory spaces (gray shaded areas in *Figure 5*) are protected from access by the user code. When an access this memory space is attempted, an ABORT signal is generated. Depending on the type of access, the ARM processor will enter “prefetch abort” state (Exception vector 0x0000_000C) or “data abort” state (Exception vector 0x0000_0010). It is up to the application software to manage these abort exceptions.

Figure 5. Memory map



4 Electrical parameters

4.1 Parameter conditions

Unless otherwise specified, all voltages are referred to V_{SS}.

4.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A=25° C and T_A=T_{Amax} (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3Σ).

4.1.2 Typical values

Unless otherwise specified, typical data are based on T_A=25° C and V_{DD}=5 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2Σ).

4.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

4.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 6*.

4.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 7*.

Figure 6. Pin loading conditions

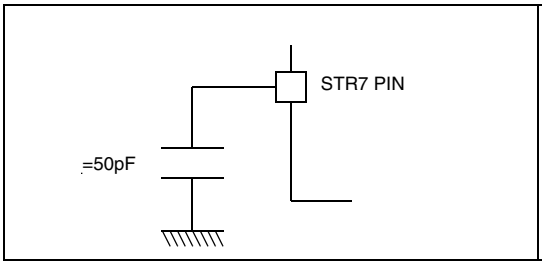
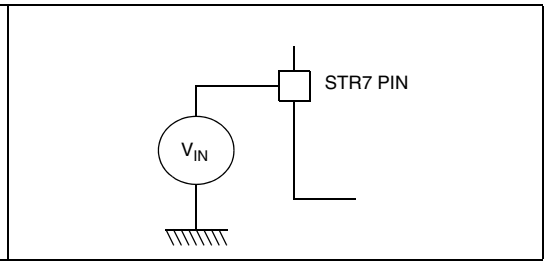


Figure 7. Pin input voltage



4.3.1 Supply current characteristics

The current consumption is measured as described in *Figure 6* and *Figure 7*.

Total current consumption

The MCU is placed under the following conditions:

- All I/O pins in input mode with a static value at V_{DD} or V_{SS} (no load)
- All peripherals are disabled except if explicitly mentioned.

Subject to general operating conditions for V_{DD}, and T_A.

Table 10. Total current consumption

Symbol	Parameter	Conditions	Typ [1]	Max [2]	Unit
I_{DD}	RUN mode[3]	Formula, f_{MCLK} in MHz, RAM execution	7 + 1.9 f_{MCLK}		mA
		f_{MCLK} = 36 MHz, RAM execution	76		mA
		f_{MCLK} = 36 MHz, Flash execution	86		mA
	WFI mode	f_{OSC} = 4 MHz, f_{MCLK}= f_{OSC}/16 = 250 kHz Main voltage regulator ON, LP voltage regulator = 2 mA, RTC and WDG on, other modules off.	6.7	8	mA
	LPWFI mode	f_{RC} = high frequency (CMU_RCCTL= 0x8), f_{MCLK}= f_{RC} /16, LP voltage regulator = 2 mA, other modules off.	220	350	µA
	STOP mode	f_{OSC} = 4 MHz, RC oscillator on f_{RC} = high frequency (CMU_RCCTL= 0x0) LP voltage regulator = 6 mA, RTC and WUT ON, other modules off. Internal wake-up possible.	500	700	µA
		f_{RC} = high frequency (CMU_RCCTL= 0xF), LP voltage regulator = 2mA. WUT ON, other modules off. Internal wake-up possible.	150	220	
		LP voltage regulator = 2 mA, WIU on, Other modules off, external wake-up.	50	140	
	HALT mode	LP voltage regulator = 2 mA.	50	140	µA

1. Typical data are based on T_A=25° C, V_{DD}=5 V
2. Data based on characterization results, tested in production at V_{DD} max. and T_A = 25° C.
3. I/O in static configuration (not toggling). RUN mode is almost **independent of temperature**. On the contrary RUN mode current is **highly dependent on the application**. The I_{DDRUN} value can be significantly reduced by the application in the following ways: switch-off unused peripherals (default), reduce peripheral frequency through internal prescaler, fetch the most frequently-used functions from RAM and use low power mode when possible.

On-chip peripherals

Table 13. Peripheral current consumption at T_A= 25°C

Symbol	Parameter	Conditions	Typ	Unit
$I_{DD(RC)}$	RC (backup oscillator) supply current	High frequency	120	µA
		Low frequency	60	µA
$I_{DD(TIM)}$	TIM timer supply current [1]	f_{MCLK}=36 MHz	350	µA
$I_{DD(BSPI)}$	BSPI supply current [1]		1.1	mA
$I_{DD(UART)}$	UART supply current [1]		850	µA
$I_{DD(I2C)}$	I2C supply current [1]		430	µA
$I_{DD(ADC)}$	ADC supply current when converting [2]		5	mA
$I_{DD(EIC)}$	EIC supply current		2.88	mA
$I_{DD(CAN)}$	CAN supply current [1]		2.95	mA
$I_{DD(GPIO)}$	GPIO supply current		150	µA
$I_{DD(TB)}$	TB supply current		250	µA
$I_{DD(PWM)}$	PWM supply current		240	µA
$I_{DD(RTC)}$	RTC supply current		370	µA
$I_{DD(DMA)}$	DMA supply current		2.5	mA
$I_{DD(ARB)}$	Native arbiter supply current		180	µA
$I_{DD(AHB)}$	AHB arbiter supply current		570	µA
$I_{DD(WUT)}$	WUT supply current		300	µA
$I_{DD(WIU)}$	WIU supply current		460	µA

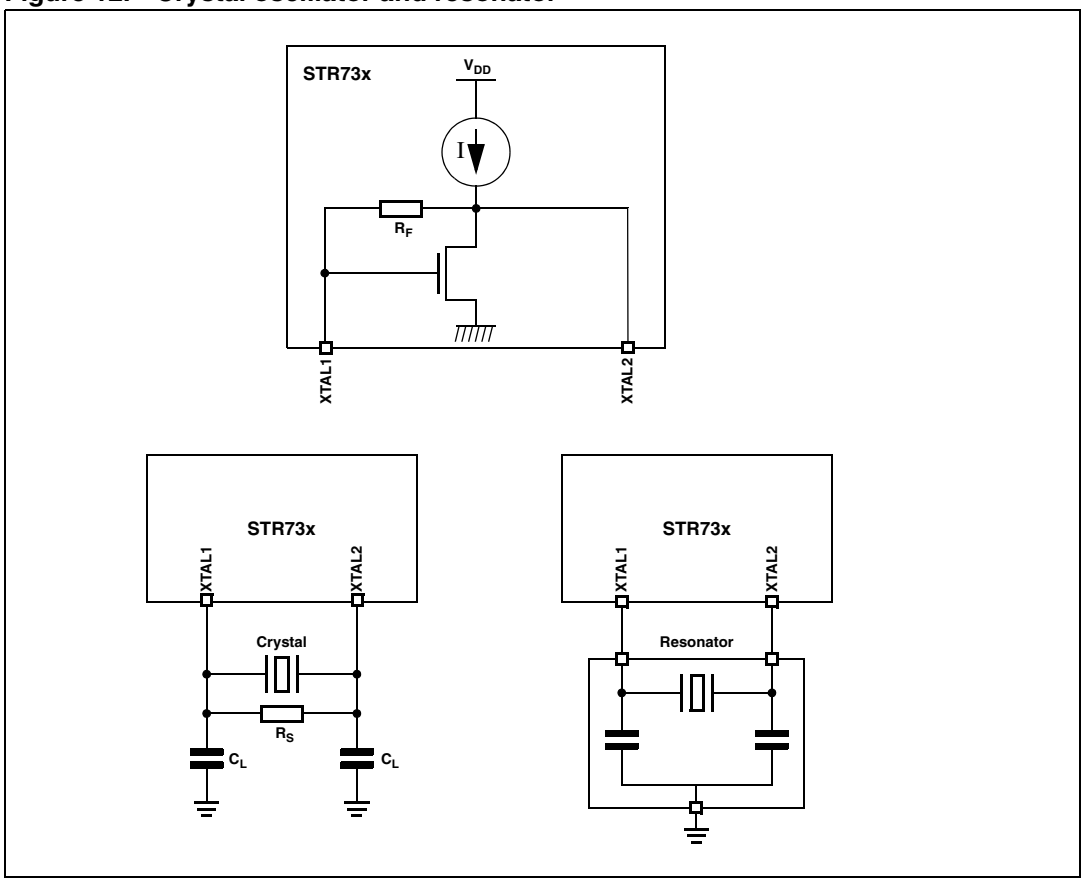
1. Data based on a differential I_{DD} measurement between the on-chip peripheral when kept under reset, not clocked and the on-chip peripheral when clocked and not kept under reset. This measurement does not include the pad toggling consumption.
2. Data based on a differential I_{DD} measurement between reset configuration and continuous A/D conversions.

4.3.2 Clock and timing characteristics

Crystal / ceramic resonator oscillator

The STR73xF can operate with a crystal oscillator or resonator clock source. *Figure 12* describes a simple model of the internal oscillator driver as well as example of connection for an oscillator or a resonator.

Figure 12. Crystal oscillator and resonator



Note: 1 XTAL2 must not be used to directly drive external circuits.

2 For test or boot purpose, XTAL2 can be used as an high impedance input pin to provide an external clock to the device. XTAL1 should be grounded, and XTAL2 connected to a wave signal generator providing a 0 to VDD signal. Directly driving XTAL2 may results in deteriorated jitter and duty cycle.

PLL electrical characteristics

V_{DD} = 5 V ± 10%, T_A = -40° C to T_{Amax}, unless otherwise specified

Table 16. PLL characteristics

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
f_{PLLIN} (1)	PLL reference clock	FREF_RANGE = '0' FREF_RANGE = '1'	1.5 3.0		3.0 5.0	MHz
f_{PLLOUT}	PLL output clock	MX = "00" MX = "01" MX = "10" MX = "11"	20 x f_{PLLIN} 12 x f_{PLLIN} 28 x f_{PLLIN} 16 x f_{PLLIN}			MHz
f_{MCLK}	System clock	DX = 1..7	f_{PLLOUT}/DX		36	MHz
f_{FREE} (2)	PLL free running frequency	FREF_RANGE = '0', MX0 = '1' FREF_RANGE = '0', MX0 = '0' FREF_RANGE = '1', MX0 = '1' FREF_RANGE = '1', MX0 = '0'		120 240 240 480		kHz
t_{LOCK} (3)	PLL lock time	Stable oscillator (f_{PLLIN} = 4 MHz), stable V_{DD}		100	300	µs
Δt_{PKJIT}	PLL jitter (pk to pk)	f_{PLLIN} = 4 MHz (pulse generator)			1.5	ns

1. f_{PLLIN} is obtained from f_{OSC} directly or through an optional divider by 2.
2. Typical data are based on T_A=25°C, V_{DD}=5V
3. Max value is guaranteed by characterization, not tested in production.

Table 17. Low-power mode wake-up timing

Symbol	Parameter	Conditions	Typ	Unit
t_{WUHALT}	Wake-up from HALT mode		200	µs
t_{WUSTOP}	Wake-up from STOP mode	RC high frequency in STOP mode	180	µs
		RC low frequency in STOP mode	234	µs
$t_{WULPWFI}$ 1)	Wake-up from LPWFI mode	Main voltage regulator on RC oscillator off f_{OSC} = 4 MHz, f_{MCLK}= f_{OSC}/16 RAM or FLASH execution	27	µs
		Main voltage regulator on RC oscillator = high frequency Flash execution	46	µs
		Main voltage regulator on RC oscillator = low frequency Flash execution	3.6	ms

1. Flash memory programmed to enter Power Down mode during LPWFI.

4.3.3 Memory characteristics

Flash memory

Table 18. Flash memory characteristics

Symbol	Parameter	Test Conditions	Value			Unit
			Min	Typ	Max[1)]	
t_{WP}	Word program (32-bit)			35	80	µs
t_{DWP}	Double word program(64-bit)			64	150	µs
t_{BP64}	Bank program (64 K)	Double word program		0.5	1.25	s
t_{BP128}	Bank program (128 K)	Double word program		1	2.5	s
t_{BP256}	Bank program (256 K)	Double word program		2	4.9	s
t_{SE8}	Sector erase (8 K)	Not preprogrammed Preprogrammed [2)]		0.6 0.5	0.9 0.8	s
t_{SE32}	Sector erase (32 K)	Not preprogrammed Preprogrammed[2)]		1.1 0.8	2 1.8	s
t_{SE64}	Sector erase (64 K)	Not preprogrammed preprogrammed [2)]		1.7 1.3	3.7 3.3	s
t_{RPD}[3)]	Recovery from power-down				20	µs
t_{PSL}[3)]	Program suspend latency				10	µs
t_{ESL}[3)]	Erase suspend latency				30	µs
t_{ESR}[3)]	Erase suspend rate	Min. time from erase resume to next erase suspend		20	20	ms
t_{SP}[3)]	Set protection			40	170	µs
t_{FPW}[3)]	First word program			1		ms
N_{END}	Endurance		10			kcycles
t_{RET}	Data retention	T_A = 85° C	20			Years

1. T_A = -45° C after 0 cycles, Guaranteed by characterization, not tested in production.
2. All bits programmed to 0.
3. Guaranteed by design, not tested in production.

Figure 15. V_{OH} JTDO pin vs I_{OL} @ V_{DD} 5 V

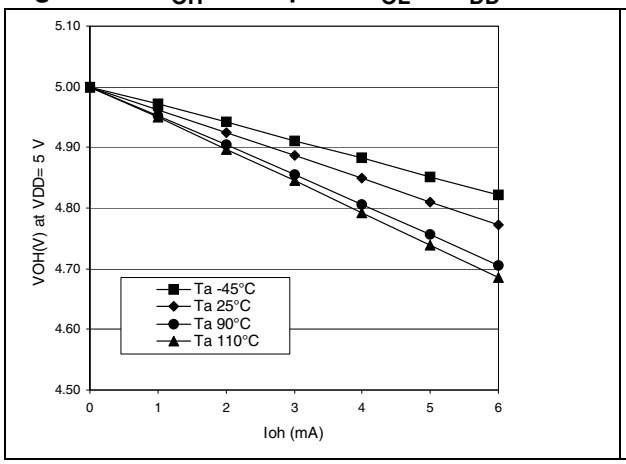


Figure 16. V_{OL} JTDO pin vs I_{OL} @ V_{DD} 5 V

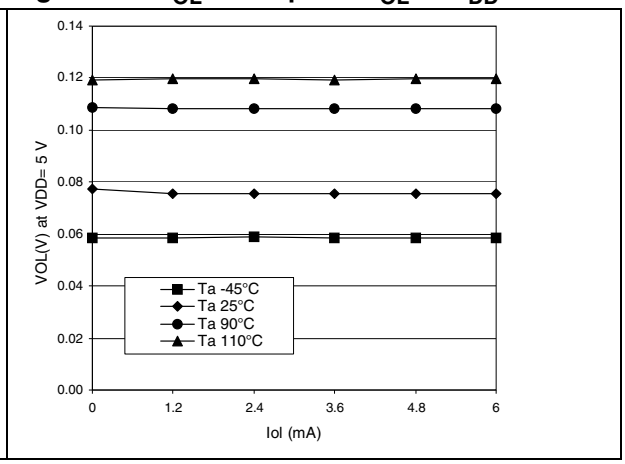


Figure 17. V_{OH} P6.0 pin vs I_{OL} @ V_{DD} 5 V

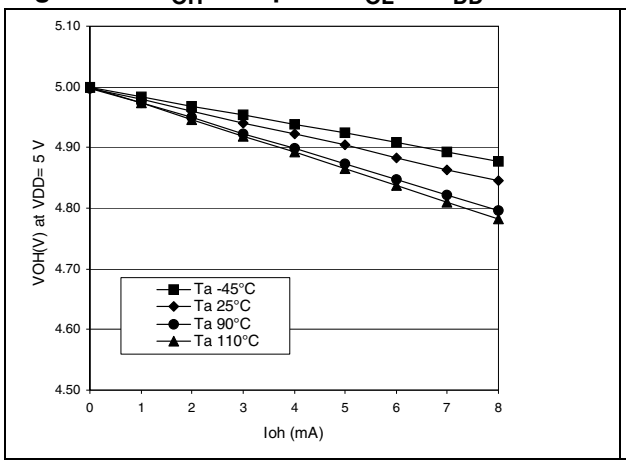
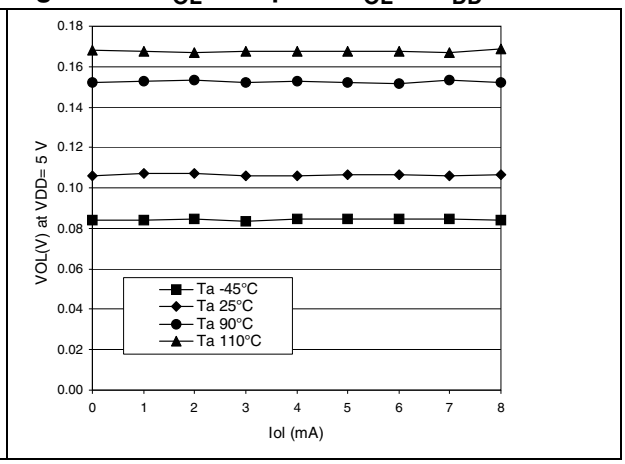


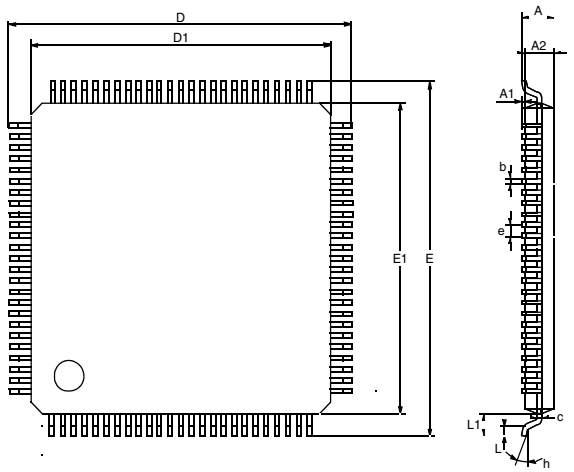
Figure 18. V_{OL} P6.0 pin vs I_{OL} @ V_{DD} 5 V



5 Package characteristics

5.1 Package mechanical data

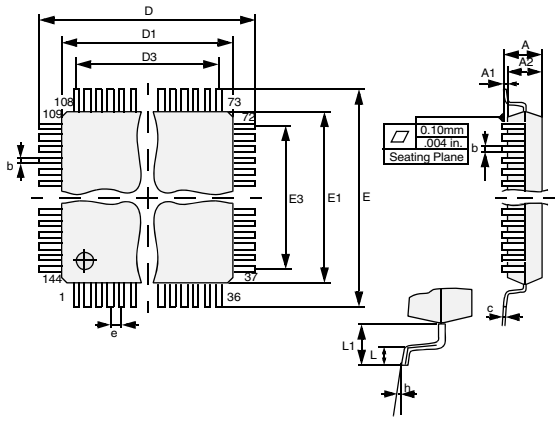
Figure 24. 100-pin thin quad flat package



Dim.	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A			1.60			0.0630
A1	0.05		0.15	0.0020		0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b	0.17	0.22	0.27	0.0067	0.0087	0.0106
C	0.09		0.20	0.0035		0.0079
D		16.00			0.6299	
D1		14.00			0.5512	
E		16.00			0.6299	
E1		14.00			0.5512	
e		0.50			0.0197	
h	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1		1.00			0.0394	
	Number of Pins					
N	100					

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 25. 144-pin thin quad flat package



Dim.	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A			1.60			0.0630
A1	0.05		0.15	0.0020		0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b	0.17	0.22	0.27	0.0067	0.0087	0.0106
c	0.09		0.20	0.0035		0.0079
D	21.80	22.00	22.20	0.8583	0.8661	0.8740
D1	19.80	20.00	20.20	0.7795	0.7874	0.7953
D3		17.50			0.6890	
E	21.80	22.00	22.20	0.8583	0.8661	0.8740
E1	19.80	20.00	20.20	0.7795	0.7874	0.7953
E3		17.50			0.6890	
e		0.50			0.0197	
K	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1		1.00			0.0394	
	Number of Pins					
N	144					

1. Values in inches are converted from mm and rounded to 4 decimal digits.

6 Order codes

Table 29. Order codes

Partnumber	Flash Kbytes	Package	RAM Kbytes	TIM timers	6x PWM module	CAN periph	A/D chan.	Wake-up lines	I/O ports	Temp. range
STR730FZ1T6	128	TQFP144 20x20	16	10	1	3	16	32	112	-40 to +85°C
STR730FZ2T6	256									
STR730FZ1H6	128	LFBGA144 10x10								
STR730FZ2H6	256									
STR735FZ1T6	128	TQFP144 20x20				0				
STR735FZ2T6	256									
STR735FZ1H6	128	LFBGA144 10x10								
STR735FZ2H6	256									
STR731FV0T6	64	TQFP100 14x14		6		3	12	18	72	
STR731FV1T6	128									
STR731FV2T6	256									
STR736FV0T6	64	TQFP100 14x14				0				
STR736FV1T6	128									
STR736FV2T6	256									
STR730FZ1T7	128	TQFP144 20x20	16	10	1	3	16	32	112	-40 to +105°C
STR730FZ2T7	256									
STR730FZ1H7	128	LFBGA144 10x10								
STR730FZ2H7	256									
STR735FZ1T7	128	TQFP144 20x20				0				
STR735FZ2T7	256									
STR735FZ1H7	128	LFBGA144 10x10								
STR735FZ2H7	256									
STR731FV0T7	64	TQFP100 14x14		6		3	12	18	72	
STR731FV1T7	128									
STR731FV2T7	256									
STR736FV0T7	64	TQFP100 14x14				0				
STR736FV1T7	128									
STR736FV2T7	256									

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