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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM7®
Core Size	32-Bit Single-Core
Speed	36MHz
Connectivity	CANbus, I²C, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	72
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/str731fv1t7

Contents

2 Overview

Table 2. Product overview

Features	STR730FZx		STR735FZx		STR731FVx			STR736FVx		
Flash memory - bytes	128K	256K	128K	256K	64K	128K	256K	64K	128K	256K
RAM - bytes	16 K				16 K					
Peripheral functions	10 TIM timers, 112 I/Os, 32 wake-up lines, 16 ADC				6 TIM timers, 72 I/Os, 18 wake-up lines, 12 ADC channels					
CAN peripherals	3		0		3			0		
Operating voltage	4.5 to 5.5 V									
Operating temperature	-40 to +85°C/-40 to +105° C									
Packages	**T**=TQFP144 20 x 20 **H**=LFBGA144 10 x10				**T**=TQFP100 14x14					

Package choice: reduced pin-count TQFP100 or feature-rich 144-pin TQFP or LFBGA

The STR73xF family is available in 3 packages. The TQFP144 and LFBGA144 versions have the full set of all features. The 100-pin version has fewer timers, I/Os and ADC channels. Refer to the Device Summary on Page 1 for a comparison of the I/Os available on each package.

The family includes versions with and without CAN.

High speed Flash memory

The Flash program memory is organized in 32-bit wide memory cells which can be used for storing both code and data constants. It is accessed by CPU with zero wait states @ 36 MHz.

The STR7 embedded Flash memory can be programmed using in-circuit programming or in-application programming.

The Flash memory endurance is 10K write/erase cycles and the data retention is 20 years @ 85° C.

IAP (in-application programming): IAP is the ability to re-program the Flash memory of a microcontroller while the user program is running.

ICP (in-circuit programming): ICP is the ability to program the Flash memory of a microcontroller using JTAG protocol while the device is mounted on the user application board.

The Flash memory can be protected against different types of unwanted access (read/write/erase). There are two types of protection:

- Sector write protection
- Flash debug protection (locks JTAG access)

Flexible power management

To minimize power consumption, you can program the STR73xF to switch to SLOW, WFI LPWFI, STOP or HALT modes depending on the current system activity in the application.

Flexible clock control

Two clock sources are used to drive the microcontroller, a main clock driven by an external crystal or ceramic resonator and an internal backup RC oscillator that operates at 2 MHz or 32 kHz. The embedded PLL can be configured to generate an internal system clock of up to 36 MHz. The PLL output frequency can be programmed using a wide selection of multipliers and dividers.

Voltage regulators

The STR73xF requires an external 4.5 to 5.5 V power supply. There are two internal Voltage Regulators for generating the 1.8 V power supply needed by the core and peripherals. The main VR is switched off and the Low Power VR switched on when the application puts the STR73xF in Low Power Wait for Interrupt (LPWFI) mode.

Low voltage detectors

The voltage regulator and Flash modules each have an embedded LVD that monitors the internal 1.8 V supply. If the voltage drops below a certain threshold, the LVD will reset the STR73xF.

Note: An external power-on reset must be provided ensure the microcontroller starts-up correctly.

2.1 On-chip peripherals

CAN interfaces

The three CAN modules are compliant with the CAN specification V2.0 part B (active). The bit rate can be programmed up to 1 MBaud. These are not available in the STR735 and STR736.

DMA

4 DMA controllers, each with 4 data streams manage memory to memory, peripheral to peripheral, peripheral to memory and memory to peripheral transfers. The DMA requests are connected to TIM timers, BSPI0, BSPI1, BSPI2 and ADC. One of the streams can be configured to be triggered by a software request, independently from any peripheral activity.

16-bit timers (TIM)

Each of the ten timers (six in 100-pin devices) have a 16-bit free-running counter with 7-bit prescaler, up to two input capture/output compare functions, a pulse counter function, and a PWM channel with selectable frequency. This provides a total of 16 independent PWMs (12 in 100-pin devices) when added with the PWM modules (see next paragraph).

PWM modules (PWM)

The six 16-bit PWM modules have independently programmable periods and duty-cycles, with 5+3 bit prescaler factor.

Timebase timers (TB)

The three 16-bit timebase timers with 8-bit prescaler for general purpose time triggering operations.

Real-time clock (RTC)

The RTC provides a set of continuously running counters driven by separate clock signal derived from the main oscillator. The RTC can be used as a general timebase or

3 Block diagram

Figure 1. STR730F/STR735F block diagram

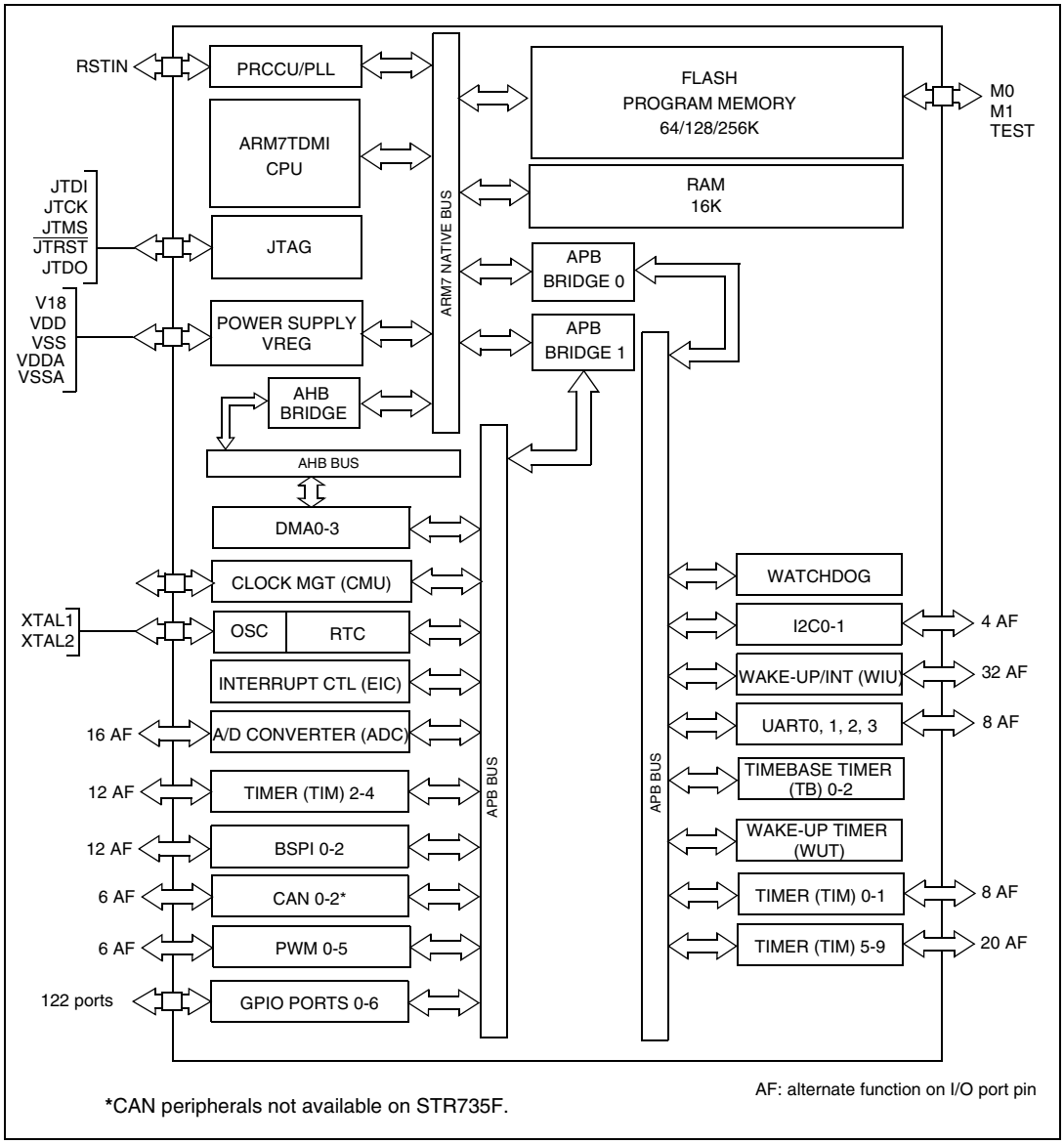
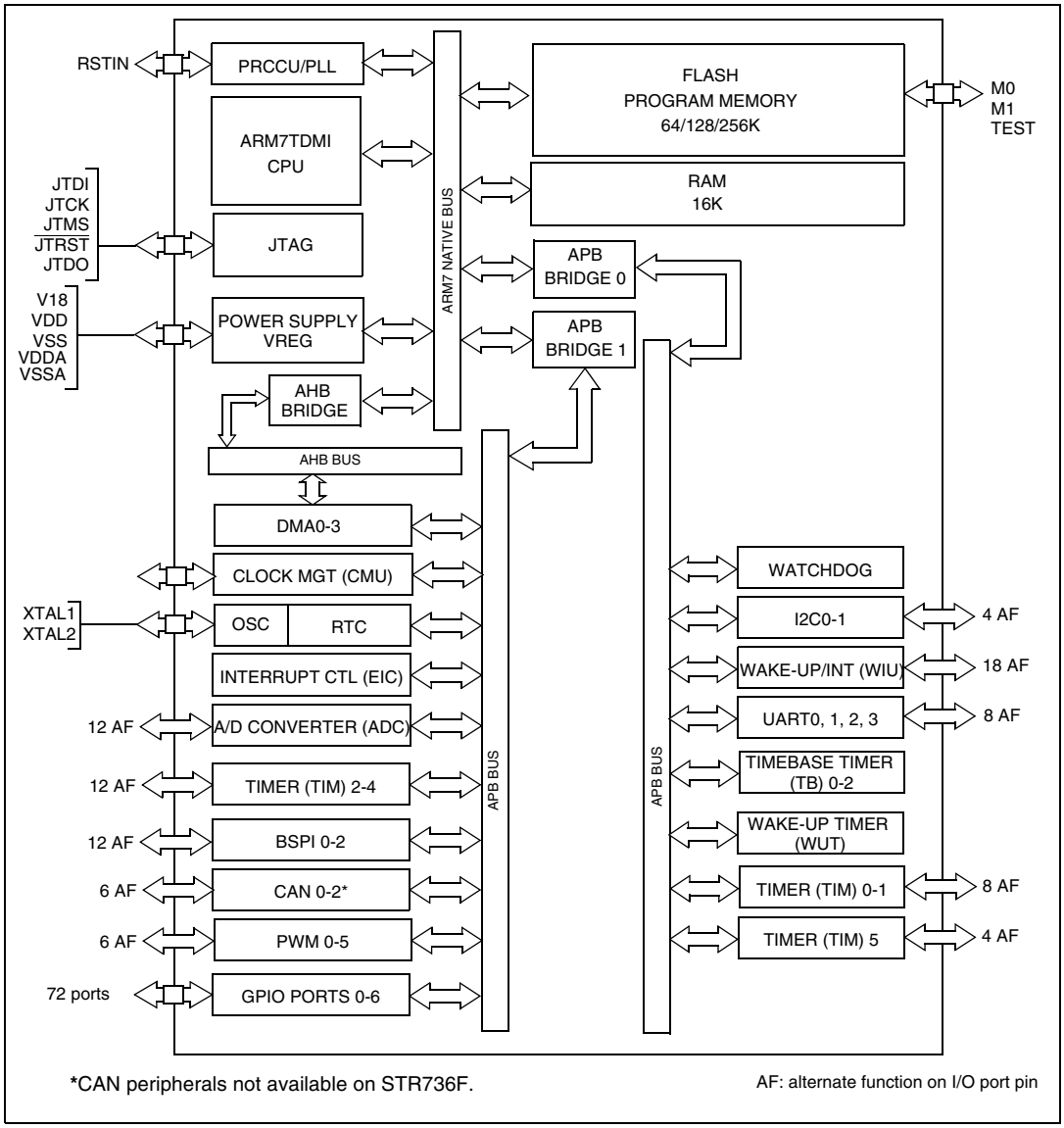


Figure 2. STR731F/STR736 block diagram



*CAN peripherals not available on STR736F.

AF: alternate function on I/O port pin

3.2.2 STR730F/STR735F (LFBGA144)

Table 3. STR730F/STR735F LFBGA ball connections

Ball	Name	Ball	Name	Ball	Name	Ball	Name
A1	P0.0 / OCMPB2	B1	P0.4 / OCMPA5	C1	P0.5 / OCMPB5	D1	V_{SS}
A2	P6.10 / WUP8	B2	P0.1 / OCMPA2	C2	P0.2 / ICAPA2	D2	V_{DD}
A3	P6.9 / TDO0	B3	P6.15 / WUP9	C3	P0.3 / ICAPB2	D3	P0.6 / ICAPA5
A4	P6.12 / MOSI0	B4	P6.13 / SCKO / WUP11	C4	P6.14 / SSO	D4	P0.7 /ICAPB5
A5	P6.6 / WUP6	B5	P6.7 / WUP7	C5	P6.8 / RDI0 / WUP10	D5	P6.11 / MISO0
A6	V_{18}	B6	P6.2 / WUP2 / RDI3	C6	P6.3 / WUP3	D6	P6.4 / WUP4 /TDO3
A7	P5.15 / INT13	B7	P5.14 / INT12	C7	V_{SS}	D7	VDD
A8	P5.8 / INT6	B8	P5.9 / INT7	C8	P5.10 / INT8 / RDI2	D8	P5.12 / INT10
A9	P5.2 / OCMPA9	B9	P5.3 / OCMPB9	C9	P5.4 / SS2	D9	P5.5 / SCK2 / WUP23
A10	P5.7 / MISO2	B10	P5.0 / MOSI1	C10	P5.1 / MISO1	D10	P4.13 / ICAPB9
A11	P5.6 / MOSI2	B11	P4.15 / SCK1 / WUP22	C11	P4.14 / SS1	D11	P4.12 / ICAPA9 / WUP21
A12	P5.11 / TDO2 / INT9	B12	P4.8 / OCMPA8	C12	P4.7 / SDA1	D12	P4.11 / OCMPB8
E1	P0.8 / OCMPA6	F1	V_{DD}	G1	V_{SS}	H1	V_{DD}
E2	P0.9 / OCMPB6	F2	P0.13 / ICAPB3	G2	P1.2 / ICAPB4	H2	P1.8 / OCMPA0 / INT0
E3	P0.10 / OCMPA7	F3	P0.14 / OCMPB3	G3	P1.3 / ICAPA4	H3	P1.9 / OCMPB0 / INT1
E4	P0.11 / OCMPB7	F4	P0.15 / OCMPA3	G4	V_{SS}	H4	P1.10 / ICAPB0 / WUP28
E5	P0.12 / ICAPA3	F5	P1.0 / OCMPA4	G5	P1.5	H5	XTAL2
E6	P6.5 / WUP5	F6	P1.1 / OCMPB4	G6	P2.11 / WUP17	H6	P2.10 / WUP16
E7	P6.0 / WUP0	F7	P6.1 / WUP1	G7	P4.0 / ICAPA7 / WUP24	H7	P2.15 / SDA 0
E8	P5.13 / INT11	F8	P4.4 / CAN2TX[1)]	G8	VDD	H8	JTMS
E9	P4.10 / ICAPA6 / WUP20	F9	P4.3 / ICAPB8 / WUP27	G9	VSS	H9	VSS
E10	P4.9 / ICAPB6	F10	P4.2 / ICAPA8 / WUP26	G10	JTDO	H10	VDD
E11	P4.6 / SCL1 / WUP19	F11	P4.1 / ICAPB7 / WUP25	G11	JTCK	H11	P3.15 / AIN15 / INT5
E12	P4.5 / WUP18 / CAN2RX[1)]	F12	JTDI	G12	nJTRST	H12	P3.14 / AIN14 / INT4
J1	P1.4	K1	P1.6 / OCMPB1	L1	P1.7 / OCMPA1	M1	P1.14 / CAN0RX[1)] / WUP12
J2	P1.11 / ICAPA0 / WUP29	K2	P1.13 / ICAPB1 / WUP31	L2	P1.15 / CAN0TX[1)]	M2	P2.4 / PWM2
J3	P1.12 / ICAPA1 / WUP30	K3	P2.1 / CAN1RX[1)] / WUP13	L3	P2.0 / PWM0	M3	P2.5 / PWM3
J4	P2.7 / PWM5	K4	P2.6 / PWM4	L4	P2.3 / PWM1	M4	P2.2 / CAN1TX[1)]
J5	V_{DD}	K5	M1	L5	RSTIN	M5	M0
J6	P2.9 / RDI1 / WUP14	K6	P2.8 / TDO1	L6	V_{SS}	M6	V_{SS}
J7	P2.14 / SCL 0 / WUP15	K7	P2.13 / INT15	L7	P2.12 / INT14	M7	XTAL1
J8	P3.1 / AIN1	K8	P3.0 / AIN0	L8	VBIAS	M8	TST
J9	P3.13 / AIN13 / INT3	K9	P3.4 / AIN4	L9	P3.3 / AIN3	M9	P3.2 / AIN2
J10	P3.12 / AIN12 / INT2	K10	V_{DDA}	L10	P3.5 / AIN5	M10	V_{SS}
J11	P3.9 / AIN9	K11	V_{SSA}	L11	P3.7 / AIN7	M11	V_{DD}
J12	P3.8 / AIN8	K12	P3.11 / AIN11	L12	P3.10 / AIN10	M12	P3.6 / AIN6

Note: CAN alternate functions not available on STR735F.

Legend / Abbreviations for *Table 4*:

Type: I = input, O = output, S = supply, HiZ= high impedance,

In/Output level: T_T= TTL 0.8 V / 2 V with input trigger
C_T= CMOS $0.3V_{DD}/0.7V_{DD}$ with input trigger

Port and control configuration:

Input: pu/pd = with internal 100 kΩ weak pull-up or pull down

Output: OD = open drain (logic level)
PP = push-pull

Interrupts:

INTx = external interrupt line

WUPx = wake-up interrupt line

The reset state (during and just after the reset) of the I/O ports is input floating (Input tristate TTL mode). To avoid excess power consumption, unused I/O ports must be tied to ground.

Table 4. STR73xF pin description

Pin n°			Pin name	Type	Input			Output			Main function (after reset)	Alternate function
TQFP144	LFBGA144	TQFP100			Input Level	pu/pd	interrupt	Capability	OD	PP		
1	A1	1	P0.0/OCMPB2	I/O	T_T			2mA	X	X	Port 0.0	TIM2: output compare B output
2	B2	2	P0.1/OCMPA2	I/O	T_T			2mA	X	X	Port 0.1	TIM2: output compare A output
3	C2	3	P0.2/ICAPA2	I/O	T_T			2mA	X	X	Port 0.2	TIM2: input capture A input
4	C3	4	P0.3/ICAPB2	I/O	T_T			2mA	X	X	Port 0.3	TIM2: input capture B input
5	D1		V_{SS}	S							Ground	
6	D2		V_{DD}	S							Supply voltage (5 V)	
7	B1	5	P0.4/OCMPA5	I/O	T_T			2mA	X	X	Port 0.4	TIM5: output compare A output
8	C1	6	P0.5/OCMPB5	I/O	T_T			2mA	X	X	Port 0.5	TIM5: output compare B output
9	D3	7	P0.6/ICAPA5	I/O	T_T			2mA	X	X	Port 0.6	TIM5: input capture A input
10	D4		P0.7/ICAPB5	I/O	T_T			2mA	X	X	Port 0.7	TIM5: input capture B input
11	E1		P0.8/OCMPA6	I/O	T_T			2mA	X	X	Port 0.8	TIM6: output compare A output
12	E2		P0.9/OCMPB6	I/O	T_T			2mA	X	X	Port 0.9	TIM6: output compare B output
13	E3		P0.10/OCMPA7	I/O	T_T			2mA	X	X	Port 0.10	TIM7: output compare A output
14	E4		P0.11/OCMPB 7	I/O	T_T			2mA	X	X	Port 0.11	TIM7: output compare B output
15	F1	8	V_{DD}	S							Supply voltage (5 V)	
16	G1	9	V_{SS}	S							Ground	
17	E5	10	P0.12/ICAPA3	I/O	T_T			2mA	X	X	Port 0.12	TIM3: input capture A input
18	F2	11	P0.13/ICAPB3	I/O	T_T			2mA	X	X	Port 0.13	TIM3: input capture B input

Table 4. STR73xF pin description

Pin n°			Pin name	Type	Input			Output			Main function (after reset)	Alternate function	
TQFP144	LFBGA144	TQFP100			Input Level	pu/pd	interrupt	Capability	OD	PP			
50	J5	36	V_{DD}	S							Supply voltage (5 V)		
51	M6	37	V_{SS}	S							Ground		
52	M7	38	XTAL1	I							Oscillator amplifier circuit input and internal clock generator input.		
53	H5	39	XTAL2	O							Oscillator amplifier circuit output.		
54	L6	40	V_{SS}	S							Ground		
55	K6	41	P2.8/TDO1/CAN2RX	I/O	T_T			2mA	X	X	Port 2.8	UART1: transmit data output	CAN2: receive data input (TQFP100 only)
56	J6	42	P2.9/RDI1/CAN2TX	I/O	T_T		WUP14	2mA	X	X	Port 2.9	UART1: receive data input	CAN2: transmit data output (TQFP100 only)
57	H6		P2.10	I/O	T_T		WUP16	2mA	X	X	Port 2.10		
58	G6		P2.11	I/O	T_T		WUP17	2mA	X	X	Port 2.11		
59	L7		P2.12	I/O	T_T		INT14	2mA	X	X	Port 2.12		
60	K7		P2.13	I/O	T_T		INT15	2mA	X	X	Port 2.13		
61	J7	43	P2.14/SCL0	I/O	T_T		WUP15	2mA	X	X	Port 2.14	I2C0: serial clock	
62	H7	44	P2.15/SDA0	I/O	T_T			2mA	X	X	Port 2.15	I2C0: serial data	
63	M8	45	Test	I		pd					Reserved pin. Must be tied to ground		
64	L8	46	V_{BIAS}	S							Internal RC oscillator bias. A 1.3 MΩ external resistor has to be connected to this pin when a 32 kHZ RC oscillator frequency is used.		
65	M10	47	V_{SS}	S							Ground		
66	M11	48	V_{DD}	S							Supply voltage (5 V)		
67	K8		P3.0/AIN0	I/O	T_T			2mA	X	X	Port 3.0	ADC: analog input 0	
68	J8		P3.1/AIN1	I/O	T_T			2mA	X	X	Port 3.1	ADC: analog input 1	
69	M9		P3.2/AIN2	I/O	T_T			2mA	X	X	Port 3.2	ADC: analog input 2	
70	L9		P3.3/AIN3	I/O	T_T			2mA	X	X	Port 3.3	ADC: analog input 3	
71	K9	49	P3.4/AIN4	I/O	T_T			2mA	X	X	Port 3.4	ADC: analog input 4 (AIN0 in TQFP100)	
72	L10	50	P3.5/AIN5	I/O	T_T			2mA	X	X	Port 3.5	ADC: Analog input 5 (AIN1 in TQFP100)	

Table 4. STR73xF pin description

Pin n°			Pin name	Type	Input			Output			Main function (after reset)	Alternate function
TQFP144	LFBGA144	TQFP100			Input Level	pu/pd	interrupt	Capability	OD	PP		
119	B8	84	P5.9/PWM5	I/O	T_T		INT7	2mA	X	X	Port 5.9	PWM5: PWM output (TQFP100 only)
120	C8	85	P5.10/RDI2	I/O	T_T		INT8	2mA	X	X	Port 5.10	UART2: receive data input
121	A12	86	P5.11/TDO2	I/O	T_T		INT9	2mA	X	X	Port 5.11	UART2: transmit data output
122	D8	87	P5.12	I/O	T_T		INT10	2mA	X	X	Port 5.12	
123	E8		P5.13	I/O	T_T		INT11	2mA	X	X	Port 5.13	
124	B7		P5.14	I/O	T_T		INT12	2mA	X	X	Port 5.14	
125	A7		P5.15	I/O	T_T		INT13	2mA	X	X	Port 5.15	
126	A6	88	V_{18}	S								1.8 V decoupling pin: a decoupling capacitor (recommended value: 100 nF) must be connected between this pin and nearest VSS pin.
127	C7	89	V_{SS}	S								Ground
128	D7	90	V_{DD}	S								Supply voltage (5 V)
129	E7	91	P6.0	I/O	T_T		WUP0	8mA	X	X	Port 6.0	
130	F7		P6.1	I/O	T_T		WUP1	2mA	X	X	Port 6.1	
131	B6	92	P6.2/RDI3	I/O	T_T		WUP2	2mA	X	X	Port 6.2	UART3: receive data input
132	C6		P6.3	I/O	T_T		WUP3	2mA	X	X	Port 6.3	
133	D6	93	P6.4/TDO3	I/O	T_T		WUP4	2mA	X	X	Port 6.4	UART3: transmit data output
134	E6		P6.5	I/O	T_T		WUP5	2mA	X	X	Port 6.5	
135	A5	94	P6.6	I/O	T_T		WUP6	2mA	X	X	Port 6.6	
136	B5		P6.7	I/O	T_T		WUP7	2mA	X	X	Port 6.7	
137	C5	95	P6.8/RDI0	I/O	T_T		WUP10	2mA	X	X	Port 6.8	UART0: receive data input
138	A3	96	P6.9/TDO0	I/O	T_T			2mA	X	X	Port 6.9	UART0: transmit data output
139	A2		P6.10	I/O	T_T		WUP8	2mA	X	X	Port 6.10	
140	D5	97	P6.11/MISO0	I/O	T_T			2mA	X	X	Port 6.11	BSPI0: master input/slave output
141	A4	98	P6.12/MOSI0	I/O	T_T			2mA	X	X	Port 6.12	BSPI0: master output/slave input
142	B4	99	P6.13/SCK0	I/O	T_T		WUP11	2mA	X	X	Port 6.13	BSPI0: serial clock
143	C4	100	P6.14/$\overline{SS}$0	I/O	T_T			2mA	X	X	Port 6.14	BSPI0: slave select
144	B3		P6.15	I/O	T_T		WUP9	2mA	X	X	Port 6.15	

4.3.1 Supply current characteristics

The current consumption is measured as described in *Figure 6* and *Figure 7*.

Total current consumption

The MCU is placed under the following conditions:

- All I/O pins in input mode with a static value at V_{DD} or V_{SS} (no load)
- All peripherals are disabled except if explicitly mentioned.

Subject to general operating conditions for V_{DD}, and T_A.

Table 10. Total current consumption

Symbol	Parameter	Conditions	Typ [1]	Max [2]	Unit
I_{DD}	RUN mode[3]	Formula, f_{MCLK} in MHz, RAM execution	7 + 1.9 f_{MCLK}		mA
		f_{MCLK} = 36 MHz, RAM execution	76		mA
		f_{MCLK} = 36 MHz, Flash execution	86		mA
	WFI mode	f_{OSC} = 4 MHz, f_{MCLK}= f_{OSC}/16 = 250 kHz Main voltage regulator ON, LP voltage regulator = 2 mA, RTC and WDG on, other modules off.	6.7	8	mA
	LPWFI mode	f_{RC} = high frequency (CMU_RCCTL= 0x8), f_{MCLK}= f_{RC} /16, LP voltage regulator = 2 mA, other modules off.	220	350	µA
	STOP mode	f_{OSC} = 4 MHz, RC oscillator on f_{RC} = high frequency (CMU_RCCTL= 0x0) LP voltage regulator = 6 mA, RTC and WUT ON, other modules off. Internal wake-up possible.	500	700	µA
		f_{RC} = high frequency (CMU_RCCTL= 0xF), LP voltage regulator = 2mA. WUT ON, other modules off. Internal wake-up possible.	150	220	
		LP voltage regulator = 2 mA, WIU on, Other modules off, external wake-up.	50	140	
	HALT mode	LP voltage regulator = 2 mA.	50	140	µA

1. Typical data are based on T_A=25° C, V_{DD}=5 V
2. Data based on characterization results, tested in production at V_{DD} max. and T_A = 25° C.
3. I/O in static configuration (not toggling). RUN mode is almost **independent of temperature**. On the contrary RUN mode current is **highly dependent on the application**. The I_{DDRUN} value can be significantly reduced by the application in the following ways: switch-off unused peripherals (default), reduce peripheral frequency through internal prescaler, fetch the most frequently-used functions from RAM and use low power mode when possible.

Figure 8. STOP I_{DD} vs. VDD

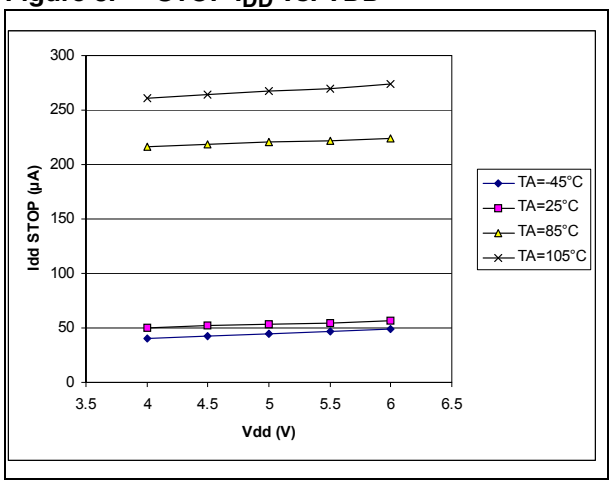


Figure 9. HALT I_{DD} vs. V_{DD}

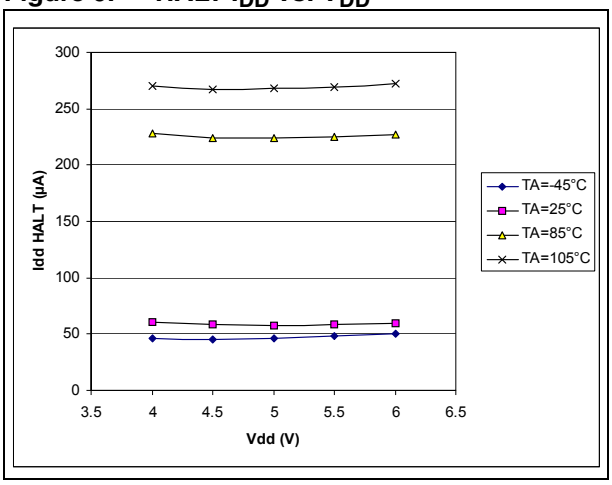


Figure 10. WFI I_{DD} vs. V_{DD}

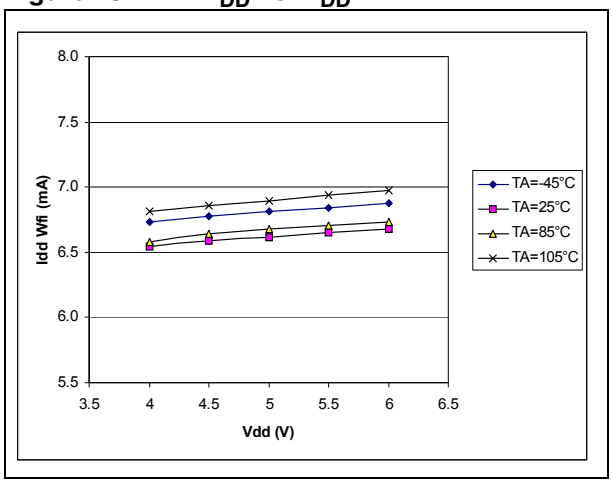
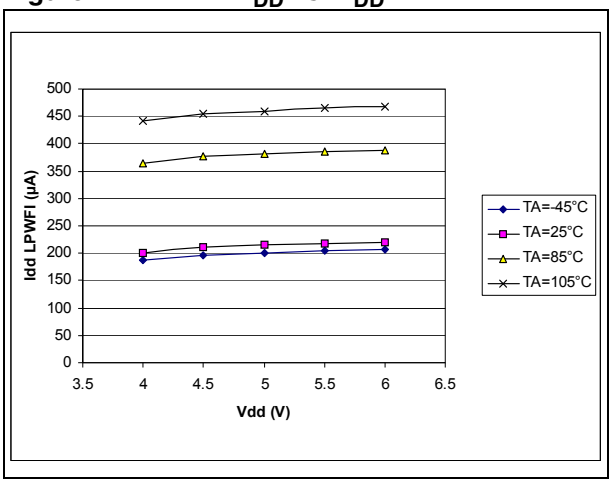


Figure 11. LPWFI I_{DD} vs. V_{DD}



PLL electrical characteristics

V_{DD} = 5 V ± 10%, T_A = -40° C to T_{Amax}, unless otherwise specified

Table 16. PLL characteristics

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
f_{PLLIN} (1)	PLL reference clock	FREF_RANGE = '0' FREF_RANGE = '1'	1.5 3.0		3.0 5.0	MHz
f_{PLLOUT}	PLL output clock	MX = "00" MX = "01" MX = "10" MX = "11"	20 x f_{PLLIN} 12 x f_{PLLIN} 28 x f_{PLLIN} 16 x f_{PLLIN}			MHz
f_{MCLK}	System clock	DX = 1..7	f_{PLLOUT}/DX		36	MHz
f_{FREE} (2)	PLL free running frequency	FREF_RANGE = '0', MX0 = '1' FREF_RANGE = '0', MX0 = '0' FREF_RANGE = '1', MX0 = '1' FREF_RANGE = '1', MX0 = '0'		120 240 240 480		kHz
t_{LOCK} (3)	PLL lock time	Stable oscillator (f_{PLLIN} = 4 MHz), stable V_{DD}		100	300	µs
Δt_{PKJIT}	PLL jitter (pk to pk)	f_{PLLIN} = 4 MHz (pulse generator)			1.5	ns

1. f_{PLLIN} is obtained from f_{OSC} directly or through an optional divider by 2.
2. Typical data are based on T_A=25°C, V_{DD}=5V
3. Max value is guaranteed by characterization, not tested in production.

Table 17. Low-power mode wake-up timing

Symbol	Parameter	Conditions	Typ	Unit
t_{WUHALT}	Wake-up from HALT mode		200	µs
t_{WUSTOP}	Wake-up from STOP mode	RC high frequency in STOP mode	180	µs
		RC low frequency in STOP mode	234	µs
$t_{WULPWFI}$ 1)	Wake-up from LPWFI mode	Main voltage regulator on RC oscillator off f_{OSC} = 4 MHz, f_{MCLK}= f_{OSC}/16 RAM or FLASH execution	27	µs
		Main voltage regulator on RC oscillator = high frequency Flash execution	46	µs
		Main voltage regulator on RC oscillator = low frequency Flash execution	3.6	ms

1. Flash memory programmed to enter Power Down mode during LPWFI.

4.3.3 Memory characteristics

Flash memory

Table 18. Flash memory characteristics

Symbol	Parameter	Test Conditions	Value			Unit
			Min	Typ	Max[1)]	
t_{WP}	Word program (32-bit)			35	80	µs
t_{DWP}	Double word program(64-bit)			64	150	µs
t_{BP64}	Bank program (64 K)	Double word program		0.5	1.25	s
t_{BP128}	Bank program (128 K)	Double word program		1	2.5	s
t_{BP256}	Bank program (256 K)	Double word program		2	4.9	s
t_{SE8}	Sector erase (8 K)	Not preprogrammed Preprogrammed [2)]		0.6 0.5	0.9 0.8	s
t_{SE32}	Sector erase (32 K)	Not preprogrammed Preprogrammed[2)]		1.1 0.8	2 1.8	s
t_{SE64}	Sector erase (64 K)	Not preprogrammed preprogrammed [2)]		1.7 1.3	3.7 3.3	s
t_{RPD}[3)]	Recovery from power-down				20	µs
t_{PSL}[3)]	Program suspend latency				10	µs
t_{ESL}[3)]	Erase suspend latency				30	µs
t_{ESR}[3)]	Erase suspend rate	Min. time from erase resume to next erase suspend		20	20	ms
t_{SP}[3)]	Set protection			40	170	µs
t_{FPW}[3)]	First word program			1		ms
N_{END}	Endurance		10			kcycles
t_{RET}	Data retention	T_A = 85° C	20			Years

1. T_A = -45° C after 0 cycles, Guaranteed by characterization, not tested in production.
2. All bits programmed to 0.
3. Guaranteed by design, not tested in production.

Output driving current

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified.

Table 24. Output driving current

I/O Type	Symbol	Parameter	Conditions	Min	Max	Unit
Standard	V_{OL} 1)	Output low level voltage for an I/O pin when 8 pins are sunk at same time	I_{IO}=+2 mA		0.4	V
	V_{OH} 2)	Output high level voltage for an I/O pin when 4 pins are sourced at same time	I_{IO}=-2 mA	V_{DD}-0.8		
Med. Current (JTDO)	V_{OL} 1)	Output low level voltage for an I/O pin	I_{IO}=+6 mA		0.4	
	V_{OH} 2)	Output high level voltage for an I/O pin	I_{IO}=-6 mA	V_{DD}-0.8		
High Current P6.0	V_{OL} 1)	Output low level voltage for an I/O pin	I_{IO}=+8 mA		0.4	
	V_{OH} 2)	Output high level voltage for an I/O pin	I_{IO}=-8 mA	V_{DD}-0.8		

1. The I_{IO} current sunk must always respect the absolute maximum rating specified in *Table 6* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
2. The I_{IO} current sourced must always respect the absolute maximum rating specified in *Table 6* and the sum of I_{IO} (I/O ports and control pins) must not exceed IV_{DD}.

Figure 13. V_{OH} standard ports vs I_{OH} @ V_{DD} 5V T_A -45° C

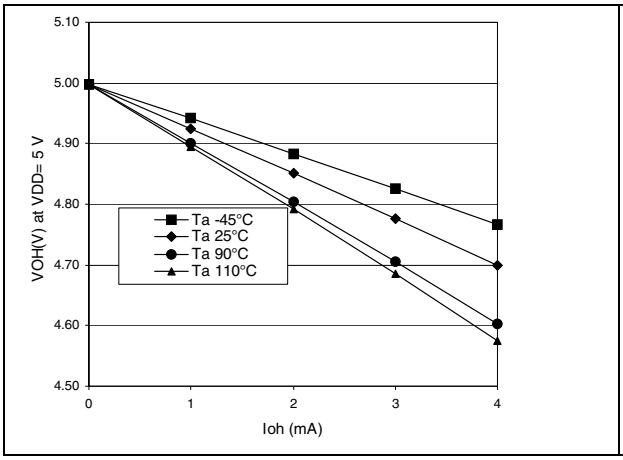


Figure 14. V_{OL} standard ports vs I_{OL} @ V_{DD} 5 V

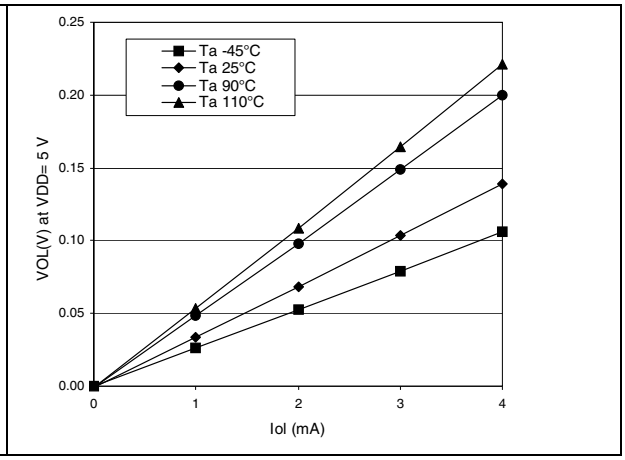


Figure 15. V_{OH} JTDO pin vs I_{OL} @ V_{DD} 5 V

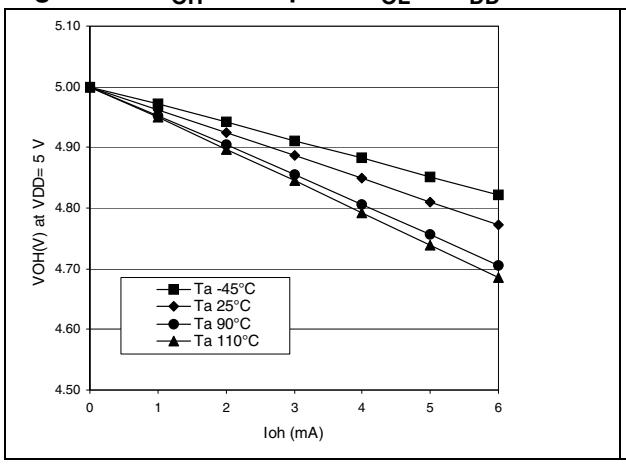


Figure 16. V_{OL} JTDO pin vs I_{OL} @ V_{DD} 5 V

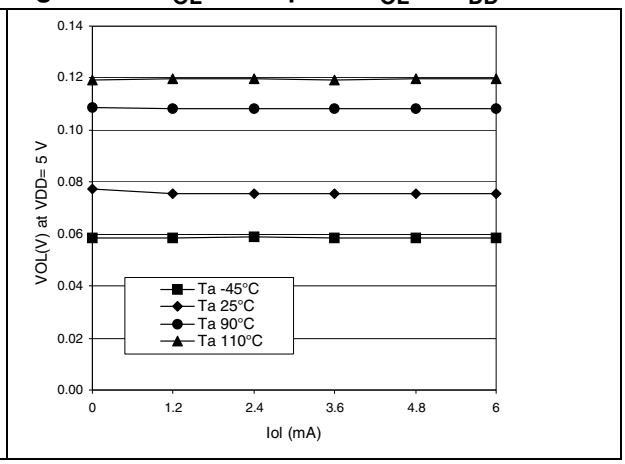


Figure 17. V_{OH} P6.0 pin vs I_{OL} @ V_{DD} 5 V

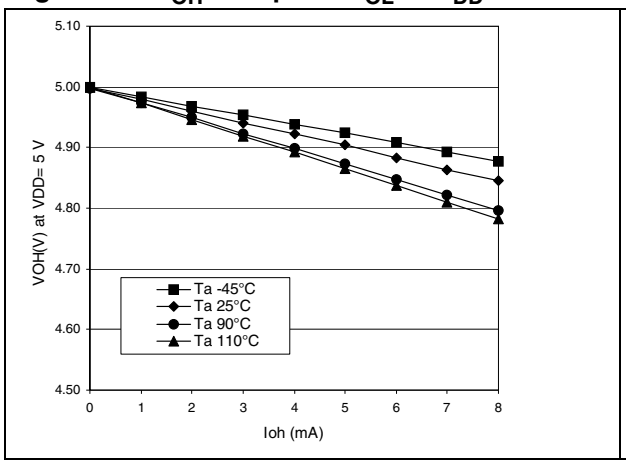


Figure 18. V_{OL} P6.0 pin vs I_{OL} @ V_{DD} 5 V

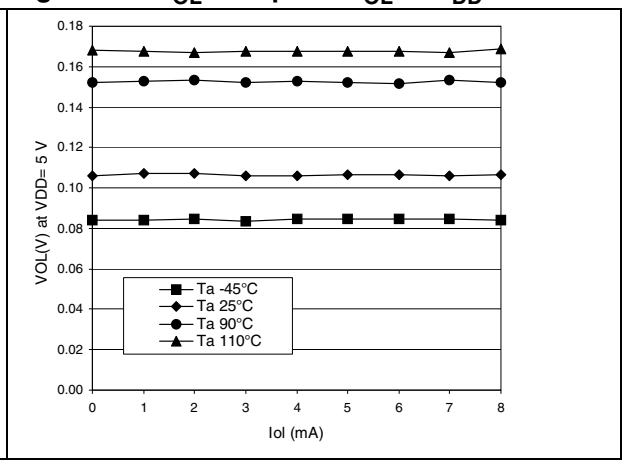


Table 27. ADC accuracy with f_{MCLK} = 20 MHz, f_{ADC}=10 MHz, R_{AIN} < 10 kΩ RAIN, V_{DDA}=5 V. This assumes that the ADC is calibrated[2)]

Symbol	Parameter	Conditions	Typ	Max	Unit
$\|E_T\|$	Total unadjusted error [1)]		1.0	2.0	LSB
$\|E_O\|$	Offset error [1)]		0.15	1.0	
$\|E_G\|$	Gain error [1)]		0.97	1.1	
$\|E_D\|$	Differential linearity error[1)]		0.7	1.0	
$\|E_L\|$	Integral linearity error [1)]		0.76	1.5	

1. ADC accuracy vs. negative injection current: Injecting negative current on any of the standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current. The effect of negative injection current on robust pins is specified in *Section 4.3.5*.
   Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 4.3.5* does not affect the ADC accuracy.
2. Calibration is needed once after each power-up.

Figure 21. ADC accuracy characteristics

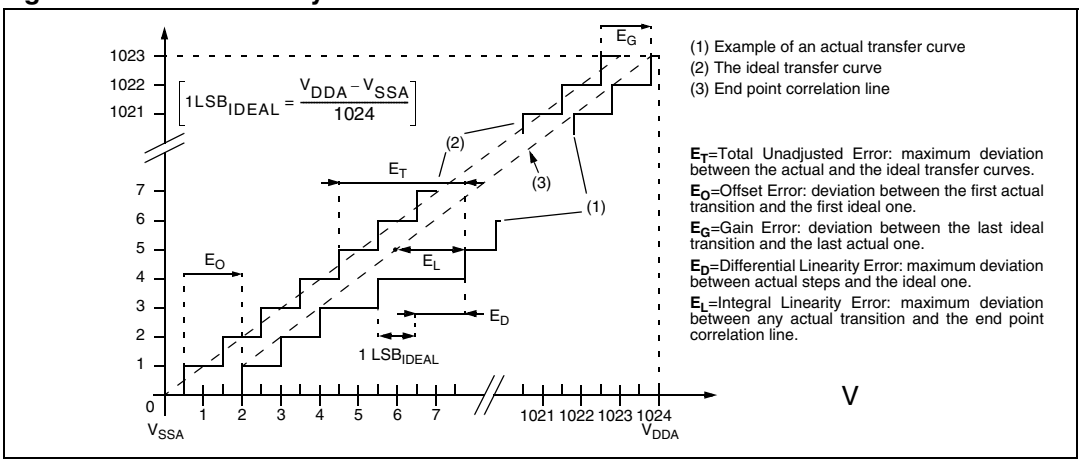
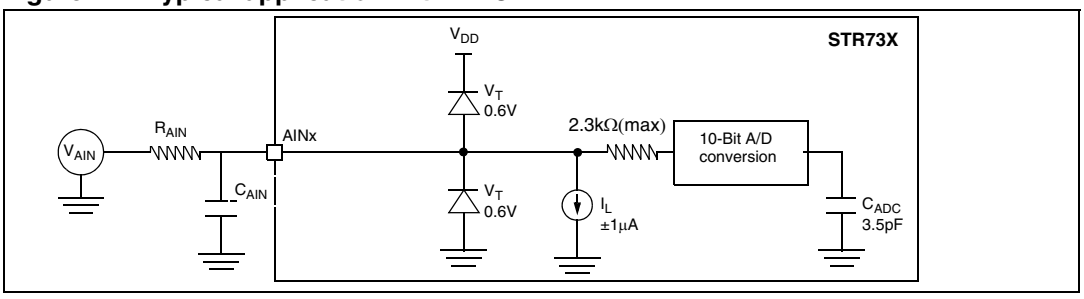


Figure 22. Typical application with ADC



Analog power supply and reference pins

The V_{DDA} and V_{SSA} pins are the analog power supply of the A/D converter cell. They act as the high and low reference voltages for the conversion.

Separation of the digital and analog power pins allow board designers to improve A/D performance. Conversion accuracy can be impacted by voltage drops and noise in the event of heavily loaded or badly decoupled power supply lines (see*: General PCB design guidelines*).

General PCB design guidelines

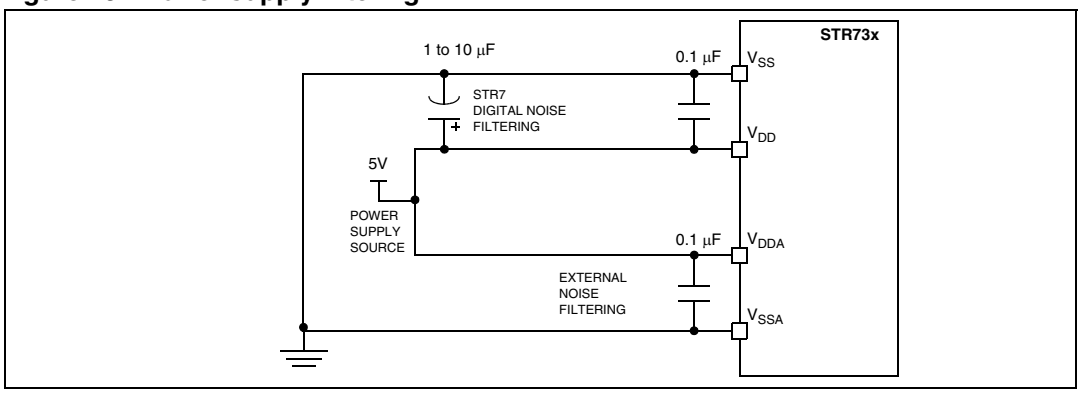
To obtain best results, some general design and layout rules should be followed when designing the application PCB to shield the noise-sensitive, analog physical interface from noise-generating CMOS logic signals.

- Use separate digital and analog planes. The analog ground plane should be connected to the digital ground plane via a single point on the PCB.
- Filter power to the analog power planes. It is recommended to connect capacitors, with good high frequency characteristics, between the power and ground lines, placing 0.1 µF and optionally, if needed 10 pF capacitors as close as possible to the STR7 power supply pins and a 1 to 10 µF capacitor close to the power source (see *Figure 23*).
- The analog and digital power supplies should be connected in a star network. Do not use a resistor, as V_{DDA} is used as a reference voltage by the A/D converter and any resistance would cause a voltage drop and a loss of accuracy.
- Properly place components and route the signal traces on the PCB to shield the analog inputs. Analog signals paths should run over the analog ground plane and be as short as possible. Isolate analog signals from digital signals that may switch while the analog inputs are being sampled by the A/D converter. Do not toggle digital outputs near the A/D input being converted.

Software filtering of spurious conversion results

For EMC performance reasons, it is recommended to filter A/D conversion outliers using software filtering techniques.

Figure 23. Power supply filtering



6 Order codes

Table 29. Order codes

Partnumber	Flash Kbytes	Package	RAM Kbytes	TIM timers	6x PWM module	CAN periph	A/D chan.	Wake-up lines	I/O ports	Temp. range
STR730FZ1T6	128	TQFP144 20x20	16	10	1	3	16	32	112	-40 to +85°C
STR730FZ2T6	256									
STR730FZ1H6	128	LFBGA144 10x10								
STR730FZ2H6	256									
STR735FZ1T6	128	TQFP144 20x20				0				
STR735FZ2T6	256									
STR735FZ1H6	128	LFBGA144 10x10								
STR735FZ2H6	256									
STR731FV0T6	64	TQFP100 14x14		6		3	12	18	72	
STR731FV1T6	128									
STR731FV2T6	256									
STR736FV0T6	64	TQFP100 14x14				0				
STR736FV1T6	128									
STR736FV2T6	256									
STR730FZ1T7	128	TQFP144 20x20	16	10	1	3	16	32	112	-40 to +105°C
STR730FZ2T7	256									
STR730FZ1H7	128	LFBGA144 10x10								
STR730FZ2H7	256									
STR735FZ1T7	128	TQFP144 20x20				0				
STR735FZ2T7	256									
STR735FZ1H7	128	LFBGA144 10x10								
STR735FZ2H7	256									
STR731FV0T7	64	TQFP100 14x14		6		3	12	18	72	
STR731FV1T7	128									
STR731FV2T7	256									
STR736FV0T7	64	TQFP100 14x14				0				
STR736FV1T7	128									
STR736FV2T7	256									

7 Known limitations

7.1 Low power wait for interrupt mode

When the STR73x device is put in Low Power Wait For Interrupt mode (LPWFI), the Flash goes into low power mode or power down mode, depending on the setting of the PWD bit in the Flash Control Register 0 (default is '0', Low Power mode). This default mode can create excessive voltage conditions on the transistor gates and may affect the long term behavior of the Low Power mode circuitry.

Workaround

There is no workaround. If Low Power Wait For Interrupt mode is used, it is strongly suggested to configure the Flash to enter power down mode (bit PWD = '1').

7.2 PLL free running mode at high temperature

When the STR73x device is operated and an ambient temperature (T_A) of more than 55° C and the main system clock (f_{MCLK}) is sourced by the PLL in free running mode, the device may not work properly.

Workaround

At high temperature (more than 55° C), it is recommended to use the internal RC oscillator as a backup clock source rather than the PLL free running mode.

8 Revision history

Table 30. Document revision history

Date	Revision	Description of changes
19-Sep-2005	1	First release
02-Nov-2005	2	Removed Table 8 power consumption in LP modes Updated PLL frequency in *Section 1.1* and *Table 12*
08-Mar-2006	3	*Section 3.4: Preliminary power consumption data* updated *Section 3.5: DC electrical characteristics* updated *Section 7: Known limitations* added
04-Jun-2006	4	*Section 4: Electrical parameters* updated *Section 7: Known limitations* updated Added temperature range -40°C to 85°C in *Section 6: Order codes*
19-Jun-2006	5	Changed Flash data retention to 20 years at 85°C in *Table 18 on page 34*.
08-Sep-2006	6	Changed *Table 24: Output driving current on page 39* Added *Figure 14: VOL standard ports vs IOL @ VDD 5 V* thru *Figure 18: VOL P6.0 pin vs IOL @ VDD 5 V on page 40*. Added *Figure 20: NRSTIN RPU vs. VDD*
08-Jun-2008	7	Inch values rounded to 4 decimal digits in *Section 5.1: Package mechanical data* Modified BSPI speed in *Section 2.1: On-chip peripherals*