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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM7®
Core Size	32-Bit Single-Core
Speed	36MHz
Connectivity	CANbus, I²C, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	72
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/str731fv2t6

Contents

1 Scope

This datasheet provides the STR73x ordering information, mechanical and electrical device characteristics.

For complete information on the STR73xF microcontroller memory, registers and peripherals. please refer to the STR73x reference manual.

For information on programming, erasing and protection of the internal Flash memory please refer to the STR7 Flash programming reference manual.

For information on the ARM7TDMI core please refer to the ARM7TDMI technical reference manual.

1.1 Description

ARM core with embedded Flash & RAM

STR73xF family combines the high performance ARM7TDMI™ CPU with an extensive range of peripheral functions and enhanced I/O capabilities. All devices have on-chip high-speed single voltage Flash memory and high-speed RAM. The STR73xF family has an embedded ARM core and is therefore compatible with all ARM tools and software.

Extensive tools support

STMicroelectronics' 32-bit, ARM core-based microcontrollers are supported by a complete range of high-end and low-cost development tools to meet the needs of application developers. This extensive line of hardware/software tools includes starter kits and complete development packages all tailored for ST's ARM core-based MCUs.

The range of development packages includes third-party solutions that come complete with a graphical development environment and an in-circuit emulator/programmer featuring a JTAG application interface. These support a range of embedded operating systems (OS), while several royalty-free OSs are also available.

For more information, please refer to ST MCU site http://www.st.com/mcu

Figure 1 shows the general block diagram of the device family.

Flexible clock control

Two clock sources are used to drive the microcontroller, a main clock driven by an external crystal or ceramic resonator and an internal backup RC oscillator that operates at 2 MHz or 32 kHz. The embedded PLL can be configured to generate an internal system clock of up to 36 MHz. The PLL output frequency can be programmed using a wide selection of multipliers and dividers.

Voltage regulators

The STR73xF requires an external 4.5 to 5.5 V power supply. There are two internal Voltage Regulators for generating the 1.8 V power supply needed by the core and peripherals. The main VR is switched off and the Low Power VR switched on when the application puts the STR73xF in Low Power Wait for Interrupt (LPWFI) mode.

Low voltage detectors

The voltage regulator and Flash modules each have an embedded LVD that monitors the internal 1.8 V supply. If the voltage drops below a certain threshold, the LVD will reset the STR73xF.

Note: An external power-on reset must be provided ensure the microcontroller starts-up correctly.

2.1 On-chip peripherals

CAN interfaces

The three CAN modules are compliant with the CAN specification V2.0 part B (active). The bit rate can be programmed up to 1 MBaud. These are not available in the STR735 and STR736.

DMA

4 DMA controllers, each with 4 data streams manage memory to memory, peripheral to peripheral, peripheral to memory and memory to peripheral transfers. The DMA requests are connected to TIM timers, BSPI0, BSPI1, BSPI2 and ADC. One of the streams can be configured to be triggered by a software request, independently from any peripheral activity.

16-bit timers (TIM)

Each of the ten timers (six in 100-pin devices) have a 16-bit free-running counter with 7-bit prescaler, up to two input capture/output compare functions, a pulse counter function, and a PWM channel with selectable frequency. This provides a total of 16 independent PWMs (12 in 100-pin devices) when added with the PWM modules (see next paragraph).

PWM modules (PWM)

The six 16-bit PWM modules have independently programmable periods and duty-cycles, with 5+3 bit prescaler factor.

Timebase timers (TB)

The three 16-bit timebase timers with 8-bit prescaler for general purpose time triggering operations.

Real-time clock (RTC)

The RTC provides a set of continuously running counters driven by separate clock signal derived from the main oscillator. The RTC can be used as a general timebase or

3.1 Related documentation

Available from www.arm.com:

ARM7TDMI technical reference manual

Available from http://www.st.com:

STR73x reference manual (RM0001)

STR7 Flash programming reference manual

STR73x software library user manual

For a list of related application notes refer to http://www.st.com.

3.2.2 STR730F/STR735F (LFBGA144)

Table 3. STR730F/STR735F LFBGA ball connections

Ball	Name	Ball	Name	Ball	Name	Ball	Name
A1	P0.0 / OCMPB2	B1	P0.4 / OCMPA5	C1	P0.5 / OCMPB5	D1	V_{SS}
A2	P6.10 / WUP8	B2	P0.1 / OCMPA2	C2	P0.2 / ICAPA2	D2	V_{DD}
A3	P6.9 / TDO0	B3	P6.15 / WUP9	C3	P0.3 / ICAPB2	D3	P0.6 / ICAPA5
A4	P6.12 / MOSI0	B4	P6.13 / SCKO / WUP11	C4	P6.14 / SSO	D4	P0.7 /ICAPB5
A5	P6.6 / WUP6	B5	P6.7 / WUP7	C5	P6.8 / RDI0 / WUP10	D5	P6.11 / MISO0
A6	V_{18}	B6	P6.2 / WUP2 / RDI3	C6	P6.3 / WUP3	D6	P6.4 / WUP4 /TDO3
A7	P5.15 / INT13	B7	P5.14 / INT12	C7	V_{SS}	D7	VDD
A8	P5.8 / INT6	B8	P5.9 / INT7	C8	P5.10 / INT8 / RDI2	D8	P5.12 / INT10
A9	P5.2 / OCMPA9	B9	P5.3 / OCMPB9	C9	P5.4 / SS2	D9	P5.5 / SCK2 / WUP23
A10	P5.7 / MISO2	B10	P5.0 / MOSI1	C10	P5.1 / MISO1	D10	P4.13 / ICAPB9
A11	P5.6 / MOSI2	B11	P4.15 / SCK1 / WUP22	C11	P4.14 / SS1	D11	P4.12 / ICAPA9 / WUP21
A12	P5.11 / TDO2 / INT9	B12	P4.8 / OCMPA8	C12	P4.7 / SDA1	D12	P4.11 / OCMPB8
E1	P0.8 / OCMPA6	F1	V_{DD}	G1	V_{SS}	H1	V_{DD}
E2	P0.9 / OCMPB6	F2	P0.13 / ICAPB3	G2	P1.2 / ICAPB4	H2	P1.8 / OCMPA0 / INT0
E3	P0.10 / OCMPA7	F3	P0.14 / OCMPB3	G3	P1.3 / ICAPA4	H3	P1.9 / OCMPB0 / INT1
E4	P0.11 / OCMPB7	F4	P0.15 / OCMPA3	G4	V_{SS}	H4	P1.10 / ICAPB0 / WUP28
E5	P0.12 / ICAPA3	F5	P1.0 / OCMPA4	G5	P1.5	H5	XTAL2
E6	P6.5 / WUP5	F6	P1.1 / OCMPB4	G6	P2.11 / WUP17	H6	P2.10 / WUP16
E7	P6.0 / WUP0	F7	P6.1 / WUP1	G7	P4.0 / ICAPA7 / WUP24	H7	P2.15 / SDA 0
E8	P5.13 / INT11	F8	P4.4 / CAN2TX[1)]	G8	VDD	H8	JTMS
E9	P4.10 / ICAPA6 / WUP20	F9	P4.3 / ICAPB8 / WUP27	G9	VSS	H9	VSS
E10	P4.9 / ICAPB6	F10	P4.2 / ICAPA8 / WUP26	G10	JTDO	H10	VDD
E11	P4.6 / SCL1 / WUP19	F11	P4.1 / ICAPB7 / WUP25	G11	JTCK	H11	P3.15 / AIN15 / INT5
E12	P4.5 / WUP18 / CAN2RX[1)]	F12	JTDI	G12	nJTRST	H12	P3.14 / AIN14 / INT4
J1	P1.4	K1	P1.6 / OCMPB1	L1	P1.7 / OCMPA1	M1	P1.14 / CAN0RX[1)] / WUP12
J2	P1.11 / ICAPA0 / WUP29	K2	P1.13 / ICAPB1 / WUP31	L2	P1.15 / CAN0TX[1)]	M2	P2.4 / PWM2
J3	P1.12 / ICAPA1 / WUP30	K3	P2.1 / CAN1RX[1)] / WUP13	L3	P2.0 / PWM0	M3	P2.5 / PWM3
J4	P2.7 / PWM5	K4	P2.6 / PWM4	L4	P2.3 / PWM1	M4	P2.2 / CAN1TX[1)]
J5	V_{DD}	K5	M1	L5	RSTIN	M5	M0
J6	P2.9 / RDI1 / WUP14	K6	P2.8 / TDO1	L6	V_{SS}	M6	V_{SS}
J7	P2.14 / SCL 0 / WUP15	K7	P2.13 / INT15	L7	P2.12 / INT14	M7	XTAL1
J8	P3.1 / AIN1	K8	P3.0 / AIN0	L8	VBIAS	M8	TST
J9	P3.13 / AIN13 / INT3	K9	P3.4 / AIN4	L9	P3.3 / AIN3	M9	P3.2 / AIN2
J10	P3.12 / AIN12 / INT2	K10	V_{DDA}	L10	P3.5 / AIN5	M10	V_{SS}
J11	P3.9 / AIN9	K11	V_{SSA}	L11	P3.7 / AIN7	M11	V_{DD}
J12	P3.8 / AIN8	K12	P3.11 / AIN11	L12	P3.10 / AIN10	M12	P3.6 / AIN6

Note: CAN alternate functions not available on STR735F.

Legend / Abbreviations for *Table 4*:

Type: I = input, O = output, S = supply, HiZ= high impedance,

In/Output level: T_T= TTL 0.8 V / 2 V with input trigger
C_T= CMOS $0.3V_{DD}/0.7V_{DD}$ with input trigger

Port and control configuration:

Input: pu/pd = with internal 100 kΩ weak pull-up or pull down

Output: OD = open drain (logic level)
PP = push-pull

Interrupts:

INTx = external interrupt line

WUPx = wake-up interrupt line

The reset state (during and just after the reset) of the I/O ports is input floating (Input tristate TTL mode). To avoid excess power consumption, unused I/O ports must be tied to ground.

Table 4. STR73xF pin description

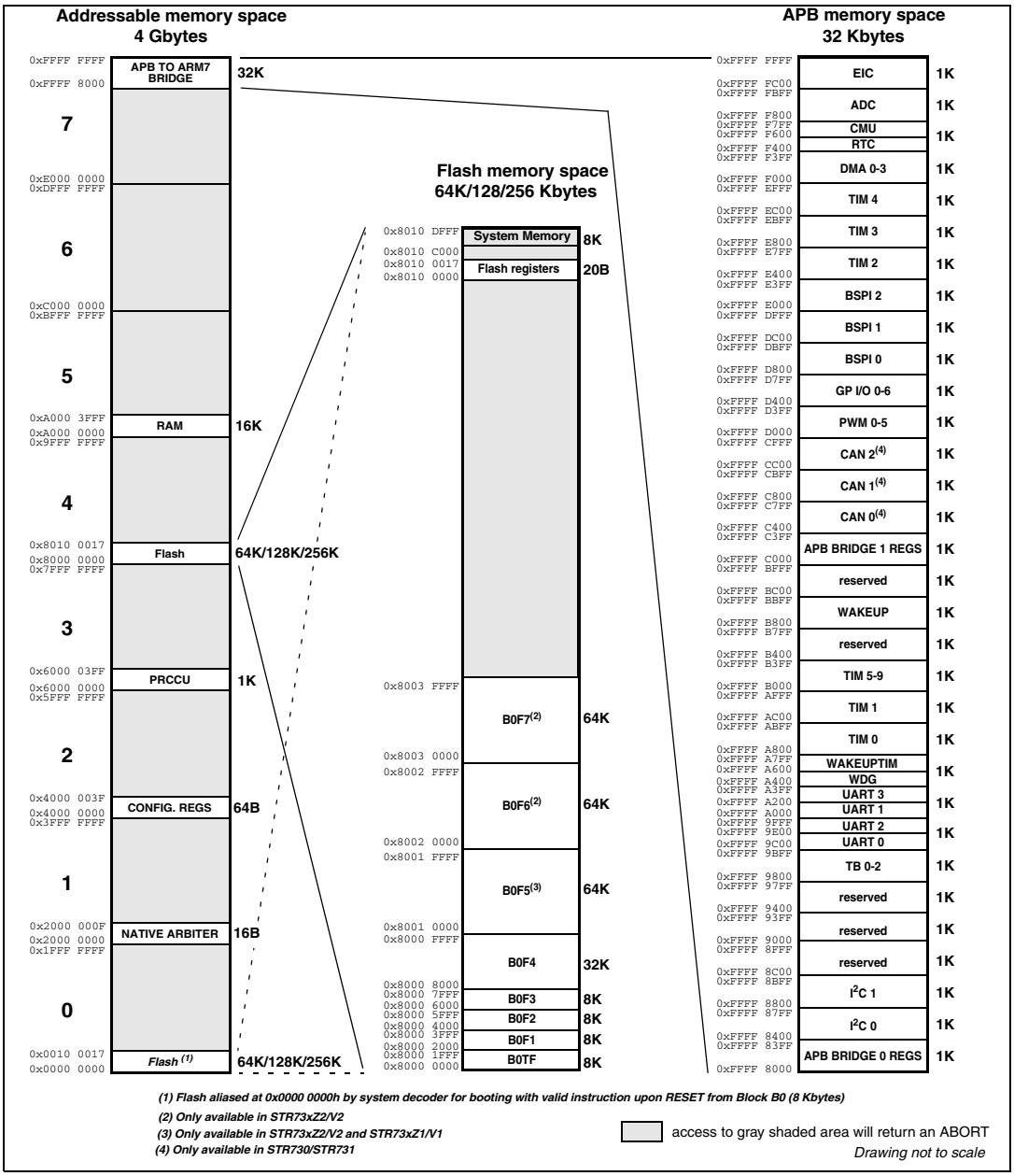
Pin n°			Pin name	Type	Input			Output			Main function (after reset)	Alternate function
TQFP144	LFBGA144	TQFP100			Input Level	pu/pd	interrupt	Capability	OD	PP		
1	A1	1	P0.0/OCMPB2	I/O	T_T			2mA	X	X	Port 0.0	TIM2: output compare B output
2	B2	2	P0.1/OCMPA2	I/O	T_T			2mA	X	X	Port 0.1	TIM2: output compare A output
3	C2	3	P0.2/ICAPA2	I/O	T_T			2mA	X	X	Port 0.2	TIM2: input capture A input
4	C3	4	P0.3/ICAPB2	I/O	T_T			2mA	X	X	Port 0.3	TIM2: input capture B input
5	D1		V_{SS}	S							Ground	
6	D2		V_{DD}	S							Supply voltage (5 V)	
7	B1	5	P0.4/OCMPA5	I/O	T_T			2mA	X	X	Port 0.4	TIM5: output compare A output
8	C1	6	P0.5/OCMPB5	I/O	T_T			2mA	X	X	Port 0.5	TIM5: output compare B output
9	D3	7	P0.6/ICAPA5	I/O	T_T			2mA	X	X	Port 0.6	TIM5: input capture A input
10	D4		P0.7/ICAPB5	I/O	T_T			2mA	X	X	Port 0.7	TIM5: input capture B input
11	E1		P0.8/OCMPA6	I/O	T_T			2mA	X	X	Port 0.8	TIM6: output compare A output
12	E2		P0.9/OCMPB6	I/O	T_T			2mA	X	X	Port 0.9	TIM6: output compare B output
13	E3		P0.10/OCMPA7	I/O	T_T			2mA	X	X	Port 0.10	TIM7: output compare A output
14	E4		P0.11/OCMPB 7	I/O	T_T			2mA	X	X	Port 0.11	TIM7: output compare B output
15	F1	8	V_{DD}	S							Supply voltage (5 V)	
16	G1	9	V_{SS}	S							Ground	
17	E5	10	P0.12/ICAPA3	I/O	T_T			2mA	X	X	Port 0.12	TIM3: input capture A input
18	F2	11	P0.13/ICAPB3	I/O	T_T			2mA	X	X	Port 0.13	TIM3: input capture B input

3.3 Memory mapping

Figure 5 shows the various memory configurations of the STR73xF system. The system memory map (from 0x0000_0000 to 0xFFFF_FFFF) is shown on the left part of the figure, the right part shows maps of the Flash and APB areas. For flexibility the Flash or RAM addresses can be aliased to Block 0 addresses using the remapping feature

Most reserved memory spaces (gray shaded areas in *Figure 5*) are protected from access by the user code. When an access this memory space is attempted, an ABORT signal is generated. Depending on the type of access, the ARM processor will enter “prefetch abort” state (Exception vector 0x0000_000C) or “data abort” state (Exception vector 0x0000_0010). It is up to the application software to manage these abort exceptions.

Figure 5. Memory map



4 Electrical parameters

4.1 Parameter conditions

Unless otherwise specified, all voltages are referred to V_{SS}.

4.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A=25° C and T_A=T_{Amax} (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3Σ).

4.1.2 Typical values

Unless otherwise specified, typical data are based on T_A=25° C and V_{DD}=5 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2Σ).

4.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

4.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 6*.

4.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 7*.

Figure 6. Pin loading conditions

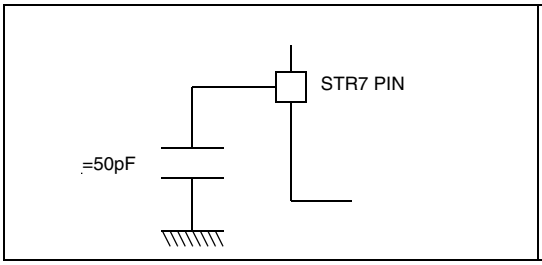
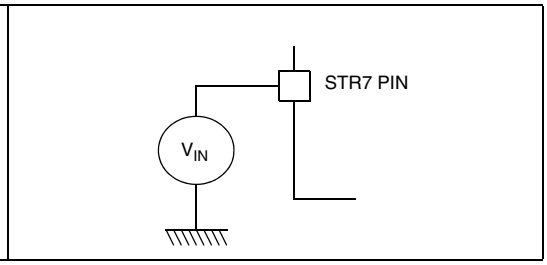


Figure 7. Pin input voltage



4.2 Absolute maximum ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 5. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DD} - V_{SS}	External 5 V Supply voltage	-0.3	6.0	V
V_{SSA}	Reference ground for A/D converter	V_{SS}	V_{SS}	V
V_{DDA}- V_{SSA}	Reference voltage for A/D converter	-0.3	V_{DD}+0.3	V
V_{IN}	Input voltage on any pin	-0.3	V_{DD}+0.3	
$\lvert\Delta V_{DDx}\rvert$	Variations between different 5 V power pins	-	0.3	mV
$\lvert V_{SSX}$ - $V_{SS}\rvert$	Variations between all the different ground pins	-	0.3	
$V_{ESD(HBM)}$	Electrostatic discharge voltage (Human Body Model)	see *: Absolute maximum ratings (electrical sensitivity) on page 36*		
$V_{ESD(MM)}$	Electrostatic discharge voltage (Machine Model)			

Table 6. Current characteristics

Symbol	Ratings	Max.	Unit
I_{VDD}	Total current into V_{DD} power lines (source) 1)	100	mA
I_{VSS}	Total current out of V_{SS} ground lines (sink) 1)	100	
I_{IO}	Output current sunk by any I/O and control pin	10	
	Output current source by any I/O and control pin	10	
$I_{INJ(PIN)}$ 2) & 3)	Injected current on any other pin 4) &5)	±10	
$\Sigma I_{INJ(PIN)}$ 2)	Total injected current (sum of all I/O and control pins) 4)	±75	

1. All 5 V power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external 5 V supply
2. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$.
3. Negative injection disturbs the analog performance of the device. See note in *Section 4.3.6: 10-bit ADC characteristics on page 43*.
4. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values). These results are based on characterization with $\Sigma I_{INJ(PIN)}$ maximum current injection on four I/O port pins of the device.

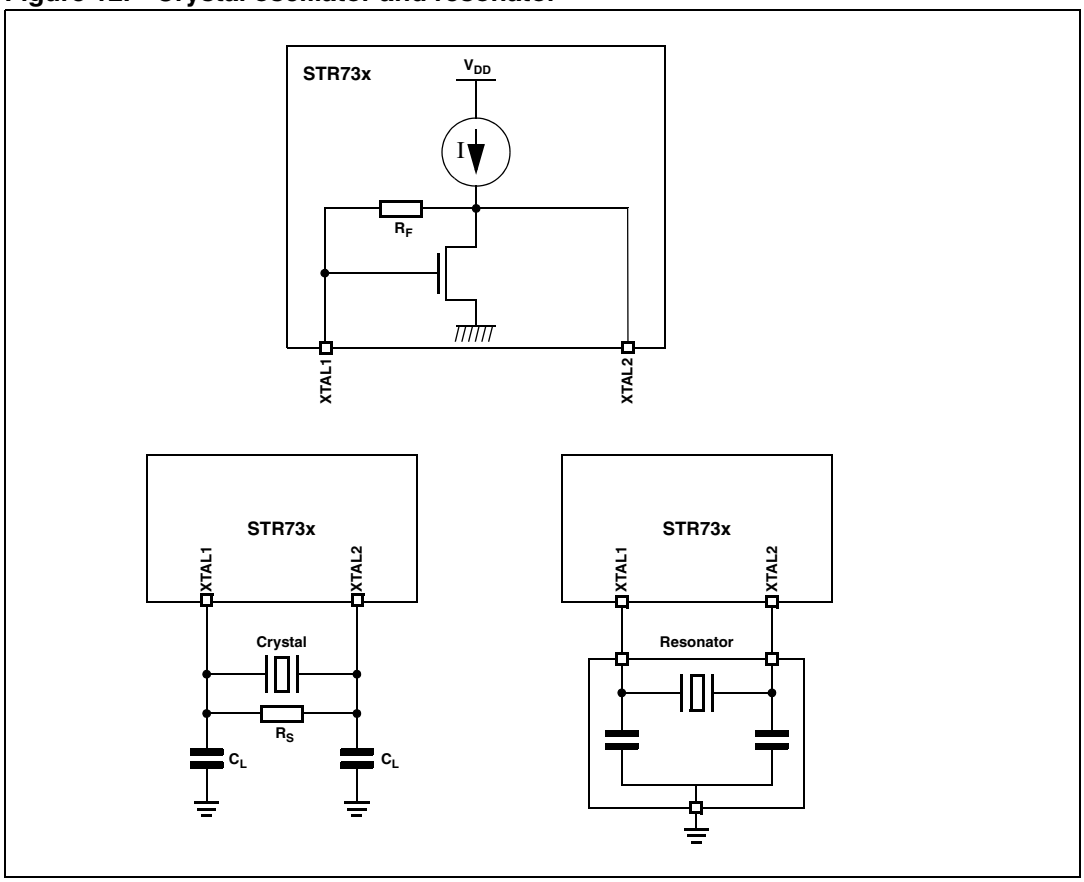
5.) In 144-pin devices, only +10 mA on P0.3, P1.13, P3.6 and P4.13 pins (negative injection not allowed).

4.3.2 Clock and timing characteristics

Crystal / ceramic resonator oscillator

The STR73xF can operate with a crystal oscillator or resonator clock source. *Figure 12* describes a simple model of the internal oscillator driver as well as example of connection for an oscillator or a resonator.

Figure 12. Crystal oscillator and resonator



Note: 1 XTAL2 must not be used to directly drive external circuits.

2 For test or boot purpose, XTAL2 can be used as an high impedance input pin to provide an external clock to the device. XTAL1 should be grounded, and XTAL2 connected to a wave signal generator providing a 0 to VDD signal. Directly driving XTAL2 may results in deteriorated jitter and duty cycle.

Main oscillator characteristics

V_{DD} = 5 V ± 10%, T_A = -40° C to T_{Amax}, unless otherwise specified.

Table 14. Main oscillator characteristics

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
f_{OSC}	Oscillator frequency		4		8	MHz
g_m	Oscillator transconductance		1.5		4.2	mA/V
V_{OSC} 1)	Oscillation amplitude	f_{OSC} = 4 MHz, T_A= 25° C	-	2.4	-	V
		f_{OSC} = 8 MHz, T_A= 25° C		1.-		
V_{AV} 1)	Oscillator operating point	Sine wave middle, T_A= 25° C	-	0.77	-	v
t_{STUP} 1)	Oscillator start-up time	External crystal, V_{DD} = 5.5 V, f_{OSC} = 4 MHz, T_A=-40° C	-	-	12	ms
		External crystal, V_{DD} = 5.0 V, f_{OSC} = 4 MHz, T_A=25° C	-	5.5	-	ms
		External crystal, V_{DD} = 5.5 V, f_{OSC} = 6 MHz, T_A=-40° C	-	-	8	ms
		External crystal, V_{DD} = 5.0 V, f_{OSC} = 6 MHz, T_A=25° C	-	3.3	-	ms
		External crystal, V_{DD} = 5.5 V, f_{OSC} = 8 MHz, T_A=-40° C	-	-	7	ms
		External crystal, V_{DD} = 5.0 V, f_{OSC} = 8 MHz, T_A= 25° C	-	2.7	-	ms

PLL electrical characteristics

V_{DD} = 5 V ± 10%, T_A = -40° C to T_{Amax}, unless otherwise specified

Table 16. PLL characteristics

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
f_{PLLIN} (1)	PLL reference clock	FREF_RANGE = '0' FREF_RANGE = '1'	1.5 3.0		3.0 5.0	MHz
f_{PLLOUT}	PLL output clock	MX = "00" MX = "01" MX = "10" MX = "11"	20 x f_{PLLIN} 12 x f_{PLLIN} 28 x f_{PLLIN} 16 x f_{PLLIN}			MHz
f_{MCLK}	System clock	DX = 1..7	f_{PLLOUT}/DX		36	MHz
f_{FREE} (2)	PLL free running frequency	FREF_RANGE = '0', MX0 = '1' FREF_RANGE = '0', MX0 = '0' FREF_RANGE = '1', MX0 = '1' FREF_RANGE = '1', MX0 = '0'		120 240 240 480		kHz
t_{LOCK} (3)	PLL lock time	Stable oscillator (f_{PLLIN} = 4 MHz), stable V_{DD}		100	300	µs
Δt_{PKJIT}	PLL jitter (pk to pk)	f_{PLLIN} = 4 MHz (pulse generator)			1.5	ns

1. f_{PLLIN} is obtained from f_{OSC} directly or through an optional divider by 2.
2. Typical data are based on T_A=25°C, V_{DD}=5V
3. Max value is guaranteed by characterization, not tested in production.

Table 17. Low-power mode wake-up timing

Symbol	Parameter	Conditions	Typ	Unit
t_{WUHALT}	Wake-up from HALT mode		200	µs
t_{WUSTOP}	Wake-up from STOP mode	RC high frequency in STOP mode	180	µs
		RC low frequency in STOP mode	234	µs
$t_{WULPWFI}$ 1)	Wake-up from LPWFI mode	Main voltage regulator on RC oscillator off f_{OSC} = 4 MHz, f_{MCLK}= f_{OSC}/16 RAM or FLASH execution	27	µs
		Main voltage regulator on RC oscillator = high frequency Flash execution	46	µs
		Main voltage regulator on RC oscillator = low frequency Flash execution	3.6	ms

1. Flash memory programmed to enter Power Down mode during LPWFI.

4.3.3 Memory characteristics

Flash memory

Table 18. Flash memory characteristics

Symbol	Parameter	Test Conditions	Value			Unit
			Min	Typ	Max[1)]	
t_{WP}	Word program (32-bit)			35	80	µs
t_{DWP}	Double word program(64-bit)			64	150	µs
t_{BP64}	Bank program (64 K)	Double word program		0.5	1.25	s
t_{BP128}	Bank program (128 K)	Double word program		1	2.5	s
t_{BP256}	Bank program (256 K)	Double word program		2	4.9	s
t_{SE8}	Sector erase (8 K)	Not preprogrammed Preprogrammed [2)]		0.6 0.5	0.9 0.8	s
t_{SE32}	Sector erase (32 K)	Not preprogrammed Preprogrammed[2)]		1.1 0.8	2 1.8	s
t_{SE64}	Sector erase (64 K)	Not preprogrammed preprogrammed [2)]		1.7 1.3	3.7 3.3	s
t_{RPD}[3)]	Recovery from power-down				20	µs
t_{PSL}[3)]	Program suspend latency				10	µs
t_{ESL}[3)]	Erase suspend latency				30	µs
t_{ESR}[3)]	Erase suspend rate	Min. time from erase resume to next erase suspend		20	20	ms
t_{SP}[3)]	Set protection			40	170	µs
t_{FPW}[3)]	First word program			1		ms
N_{END}	Endurance		10			kcycles
t_{RET}	Data retention	T_A = 85° C	20			Years

1. T_A = -45° C after 0 cycles, Guaranteed by characterization, not tested in production.
2. All bits programmed to 0.
3. Guaranteed by design, not tested in production.

4.3.4 EMC characteristics

Susceptibility tests are performed on a sample basis during product characterization.

Functional EMS (electromagnetic susceptibility)

Based on a simple running application on the product (toggling 2 LEDs through I/O ports), the product is stressed by two electromagnetic events until a failure occurs (indicated by the LEDs).

- **ESD**: Electrostatic discharge (positive and negative) is applied on all pins of the device until a functional disturbance occurs. This test conforms with the IEC 1000-4-2 standard.
- **FTB**: A burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test conforms with the IEC 1000-4-4 standard.

A device reset allows normal operations to be resumed. The test results are given in the table below based on the EMS levels and classes defined in application note AN1709.

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations:

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical data corruption (control registers...)

Prequalification trials:

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the RESET pin or the oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Table 19. EMS data

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD}=5 V, T_A=+25° C, f_{MCLK}=36 MHz conforms to IEC 1000-4-2	4A
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD}=5 V, T_A=+25° C, f_{MCLK}=36 MHz conforms to IEC 1000-4-4	4A

Electromagnetic interference (EMI)

Based on a simple application running on the product (toggling 2 LEDs through the I/O ports), the product is monitored in terms of emission. This emission test is in line with the norm SAE J 1752/3 which specifies the board and the loading of each pin.

Table 20. EMI data

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{OSC4M}/f_{MCLK}]		Unit
				6/36 MHz	8/8 MHz	
S_{EMI}	Peak level	V_{DD}=5.0V, T_A=+25°C, All packages	0.1 MHz to 30 MHz	23	30	dBµV
			30 MHz to 130 MHz	37	34	
			130 MHz to 1 GHz	20	7	
			SAE EMI Level	4	3.5	-

Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU and DLU) using specific measurement methods, the product is stressed in order to determine its performance in terms of electrical sensitivity. For more details, refer to the application note AN1181.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts*(n+1) supply pin). Two models can be simulated: human body model and machine model. This test conforms to the JESD22-A114A/A115A standard.

Table 21. ESD Absolute Maximum ratings

Symbol	Ratings	Conditions	Maximum value [1]	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A=+25° C	2000	V
$V_{ESD(MM)}$	Electrostatic discharge voltage (machine model)		200	
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)		750 on corner pins, 500 on others	

Notes:

1. Data based on characterization results, not tested in production.

Static and dynamic latch-up

- **LU**: 3 complementary static tests are required on 10 parts to assess the latch-up performance. A supply overvoltage (applied to each power supply pin) and a current injection (applied to each input, output and configurable I/O pin) are performed on each

Output driving current

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified.

Table 24. Output driving current

I/O Type	Symbol	Parameter	Conditions	Min	Max	Unit
Standard	V_{OL} 1)	Output low level voltage for an I/O pin when 8 pins are sunk at same time	I_{IO}=+2 mA		0.4	V
	V_{OH} 2)	Output high level voltage for an I/O pin when 4 pins are sourced at same time	I_{IO}=-2 mA	V_{DD}-0.8		
Med. Current (JTDO)	V_{OL} 1)	Output low level voltage for an I/O pin	I_{IO}=+6 mA		0.4	
	V_{OH} 2)	Output high level voltage for an I/O pin	I_{IO}=-6 mA	V_{DD}-0.8		
High Current P6.0	V_{OL} 1)	Output low level voltage for an I/O pin	I_{IO}=+8 mA		0.4	
	V_{OH} 2)	Output high level voltage for an I/O pin	I_{IO}=-8 mA	V_{DD}-0.8		

1. The I_{IO} current sunk must always respect the absolute maximum rating specified in *Table 6* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
2. The I_{IO} current sourced must always respect the absolute maximum rating specified in *Table 6* and the sum of I_{IO} (I/O ports and control pins) must not exceed IV_{DD}.

Figure 13. V_{OH} standard ports vs I_{OH} @ V_{DD} 5V T_A -45° C

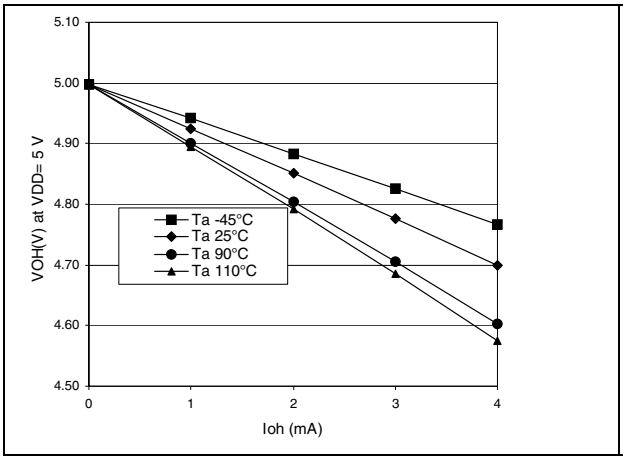


Figure 14. V_{OL} standard ports vs I_{OL} @ V_{DD} 5 V

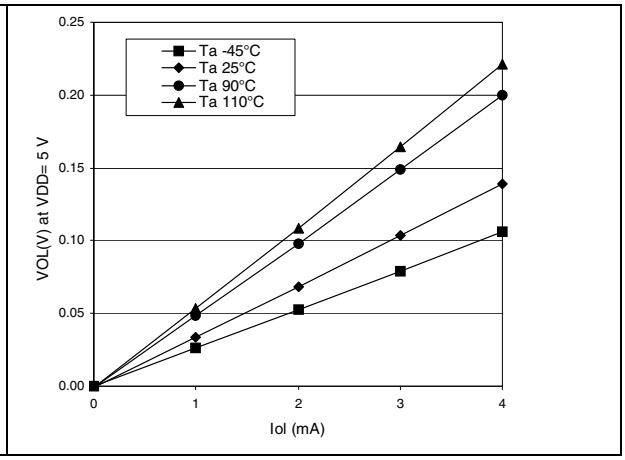


Figure 15. V_{OH} JTDO pin vs I_{OL} @ V_{DD} 5 V

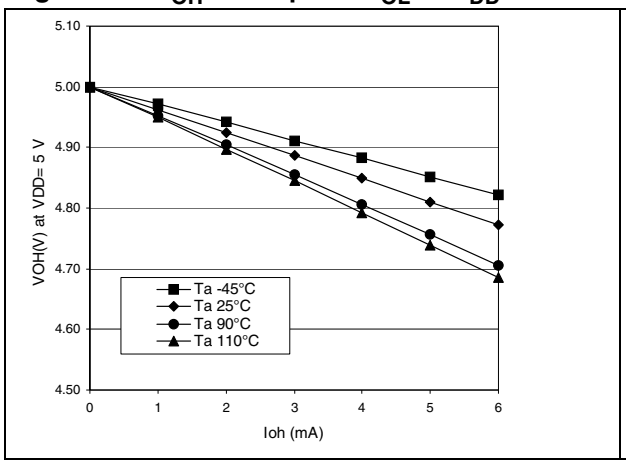


Figure 16. V_{OL} JTDO pin vs I_{OL} @ V_{DD} 5 V

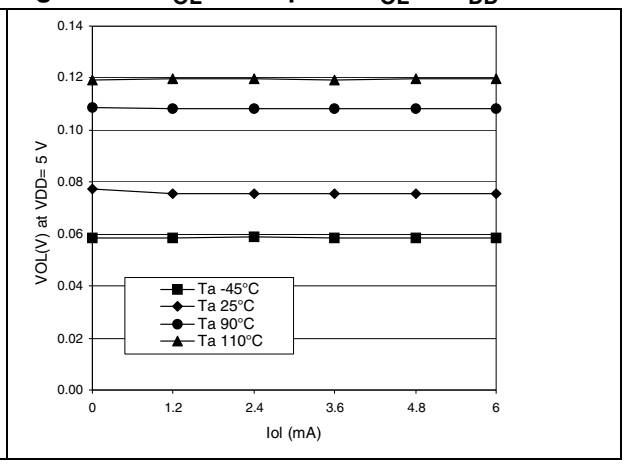


Figure 17. V_{OH} P6.0 pin vs I_{OL} @ V_{DD} 5 V

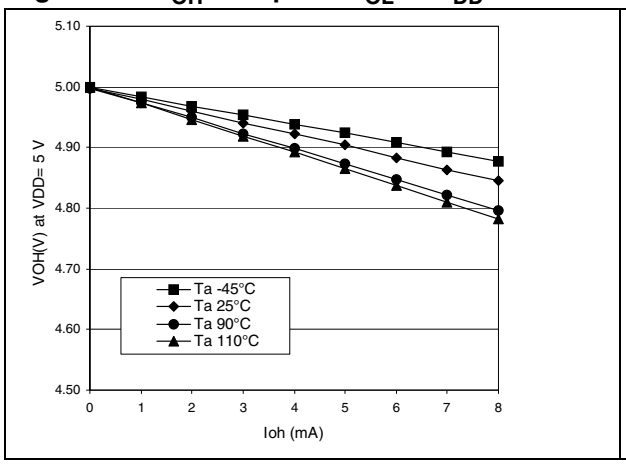
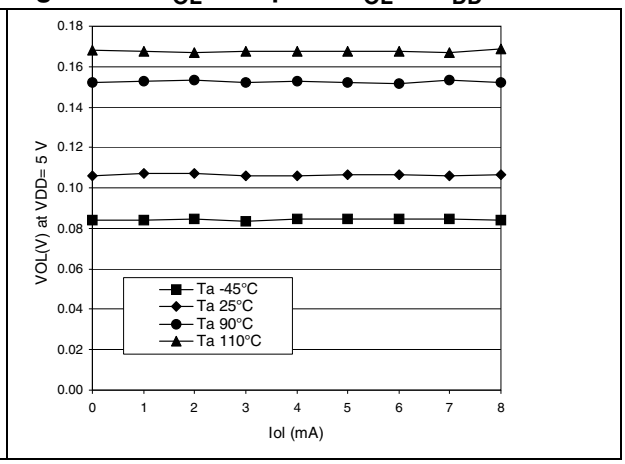


Figure 18. V_{OL} P6.0 pin vs I_{OL} @ V_{DD} 5 V



NRSTIN pin

The NRSTIN pin input driver is CMOS. A permanent pull-up is present which is the same as R_{PU} (see *: General characteristics on page 38*)

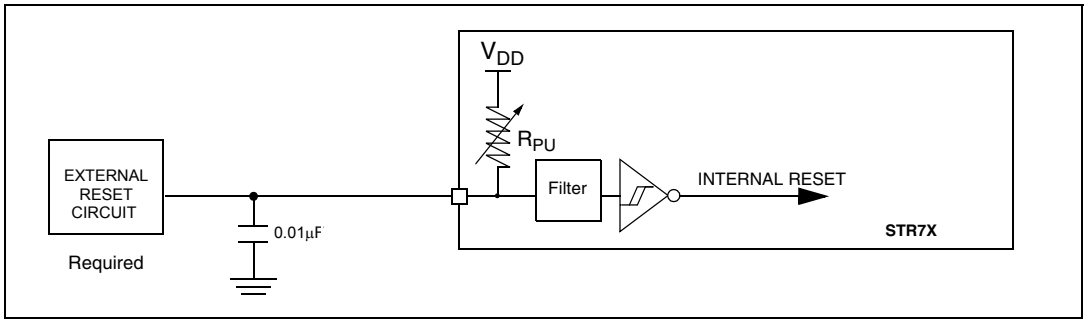
Subject to general operating conditions for V_{DD} and T_A unless otherwise specified.

Table 25. Reset pin characteristics

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
$V_{IL(NRSTIN)}$	NRSTIN Input low level voltage [1]				0.3 V_{DD}	V
$V_{IH(NRSTIN)}$	NRSTIN Input high level voltage [1]		0.7 V_{DD}			
$V_{hys(NRSTIN)}$	NRSTIN Schmitt trigger voltage hysteresis [2]			800		mV
$V_{F(RSTINn)}$	NRSTIN Input filtered pulse[3]				500	ns
$V_{NF(RSTINn)}$	NRSTIN Input not filtered pulse[3]		2			µs
$V_{RP(RSTINn)}$	NRSTIN removal after Power-up[3]		100			µs

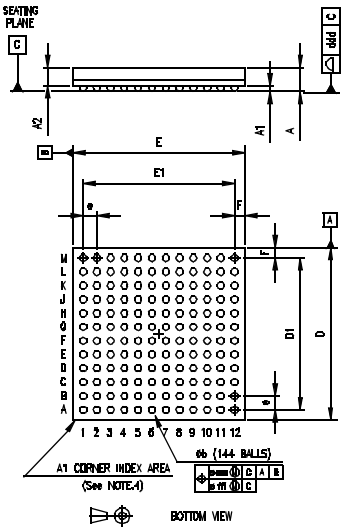
1. Data based on characterization results, not tested in production.
2. Hysteresis voltage between Schmitt trigger switching levels.
3. Data guaranteed by design, not tested in production.

Figure 19. Recommended NRSTIN pin protection[1]



1. The R_{PU} pull-up equivalent resistor is based on a resistive transistor.
2. The reset network protects the device against parasitic resets.
3. The user must ensure that the level on the NRSTIN pin can go below the $V_{IL(NRSTIN)}$ max. level specified in *Table 25*. Otherwise the reset will not be taken into account internally.

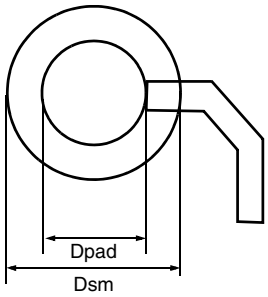
Figure 26. 144-ball low profile fine pitch ball grid array package



Dim.	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	1.21		1.70	0.0476		0.0669
A1	0.21			0.0083		
A2		1.085			0.0427	
b	0.35	0.40	0.45	0.0138	0.0157	0.0177
D	9.85	10.00	10.15	0.3878	0.3937	0.3996
D1		8.80			0.3465	
E	9.85	10.00	10.15	0.3878	0.3937	0.3996
E1		8.80			0.3465	
e		0.80			0.0315	
F		0.60			0.0236	
ddd			0.10			0.0039
eee			0.15			0.0059
fff			0.08			0.0031
	Number of Pins					
N	144					

[1] Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 27. Recommended PCB design rules (0.80/0.75mm pitch BGA)



Dpad	0.37 mm
Dsm	0.52 mm typ. (depends on solder mask registration tolerance
Solder paste	0.37 mm aperture diameter
– Non solder mask defined pads are recommended – 4 to 6 mils screen print	