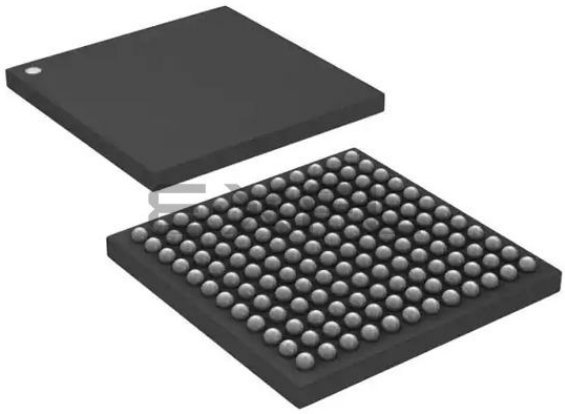

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM7®
Core Size	32-Bit Single-Core
Speed	36MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	112
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LFBGA
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/str735fz1h7

3.1 Related documentation

Available from www.arm.com:

ARM7TDMI technical reference manual

Available from http://www.st.com:

STR73x reference manual (RM0001)

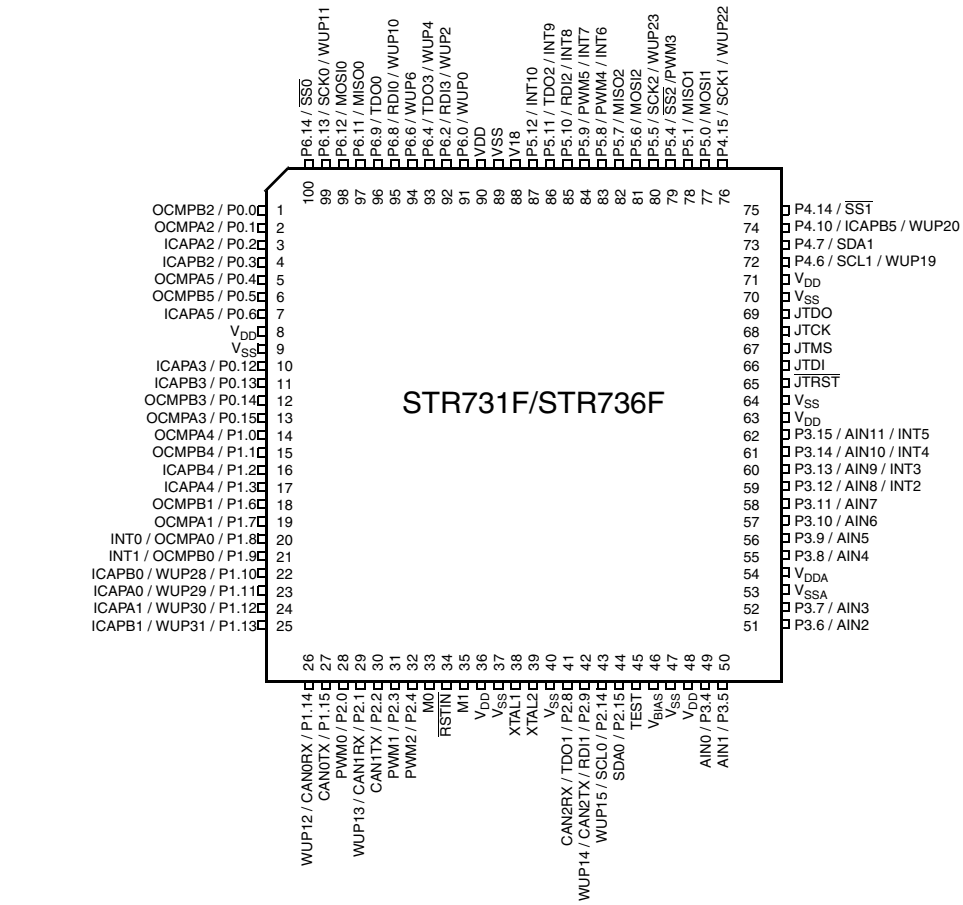
STR7 Flash programming reference manual

STR73x software library user manual

For a list of related application notes refer to http://www.st.com.

3.2.3 STR731F/STR736F (TQFP100)

Figure 4. STR731F/STR736F pin configuration (top view)



Note: CAN alternate functions not available on STR736F.

Table 4. STR73xF pin description

Pin n°			Pin name	Type	Input			Output			Main function (after reset)	Alternate function
TQFP144	LFBGA144	TQFP100			Input Level	pu/pd	interrupt	Capability	OD	PP		
19	F3	12	P0.14/OCMPB3	I/O	T_T			2mA	X	X	Port 0.14	TIM3: output compare B output
20	F4	13	P0.15/OCMPA3	I/O	T_T			2mA	X	X	Port 0.15	TIM3: output compare A output
21	F5	14	P1.0/OCMPA4	I/O	T_T			2mA	X	X	Port 1.0	TIM4: output compare A output
22	F6	15	P1.1/OCMPB4	I/O	T_T			2mA	X	X	Port 1.1	TIM4: output compare B output
23	G2	16	P1.2/ICAPB4	I/O	T_T			2mA	X	X	Port 1.2	TIM4: input capture B input
24	G3	17	P1.3/ICAPA4	I/O	T_T			2mA	X	X	Port 1.3	TIM4: input capture A input
25	G4		V_{SS}	S							Ground	
26	H1		V_{DD}	S							Supply voltage (5 V)	
27	J1		P1.4	I/O	T_T			2mA	X	X	Port 1.4	
28	G5		P1.5	I/O	T_T			2mA	X	X	Port 1.5	
29	K1	18	P1.6/OCMPB1	I/O	T_T			2mA	X	X	Port 1.6	TIM1: output compare B output
30	L1	19	P1.7/OCMPA1	I/O	T_T			2mA	X	X	Port 1.7	TIM1: output compare A output
31	H2	20	P1.8/OCMPA0	I/O	T_T		INT0	2mA	X	X	Port 1.8	TIM0: output compare A output
32	H3	21	P1.9/OCMPB0	I/O	T_T		INT1	2mA	X	X	Port 1.9	TIM0: output compare B output
33	H4	22	P1.10/ICAPB0	I/O	T_T		WUP28	2mA	X	X	Port 1.10	TIM0: input capture B input
34	J2	23	P1.11/ICAPA0	I/O	T_T		WUP29	2mA	X	X	Port 1.11	TIM0: input capture A input
35	J3	24	P1.12/ICAPA1	I/O	T_T		WUP30	2mA	X	X	Port 1.12	TIM1: input capture A input
36	K2	25	P1.13/ICAPB1	I/O	T_T		WUP31	2mA	X	X	Port 1.13	TIM1: input capture B input
37	M1	26	P1.14/CAN0RX	I/O	T_T		WUP12	2mA	X	X	Port 1.14	CAN0: receive data input
38	L2	27	P1.15/CAN0TX	I/O	T_T			2mA	X	X	Port 1.15	CAN0: transmit data output
39	L3	28	P2.0/PWM0	I/O	T_T			2mA	X	X	Port 2.0	PWM0: PWM output
40	K3	29	P2.1/CAN1RX	I/O	T_T		WUP13	2mA	X	X	Port 2.1	CAN1: receive data input
41	M4	30	P2.2/CAN1TX	I/O	T_T			2mA	X	X	Port 2.2	CAN1: transmit data output
42	L4	31	P2.3/PWM1	I/O	T_T			2mA	X	X	Port 2.3	PWM1: PWM output
43	M2	32	P2.4/PWM2	I/O	T_T			2mA	X	X	Port 2.4	PWM2: PWM output
44	M3		P2.5/PWM3	I/O	T_T			2mA	X	X	Port 2.5	PWM3: PWM output
45	K4		P2.6/PWM4	I/O	T_T			2mA	X	X	Port 2.6	PWM4: PWM output
46	J4		P2.7/PWM5	I/O	T_T			2mA	X	X	Port 2.7	PWM5: PWM output
47	M5	33	M0	I	T_T	pd					BOOT: mode selection 0 input	
48	L5	34	RSTIN	I	C_T	pu					Reset input	
49	K5	35	M1	I	T_T	pd					BOOT: mode selection 1 input	

Table 4. STR73xF pin description

Pin n°			Pin name	Type	Input			Output			Main function (after reset)	Alternate function	
TQFP144	LFBGA144	TQFP100			Input Level	pu/pd	interrupt	Capability	OD	PP			
97	F9		P4.3/ICAPB8	I/O	T_T		WUP27	2mA	X	X	Port 4.3	TIM8: input capture B input	
98	F8		P4.4/CAN2TX	I/O	T_T			2mA	X	X	Port 4.4	CAN2: transmit data output	
99	E12		P4.5/CAN2RX	I/O	T_T		WUP18	2mA	X	X	Port 4.5	CAN2: receive data input	
100	E11	72	P4.6/SCL1	I/O	T_T		WUP19	2mA	X	X	Port 4.6	I2C1: serial clock	
101	C12	73	P4.7/SDA1	I/O	T_T			2mA	X	X	Port 4.7	I2C1: serial data	
102	B12		P4.8/OCMPA8	I/O	T_T			2mA	X	X	Port 4.8	TIM8: output compare A output	
103	E10		P4.9/ICAPB6	I/O	T_T			2mA	X	X	Port 4.9	TIM6: input capture B input	
104	E9	74	P4.10/ICAPA6/ICAPB5	I/O	T_T		WUP20	2mA	X	X	Port 4.10	TIM6: input capture A input (144-pin pkg only)	TIM5: input capture B input (TQFP100 only)
105	D12		P4.11/OCMPB8	I/O	T_T			2mA	X	X	Port 4.11	TIM8: output compare B output	
106	D11		P4.12/ICAPA9	I/O	T_T		WUP21	2mA	X	X	Port 4.12	TIM9: input capture A input	
107	D10		P4.13/ICAPB9	I/O	T_T			2mA	X	X	Port 4.13	TIM9: input capture B input	
108	C11	75	P4.14/$\overline{SS}$1	I/O	T_T			2mA	X	X	Port 4.14	BSPI1: slave select	
109	B11	76	P4.15/SCK1	I/O	T_T		WUP22	2mA	X	X	Port 4.15	BSPI1: serial clock	
110	B10	77	P5.0/MOSI1	I/O	T_T			2mA	X	X	Port 5.0	BSPI1: master output/slave input	
111	C10	78	P5.1/MISO1	I/O	T_T			2mA	X	X	Port 5.1	BSPI1: master input/Slave output	
112	A9		P5.2/OCMPA9	I/O	T_T			2mA	X	X	Port 5.2	TIM9: output compare A output	
113	B9		P5.3/OCMPB9	I/O	T_T			2mA	X	X	Port 5.3	TIM9: output compare B output	
114	C9	79	P5.4/$\overline{SS}$2/PWM3	I/O	T_T			2mA	X	X	Port 5.4	BSPI2: slave select	PWM3: PWM output (TQFP100 only)
115	D9	80	P5.5/SCK2	I/O	T_T		WUP23	2mA	X	X	Port 5.5	BSPI2: serial clock	
116	A11	81	P5.6/MOSI2	I/O	T_T			2mA	X	X	Port 5.6	BSPI2: master output/slave input	
117	A10	82	P5.7/MISO2	I/O	T_T			2mA	X	X	Port 5.7	BSPI2: master input/slave output	
118	A8	83	P5.8/PWM4	I/O	T_T		INT6	2mA	X	X	Port 5.8	PWM4: PWM output (TQFP100 only)	

Table 4. STR73xF pin description

Pin n°			Pin name	Type	Input			Output			Main function (after reset)	Alternate function
TQFP144	LFBGA144	TQFP100			Input Level	pu/pd	interrupt	Capability	OD	PP		
119	B8	84	P5.9/PWM5	I/O	T_T		INT7	2mA	X	X	Port 5.9	PWM5: PWM output (TQFP100 only)
120	C8	85	P5.10/RDI2	I/O	T_T		INT8	2mA	X	X	Port 5.10	UART2: receive data input
121	A12	86	P5.11/TDO2	I/O	T_T		INT9	2mA	X	X	Port 5.11	UART2: transmit data output
122	D8	87	P5.12	I/O	T_T		INT10	2mA	X	X	Port 5.12	
123	E8		P5.13	I/O	T_T		INT11	2mA	X	X	Port 5.13	
124	B7		P5.14	I/O	T_T		INT12	2mA	X	X	Port 5.14	
125	A7		P5.15	I/O	T_T		INT13	2mA	X	X	Port 5.15	
126	A6	88	V_{18}	S								1.8 V decoupling pin: a decoupling capacitor (recommended value: 100 nF) must be connected between this pin and nearest VSS pin.
127	C7	89	V_{SS}	S								Ground
128	D7	90	V_{DD}	S								Supply voltage (5 V)
129	E7	91	P6.0	I/O	T_T		WUP0	8mA	X	X	Port 6.0	
130	F7		P6.1	I/O	T_T		WUP1	2mA	X	X	Port 6.1	
131	B6	92	P6.2/RDI3	I/O	T_T		WUP2	2mA	X	X	Port 6.2	UART3: receive data input
132	C6		P6.3	I/O	T_T		WUP3	2mA	X	X	Port 6.3	
133	D6	93	P6.4/TDO3	I/O	T_T		WUP4	2mA	X	X	Port 6.4	UART3: transmit data output
134	E6		P6.5	I/O	T_T		WUP5	2mA	X	X	Port 6.5	
135	A5	94	P6.6	I/O	T_T		WUP6	2mA	X	X	Port 6.6	
136	B5		P6.7	I/O	T_T		WUP7	2mA	X	X	Port 6.7	
137	C5	95	P6.8/RDI0	I/O	T_T		WUP10	2mA	X	X	Port 6.8	UART0: receive data input
138	A3	96	P6.9/TDO0	I/O	T_T			2mA	X	X	Port 6.9	UART0: transmit data output
139	A2		P6.10	I/O	T_T		WUP8	2mA	X	X	Port 6.10	
140	D5	97	P6.11/MISO0	I/O	T_T			2mA	X	X	Port 6.11	BSPI0: master input/slave output
141	A4	98	P6.12/MOSI0	I/O	T_T			2mA	X	X	Port 6.12	BSPI0: master output/slave input
142	B4	99	P6.13/SCK0	I/O	T_T		WUP11	2mA	X	X	Port 6.13	BSPI0: serial clock
143	C4	100	P6.14/$\overline{SS}$0	I/O	T_T			2mA	X	X	Port 6.14	BSPI0: slave select
144	B3		P6.15	I/O	T_T		WUP9	2mA	X	X	Port 6.15	

4.2 Absolute maximum ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 5. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DD} - V_{SS}	External 5 V Supply voltage	-0.3	6.0	V
V_{SSA}	Reference ground for A/D converter	V_{SS}	V_{SS}	V
V_{DDA}- V_{SSA}	Reference voltage for A/D converter	-0.3	V_{DD}+0.3	V
V_{IN}	Input voltage on any pin	-0.3	V_{DD}+0.3	
$\lvert\Delta V_{DDx}\rvert$	Variations between different 5 V power pins	-	0.3	mV
$\lvert V_{SSX}$ - $V_{SS}\rvert$	Variations between all the different ground pins	-	0.3	
$V_{ESD(HBM)}$	Electrostatic discharge voltage (Human Body Model)	see *: Absolute maximum ratings (electrical sensitivity) on page 36*		
$V_{ESD(MM)}$	Electrostatic discharge voltage (Machine Model)			

Table 6. Current characteristics

Symbol	Ratings	Max.	Unit
I_{VDD}	Total current into V_{DD} power lines (source) 1)	100	mA
I_{VSS}	Total current out of V_{SS} ground lines (sink) 1)	100	
I_{IO}	Output current sunk by any I/O and control pin	10	
	Output current source by any I/O and control pin	10	
$I_{INJ(PIN)}$ 2) & 3)	Injected current on any other pin 4) &5)	±10	
$\Sigma I_{INJ(PIN)}$ 2)	Total injected current (sum of all I/O and control pins) 4)	±75	

1. All 5 V power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external 5 V supply
2. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$.
3. Negative injection disturbs the analog performance of the device. See note in *Section 4.3.6: 10-bit ADC characteristics on page 43*.
4. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values). These results are based on characterization with $\Sigma I_{INJ(PIN)}$ maximum current injection on four I/O port pins of the device.

5.) In 144-pin devices, only +10 mA on P0.3, P1.13, P3.6 and P4.13 pins (negative injection not allowed).

Table 7. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-55 to +150	°C
T_J	Maximum junction temperature (see *Section 5.2: Thermal characteristics on page 48*)		

Typical application current consumption

Table 11. Typical consumption in Run mode at 25°C and 85°C

Conditions		f_{MCLK} (MHz)	f_{ADC} (MHz)	Typical I_{DD} (mA)
V_{DD}= 5.5 V, RC oscillator off, PLL on, RTC enabled, 1 Timer (TIM) running, and ADC running in scan mode.	Code executing in RAM	10	10	20
		20		29
		36	9	42
	Code executing in Flash	10	10	22
		20		32
		36	9	48

Table 12. Typical consumption in Run and low power modes at 25°C

Mode	Conditions	f_{MCLK}	Typical I_{DD}
RUN	All peripherals on, RAM execution	36 MHz	76 mA
		24 MHz	56 mA
WFI	Main voltage regulator on, Flash on, EIC on, WIU on, GPIOs on.	36 MHz	33 mA
		24 MHz	31 mA
SLOW	PLL off, main voltage regulator on	4 MHz	11 mA
	CLOCK2/16, main voltage regulator on	250 kHz	8 mA
	CLOCK2/16, main voltage regulator off	250 kHz	3 mA
	RC oscillator running in low frequency, main crystal oscillator off, main voltage regulator off	29 kHz	2.5 mA
LPWFI	CLOCK2/16, main voltage regulator off, LP voltage regulator = 2 mA, Flash in power down mode.	250 kHz	528 µA
STOP	Main voltage regulator off, RTC on, RC oscillator off, LP voltage regulator = 6 mA	-	378 µA
	Main voltage regulator off, RTC off, RC oscillator off, LP voltage regulator = 6 mA	-	83 µA
	Main voltage regulator off, RTC off, RC oscillator off, LP voltage regulator = 4 mA	-	64 µA
	Main voltage regulator off, RTC off, RC oscillator off, LP voltage regulator = 2 mA	-	44 µA
HALT	RTC off, LP voltage regulator = 2 mA	-	44 µA

On-chip peripherals

Table 13. Peripheral current consumption at T_A= 25°C

Symbol	Parameter	Conditions	Typ	Unit
$I_{DD(RC)}$	RC (backup oscillator) supply current	High frequency	120	µA
		Low frequency	60	µA
$I_{DD(TIM)}$	TIM timer supply current [1]	f_{MCLK}=36 MHz	350	µA
$I_{DD(BSPI)}$	BSPI supply current [1]		1.1	mA
$I_{DD(UART)}$	UART supply current [1]		850	µA
$I_{DD(I2C)}$	I2C supply current [1]		430	µA
$I_{DD(ADC)}$	ADC supply current when converting [2]		5	mA
$I_{DD(EIC)}$	EIC supply current		2.88	mA
$I_{DD(CAN)}$	CAN supply current [1]		2.95	mA
$I_{DD(GPIO)}$	GPIO supply current		150	µA
$I_{DD(TB)}$	TB supply current		250	µA
$I_{DD(PWM)}$	PWM supply current		240	µA
$I_{DD(RTC)}$	RTC supply current		370	µA
$I_{DD(DMA)}$	DMA supply current		2.5	mA
$I_{DD(ARB)}$	Native arbiter supply current		180	µA
$I_{DD(AHB)}$	AHB arbiter supply current		570	µA
$I_{DD(WUT)}$	WUT supply current		300	µA
$I_{DD(WIU)}$	WIU supply current		460	µA

1. Data based on a differential I_{DD} measurement between the on-chip peripheral when kept under reset, not clocked and the on-chip peripheral when clocked and not kept under reset. This measurement does not include the pad toggling consumption.
2. Data based on a differential I_{DD} measurement between reset configuration and continuous A/D conversions.

Main oscillator characteristics

V_{DD} = 5 V ± 10%, T_A = -40° C to T_{Amax}, unless otherwise specified.

Table 14. Main oscillator characteristics

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
f_{OSC}	Oscillator frequency		4		8	MHz
g_m	Oscillator transconductance		1.5		4.2	mA/V
V_{OSC} 1)	Oscillation amplitude	f_{OSC} = 4 MHz, T_A= 25° C	-	2.4	-	V
		f_{OSC} = 8 MHz, T_A= 25° C		1.-		
V_{AV} 1)	Oscillator operating point	Sine wave middle, T_A= 25° C	-	0.77	-	v
t_{STUP} 1)	Oscillator start-up time	External crystal, V_{DD} = 5.5 V, f_{OSC} = 4 MHz, T_A=-40° C	-	-	12	ms
		External crystal, V_{DD} = 5.0 V, f_{OSC} = 4 MHz, T_A=25° C	-	5.5	-	ms
		External crystal, V_{DD} = 5.5 V, f_{OSC} = 6 MHz, T_A=-40° C	-	-	8	ms
		External crystal, V_{DD} = 5.0 V, f_{OSC} = 6 MHz, T_A=25° C	-	3.3	-	ms
		External crystal, V_{DD} = 5.5 V, f_{OSC} = 8 MHz, T_A=-40° C	-	-	7	ms
		External crystal, V_{DD} = 5.0 V, f_{OSC} = 8 MHz, T_A= 25° C	-	2.7	-	ms

RC/backup oscillator characteristics

V_{DD} = 5V ± 10%, T_A = -40°C to T_{Amax}, unless otherwise specified.

Table 15. RC oscillator characteristics

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
f_{RC}	RC frequency	High frequency mode [1]		2.35		MHz
		Low frequency mode[1]		29		kHz
f_{RCHF}	RC high frequency	CMU_RCCTL = 0x0	3			MHz
		CMU_RCCTL = 0xF			2.3	MHz
f_{RCLF}	RC low frequency	CMU_RCCTL = 0x0	35			kHz
		CMU_RCCTL = 0xF			30	kHz
f_{RCHFS}[2]	RC high frequency stability	Fixed CMU_RCCTL			10	%
f_{RCLFS}[2]	RC low frequency stability	Fixed CMU_RCCTL			23	%
t_{RCSTUP}	RC start-up time	Stable V_{DD}, f_{RC} = 2.35 MHz, T_A = 25°C		2.35		µs

1) CMU_RCCTL = 0x8

2) RC frequency shift versus average value (%)

PLL electrical characteristics

V_{DD} = 5 V ± 10%, T_A = -40° C to T_{Amax}, unless otherwise specified

Table 16. PLL characteristics

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
f_{PLLIN} (1)	PLL reference clock	FREF_RANGE = '0' FREF_RANGE = '1'	1.5 3.0		3.0 5.0	MHz
f_{PLLOUT}	PLL output clock	MX = "00" MX = "01" MX = "10" MX = "11"	20 x f_{PLLIN} 12 x f_{PLLIN} 28 x f_{PLLIN} 16 x f_{PLLIN}			MHz
f_{MCLK}	System clock	DX = 1..7	f_{PLLOUT}/DX		36	MHz
f_{FREE} (2)	PLL free running frequency	FREF_RANGE = '0', MX0 = '1' FREF_RANGE = '0', MX0 = '0' FREF_RANGE = '1', MX0 = '1' FREF_RANGE = '1', MX0 = '0'		120 240 240 480		kHz
t_{LOCK} (3)	PLL lock time	Stable oscillator (f_{PLLIN} = 4 MHz), stable V_{DD}		100	300	µs
Δt_{PKJIT}	PLL jitter (pk to pk)	f_{PLLIN} = 4 MHz (pulse generator)			1.5	ns

1. f_{PLLIN} is obtained from f_{OSC} directly or through an optional divider by 2.
2. Typical data are based on T_A=25°C, V_{DD}=5V
3. Max value is guaranteed by characterization, not tested in production.

Table 17. Low-power mode wake-up timing

Symbol	Parameter	Conditions	Typ	Unit
t_{WUHALT}	Wake-up from HALT mode		200	µs
t_{WUSTOP}	Wake-up from STOP mode	RC high frequency in STOP mode	180	µs
		RC low frequency in STOP mode	234	µs
$t_{WULPWFI}$ 1)	Wake-up from LPWFI mode	Main voltage regulator on RC oscillator off f_{OSC} = 4 MHz, f_{MCLK}= f_{OSC}/16 RAM or FLASH execution	27	µs
		Main voltage regulator on RC oscillator = high frequency Flash execution	46	µs
		Main voltage regulator on RC oscillator = low frequency Flash execution	3.6	ms

1. Flash memory programmed to enter Power Down mode during LPWFI.

4.3.4 EMC characteristics

Susceptibility tests are performed on a sample basis during product characterization.

Functional EMS (electromagnetic susceptibility)

Based on a simple running application on the product (toggling 2 LEDs through I/O ports), the product is stressed by two electromagnetic events until a failure occurs (indicated by the LEDs).

- **ESD**: Electrostatic discharge (positive and negative) is applied on all pins of the device until a functional disturbance occurs. This test conforms with the IEC 1000-4-2 standard.
- **FTB**: A burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test conforms with the IEC 1000-4-4 standard.

A device reset allows normal operations to be resumed. The test results are given in the table below based on the EMS levels and classes defined in application note AN1709.

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations:

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical data corruption (control registers...)

Prequalification trials:

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the RESET pin or the oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Table 19. EMS data

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD}=5 V, T_A=+25° C, f_{MCLK}=36 MHz conforms to IEC 1000-4-2	4A
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD}=5 V, T_A=+25° C, f_{MCLK}=36 MHz conforms to IEC 1000-4-4	4A

sample. This test conforms to the EIA/JESD 78 IC latch-up standard. For more details, refer to the application note AN1181.

- **DLU**: Electrostatic discharges (one positive then one negative test) are applied to each pin of 3 samples when the micro is running to assess the latch-up performance in dynamic mode. Power supplies are set to the typical values, the oscillator is connected as near as possible to the pins of the micro and the component is put in reset mode. This test conforms to the IEC1000-4-2 and SAEJ1752/3 standards. For more details, refer to the application note AN1181.

Table 22. Electrical sensitivities

Symbol	Parameter	Conditions	Class [1]
LU	Static latch-up class	T_A=+25°C T_A=+85°C T_A=+105°C	A A A
DLU	Dynamic latch-up class	V_{DD}= 5.5 V, f_{OSC4M} = 4 MHz, f_{MCLK} = 32 MHz, T_A = +25° C	A

1. Class description: A Class is an STMicroelectronics internal specification. All its limits are higher than the JEDEC specifications, that means when a device belongs to Class A it exceeds the JEDEC standard. B Class strictly covers all the JEDEC criteria (international standard).

Figure 15. V_{OH} JTDO pin vs I_{OL} @ V_{DD} 5 V

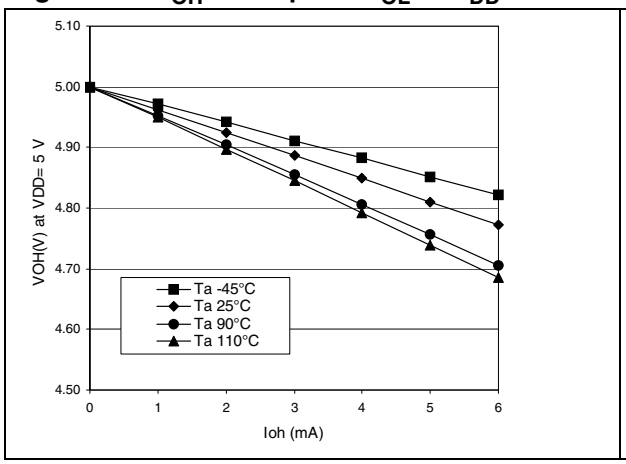


Figure 16. V_{OL} JTDO pin vs I_{OL} @ V_{DD} 5 V

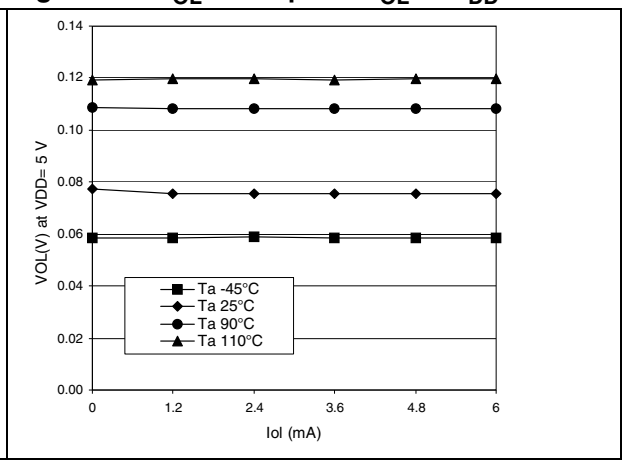


Figure 17. V_{OH} P6.0 pin vs I_{OL} @ V_{DD} 5 V

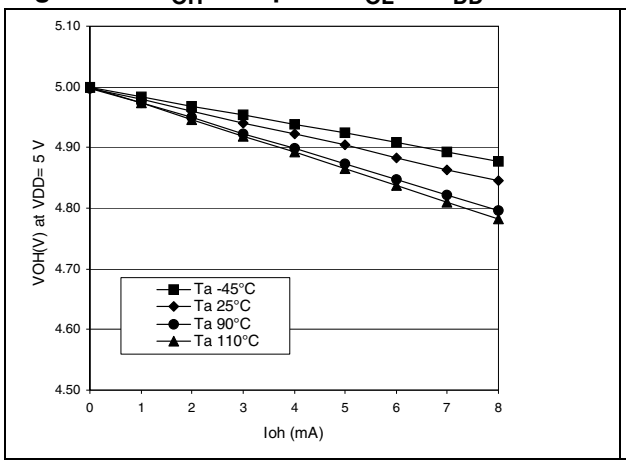
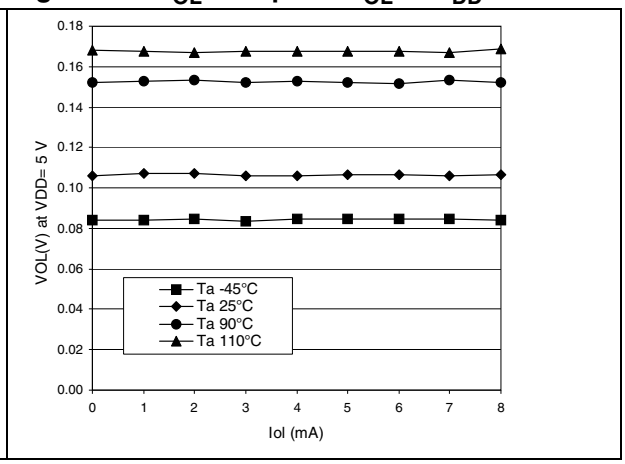


Figure 18. V_{OL} P6.0 pin vs I_{OL} @ V_{DD} 5 V



4.3.6 10-bit ADC characteristics

Subject to general operating conditions for V_{DDA}, f_{MCLK}, and T_A unless otherwise specified.

Table 26. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
f_{ADC}			0.4		10	MHz
V_{AIN}	Conversion voltage range [2]		V_{SSA}		V_{DDA}	V
I_{lkg}	Negative input leakage current on analog pins	$V_{IN}<V_{SS,}$ | I_{IN} |< 400 µA on adjacent analog pin		5	6	µA
C_{ADC}	Internal sample and hold capacitor				3.5	pF
t_{CAL} [2]	Calibration time	f_{ADC} = 10 MHz	580.2			µs
			5802			$1/f_{ADC}$
t_S [3]	Sampling time	f_{ADC} = 10 MHz	1		14	µs
t_{CONV}	Total conversion time (including sampling time)	f_{ADC} = 10 MHz	3			µs
			30 (10 for sampling +20 for successive approximation)			$1/f_{ADC}$
I_{ADC}	Running mode	Normal mode			5	mA
	Power-down mode				1	µA

1. Unless otherwise specified, typical data are based on T_A=25°C and V_{DDA}-V_{SS}=5.0V. They are given only as design guidelines and are not tested.
2. Calibration is recommended once after each power-up.
3. During the sample time the input capacitance C_{AIN} (6.8 max) can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_S. After the end of the sample time t_S, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_S depend on programming.

Analog power supply and reference pins

The V_{DDA} and V_{SSA} pins are the analog power supply of the A/D converter cell. They act as the high and low reference voltages for the conversion.

Separation of the digital and analog power pins allow board designers to improve A/D performance. Conversion accuracy can be impacted by voltage drops and noise in the event of heavily loaded or badly decoupled power supply lines (see*: General PCB design guidelines*).

General PCB design guidelines

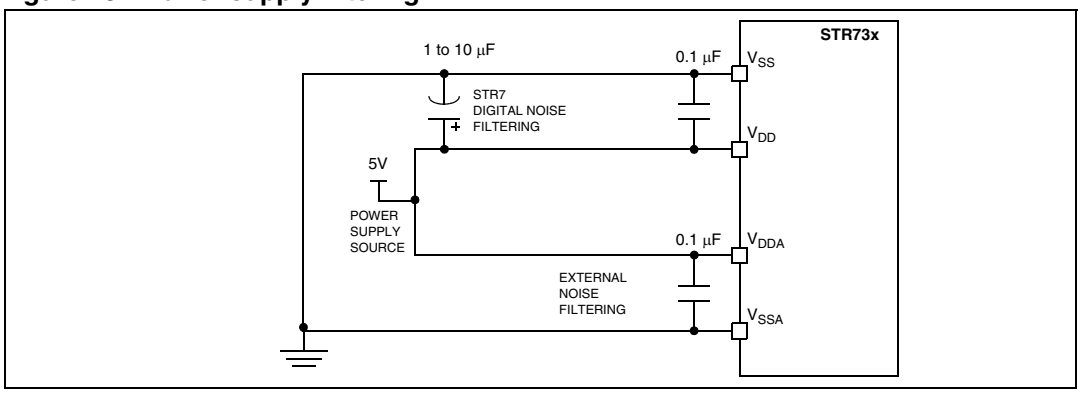
To obtain best results, some general design and layout rules should be followed when designing the application PCB to shield the noise-sensitive, analog physical interface from noise-generating CMOS logic signals.

- Use separate digital and analog planes. The analog ground plane should be connected to the digital ground plane via a single point on the PCB.
- Filter power to the analog power planes. It is recommended to connect capacitors, with good high frequency characteristics, between the power and ground lines, placing 0.1 µF and optionally, if needed 10 pF capacitors as close as possible to the STR7 power supply pins and a 1 to 10 µF capacitor close to the power source (see *Figure 23*).
- The analog and digital power supplies should be connected in a star network. Do not use a resistor, as V_{DDA} is used as a reference voltage by the A/D converter and any resistance would cause a voltage drop and a loss of accuracy.
- Properly place components and route the signal traces on the PCB to shield the analog inputs. Analog signals paths should run over the analog ground plane and be as short as possible. Isolate analog signals from digital signals that may switch while the analog inputs are being sampled by the A/D converter. Do not toggle digital outputs near the A/D input being converted.

Software filtering of spurious conversion results

For EMC performance reasons, it is recommended to filter A/D conversion outliers using software filtering techniques.

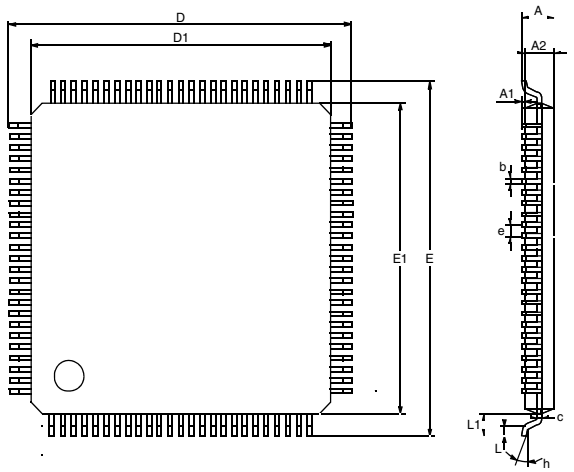
Figure 23. Power supply filtering



5 Package characteristics

5.1 Package mechanical data

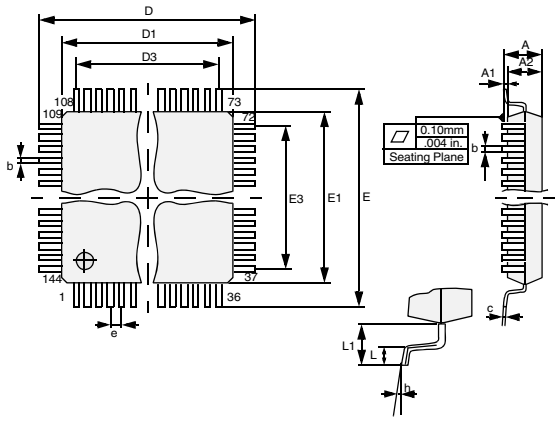
Figure 24. 100-pin thin quad flat package



Dim.	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A			1.60			0.0630
A1	0.05		0.15	0.0020		0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b	0.17	0.22	0.27	0.0067	0.0087	0.0106
C	0.09		0.20	0.0035		0.0079
D		16.00			0.6299	
D1		14.00			0.5512	
E		16.00			0.6299	
E1		14.00			0.5512	
e		0.50			0.0197	
h	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1		1.00			0.0394	
	Number of Pins					
N	100					

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 25. 144-pin thin quad flat package



Dim.	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A			1.60			0.0630
A1	0.05		0.15	0.0020		0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b	0.17	0.22	0.27	0.0067	0.0087	0.0106
c	0.09		0.20	0.0035		0.0079
D	21.80	22.00	22.20	0.8583	0.8661	0.8740
D1	19.80	20.00	20.20	0.7795	0.7874	0.7953
D3		17.50			0.6890	
E	21.80	22.00	22.20	0.8583	0.8661	0.8740
E1	19.80	20.00	20.20	0.7795	0.7874	0.7953
E3		17.50			0.6890	
e		0.50			0.0197	
K	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1		1.00			0.0394	
	Number of Pins					
N	144					

1. Values in inches are converted from mm and rounded to 4 decimal digits.

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