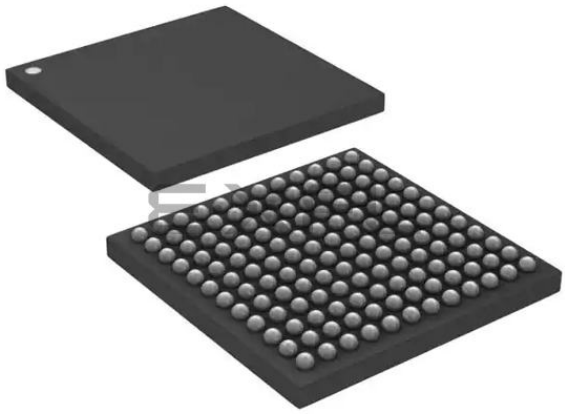

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM7®
Core Size	32-Bit Single-Core
Speed	36MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	112
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LFBGA
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/str735fz2h7

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1 Scope

This datasheet provides the STR73x ordering information, mechanical and electrical device characteristics.

For complete information on the STR73xF microcontroller memory, registers and peripherals. please refer to the STR73x reference manual.

For information on programming, erasing and protection of the internal Flash memory please refer to the STR7 Flash programming reference manual.

For information on the ARM7TDMI core please refer to the ARM7TDMI technical reference manual.

1.1 Description

ARM core with embedded Flash & RAM

STR73xF family combines the high performance ARM7TDMI™ CPU with an extensive range of peripheral functions and enhanced I/O capabilities. All devices have on-chip high-speed single voltage Flash memory and high-speed RAM. The STR73xF family has an embedded ARM core and is therefore compatible with all ARM tools and software.

Extensive tools support

STMicroelectronics' 32-bit, ARM core-based microcontrollers are supported by a complete range of high-end and low-cost development tools to meet the needs of application developers. This extensive line of hardware/software tools includes starter kits and complete development packages all tailored for ST's ARM core-based MCUs.

The range of development packages includes third-party solutions that come complete with a graphical development environment and an in-circuit emulator/programmer featuring a JTAG application interface. These support a range of embedded operating systems (OS), while several royalty-free OSs are also available.

For more information, please refer to ST MCU site http://www.st.com/mcu

Figure 1 shows the general block diagram of the device family.

clock/calendar/alarm function. When the STR73xF is in LPWFI mode the RTC keeps running, powered by the low power voltage regulator.

UARTs

The 4 UARTs allow full duplex, asynchronous, communications with external devices with independently programmable TX and RX baud rates up to 625 Kbaud.

Buffered serial peripheral interfaces (BSPI)

Each of the three BSPIs allow full duplex, synchronous communications with external devices, master or slave communication at up to 6 Mb/s in master mode and up to 4.5 Mb/s in slave mode (@36 MHz system clock).

I^2C interfaces

The two I^2C Interfaces provide multi-master and slave functions, support normal and fast I^2C mode (400 kHz) and 7 or 10-bit addressing modes.

A/D converter

The 10-bit analog to digital converter, converts up to 16 channels in single-shot or continuous conversion modes (12 channels in 100-pin devices). The minimum conversion time is 3 µs.

Watchdog

The 16-bit watchdog timer protects the application against hardware or software failures and ensures recovery by generating a reset.

I/O ports

Up to 112 I/O ports (72 in 100-pin devices) are programmable as general purpose input/output or alternate function.

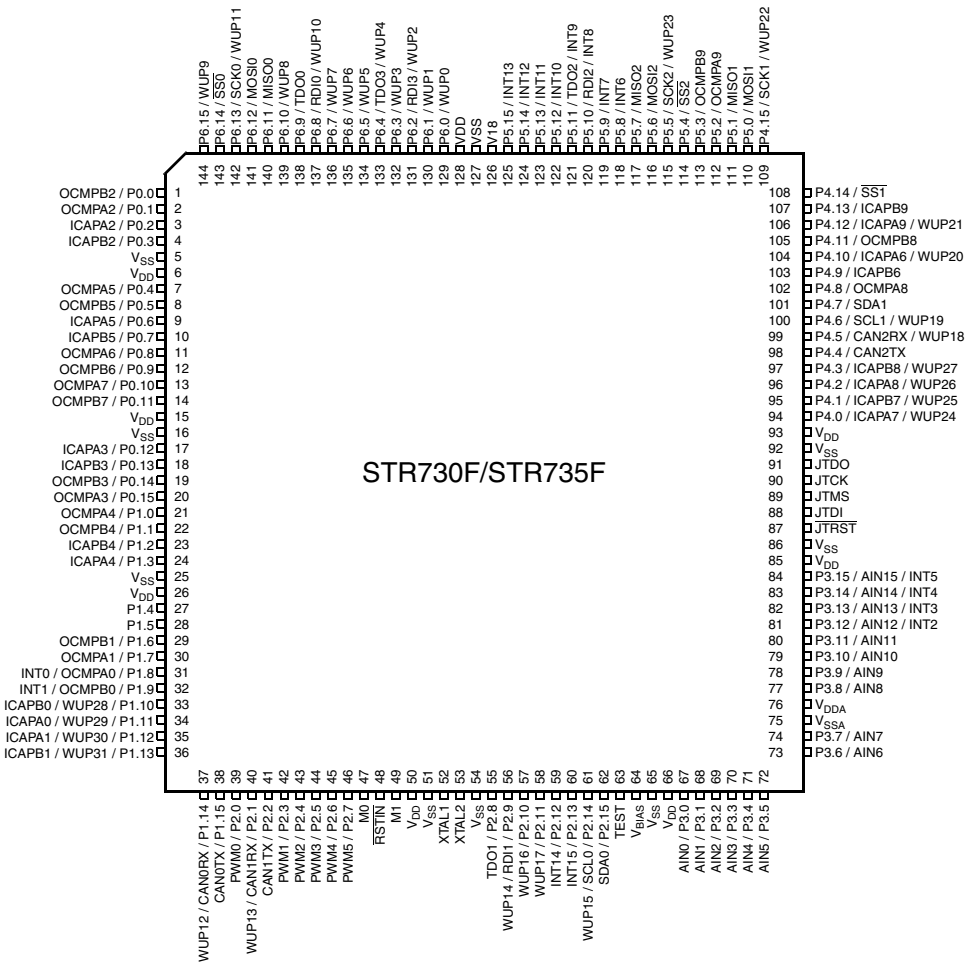
External interrupts and wake-up lines

16 external interrupts lines are available for application use. In addition, up to 32 external Wake-up lines (18 in 100-pin devices) can be used as general purpose interrupts or to wake-up the application from STOP mode.

3.2 Pin description

3.2.1 STR730F/STR735F (TQFP144)

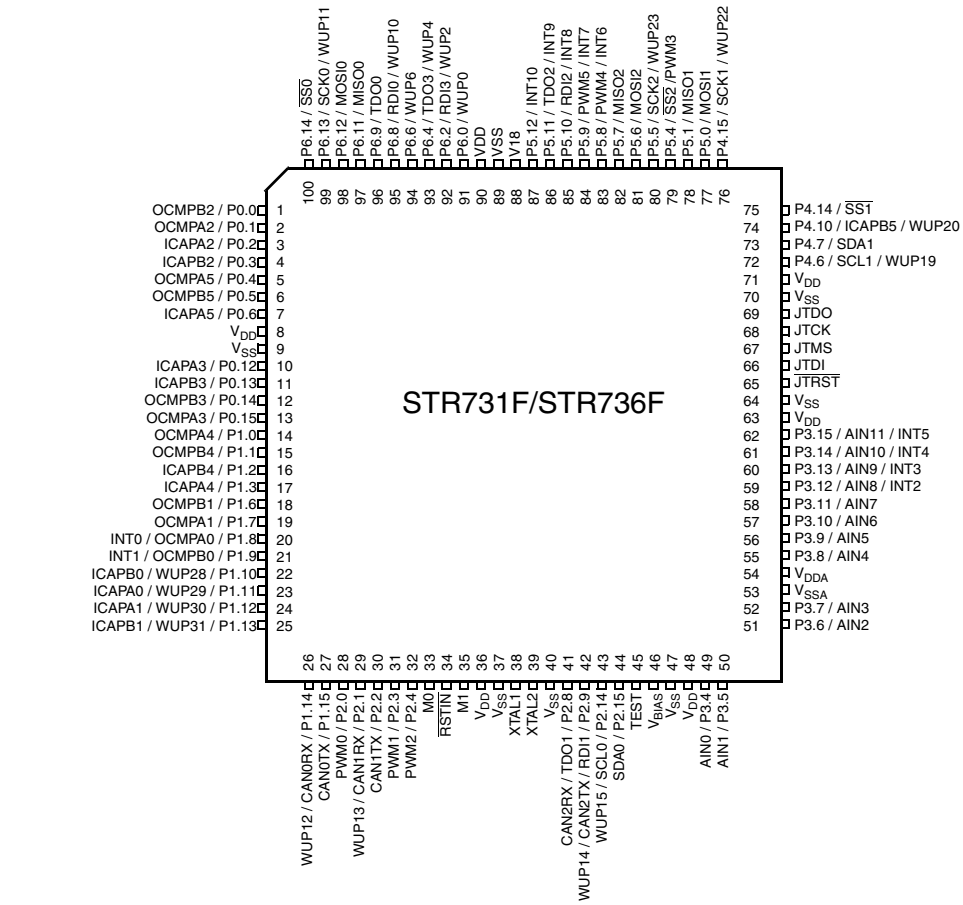
Figure 3. STR730F/STR735F pin configuration (top view)



Note: CAN alternate functions not available on STR735F.

3.2.3 STR731F/STR736F (TQFP100)

Figure 4. STR731F/STR736F pin configuration (top view)



Note: CAN alternate functions not available on STR736F.

Table 4. STR73xF pin description

Pin n°			Pin name	Type	Input			Output			Main function (after reset)	Alternate function
TQFP144	LFBGA144	TQFP100			Input Level	pu/pd	interrupt	Capability	OD	PP		
19	F3	12	P0.14/OCMPB3	I/O	T_T			2mA	X	X	Port 0.14	TIM3: output compare B output
20	F4	13	P0.15/OCMPA3	I/O	T_T			2mA	X	X	Port 0.15	TIM3: output compare A output
21	F5	14	P1.0/OCMPA4	I/O	T_T			2mA	X	X	Port 1.0	TIM4: output compare A output
22	F6	15	P1.1/OCMPB4	I/O	T_T			2mA	X	X	Port 1.1	TIM4: output compare B output
23	G2	16	P1.2/ICAPB4	I/O	T_T			2mA	X	X	Port 1.2	TIM4: input capture B input
24	G3	17	P1.3/ICAPA4	I/O	T_T			2mA	X	X	Port 1.3	TIM4: input capture A input
25	G4		V_{SS}	S							Ground	
26	H1		V_{DD}	S							Supply voltage (5 V)	
27	J1		P1.4	I/O	T_T			2mA	X	X	Port 1.4	
28	G5		P1.5	I/O	T_T			2mA	X	X	Port 1.5	
29	K1	18	P1.6/OCMPB1	I/O	T_T			2mA	X	X	Port 1.6	TIM1: output compare B output
30	L1	19	P1.7/OCMPA1	I/O	T_T			2mA	X	X	Port 1.7	TIM1: output compare A output
31	H2	20	P1.8/OCMPA0	I/O	T_T		INT0	2mA	X	X	Port 1.8	TIM0: output compare A output
32	H3	21	P1.9/OCMPB0	I/O	T_T		INT1	2mA	X	X	Port 1.9	TIM0: output compare B output
33	H4	22	P1.10/ICAPB0	I/O	T_T		WUP28	2mA	X	X	Port 1.10	TIM0: input capture B input
34	J2	23	P1.11/ICAPA0	I/O	T_T		WUP29	2mA	X	X	Port 1.11	TIM0: input capture A input
35	J3	24	P1.12/ICAPA1	I/O	T_T		WUP30	2mA	X	X	Port 1.12	TIM1: input capture A input
36	K2	25	P1.13/ICAPB1	I/O	T_T		WUP31	2mA	X	X	Port 1.13	TIM1: input capture B input
37	M1	26	P1.14/CAN0RX	I/O	T_T		WUP12	2mA	X	X	Port 1.14	CAN0: receive data input
38	L2	27	P1.15/CAN0TX	I/O	T_T			2mA	X	X	Port 1.15	CAN0: transmit data output
39	L3	28	P2.0/PWM0	I/O	T_T			2mA	X	X	Port 2.0	PWM0: PWM output
40	K3	29	P2.1/CAN1RX	I/O	T_T		WUP13	2mA	X	X	Port 2.1	CAN1: receive data input
41	M4	30	P2.2/CAN1TX	I/O	T_T			2mA	X	X	Port 2.2	CAN1: transmit data output
42	L4	31	P2.3/PWM1	I/O	T_T			2mA	X	X	Port 2.3	PWM1: PWM output
43	M2	32	P2.4/PWM2	I/O	T_T			2mA	X	X	Port 2.4	PWM2: PWM output
44	M3		P2.5/PWM3	I/O	T_T			2mA	X	X	Port 2.5	PWM3: PWM output
45	K4		P2.6/PWM4	I/O	T_T			2mA	X	X	Port 2.6	PWM4: PWM output
46	J4		P2.7/PWM5	I/O	T_T			2mA	X	X	Port 2.7	PWM5: PWM output
47	M5	33	M0	I	T_T	pd					BOOT: mode selection 0 input	
48	L5	34	RSTIN	I	C_T	pu					Reset input	
49	K5	35	M1	I	T_T	pd					BOOT: mode selection 1 input	

3.3 Memory mapping

Figure 5 shows the various memory configurations of the STR73xF system. The system memory map (from 0x0000_0000 to 0xFFFF_FFFF) is shown on the left part of the figure, the right part shows maps of the Flash and APB areas. For flexibility the Flash or RAM addresses can be aliased to Block 0 addresses using the remapping feature

Most reserved memory spaces (gray shaded areas in *Figure 5*) are protected from access by the user code. When an access this memory space is attempted, an ABORT signal is generated. Depending on the type of access, the ARM processor will enter “prefetch abort” state (Exception vector 0x0000_000C) or “data abort” state (Exception vector 0x0000_0010). It is up to the application software to manage these abort exceptions.

Figure 5. Memory map

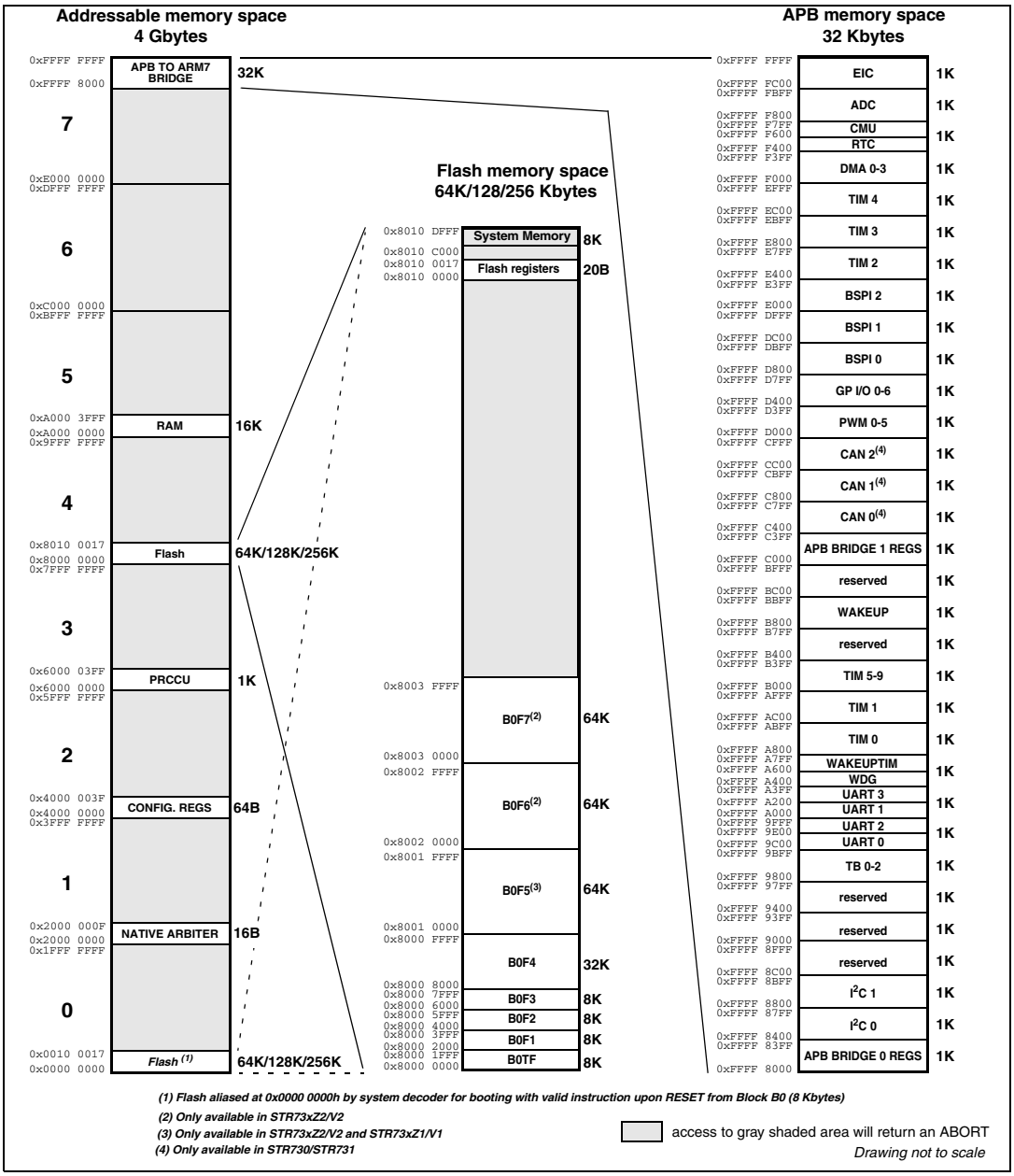


Table 7. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-55 to +150	°C
T_J	Maximum junction temperature (see *Section 5.2: Thermal characteristics on page 48*)		

4.3.1 Supply current characteristics

The current consumption is measured as described in *Figure 6* and *Figure 7*.

Total current consumption

The MCU is placed under the following conditions:

- All I/O pins in input mode with a static value at V_{DD} or V_{SS} (no load)
- All peripherals are disabled except if explicitly mentioned.

Subject to general operating conditions for V_{DD}, and T_A.

Table 10. Total current consumption

Symbol	Parameter	Conditions	Typ [1]	Max [2]	Unit
I_{DD}	RUN mode[3]	Formula, f_{MCLK} in MHz, RAM execution	7 + 1.9 f_{MCLK}		mA
		f_{MCLK} = 36 MHz, RAM execution	76		mA
		f_{MCLK} = 36 MHz, Flash execution	86		mA
	WFI mode	f_{OSC} = 4 MHz, f_{MCLK}= f_{OSC}/16 = 250 kHz Main voltage regulator ON, LP voltage regulator = 2 mA, RTC and WDG on, other modules off.	6.7	8	mA
	LPWFI mode	f_{RC} = high frequency (CMU_RCCTL= 0x8), f_{MCLK}= f_{RC} /16, LP voltage regulator = 2 mA, other modules off.	220	350	µA
	STOP mode	f_{OSC} = 4 MHz, RC oscillator on f_{RC} = high frequency (CMU_RCCTL= 0x0) LP voltage regulator = 6 mA, RTC and WUT ON, other modules off. Internal wake-up possible.	500	700	µA
		f_{RC} = high frequency (CMU_RCCTL= 0xF), LP voltage regulator = 2mA. WUT ON, other modules off. Internal wake-up possible.	150	220	
		LP voltage regulator = 2 mA, WIU on, Other modules off, external wake-up.	50	140	
	HALT mode	LP voltage regulator = 2 mA.	50	140	µA

1. Typical data are based on T_A=25° C, V_{DD}=5 V
2. Data based on characterization results, tested in production at V_{DD} max. and T_A = 25° C.
3. I/O in static configuration (not toggling). RUN mode is almost **independent of temperature**. On the contrary RUN mode current is **highly dependent on the application**. The I_{DDRUN} value can be significantly reduced by the application in the following ways: switch-off unused peripherals (default), reduce peripheral frequency through internal prescaler, fetch the most frequently-used functions from RAM and use low power mode when possible.

Figure 8. STOP I_{DD} vs. VDD

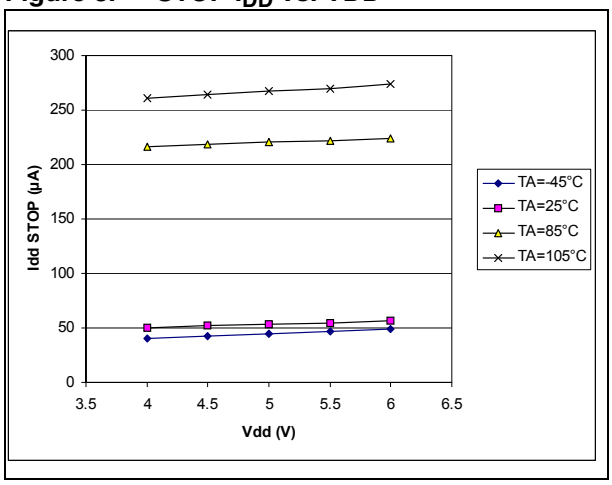


Figure 9. HALT I_{DD} vs. V_{DD}

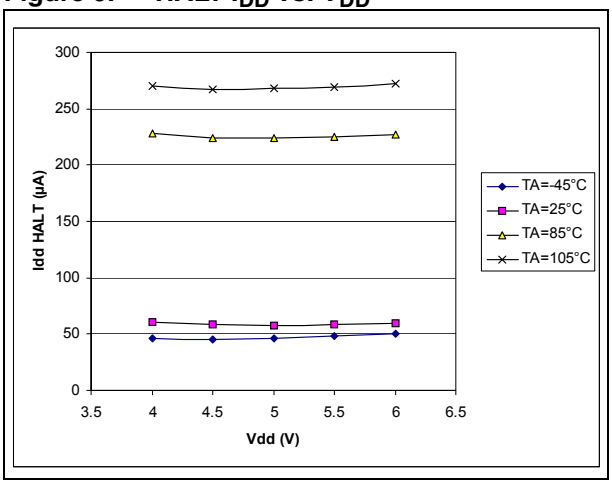


Figure 10. WFI I_{DD} vs. V_{DD}

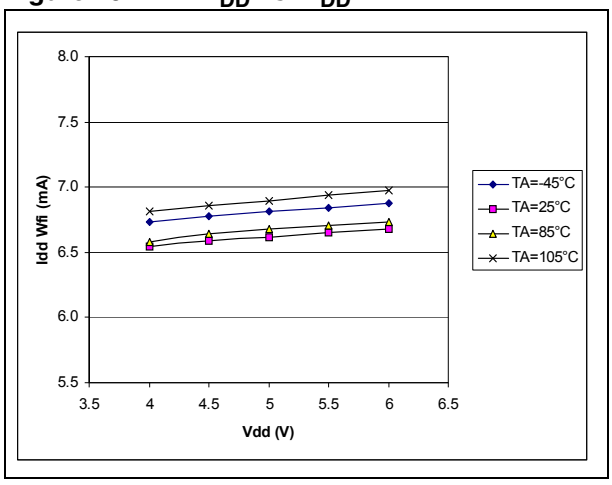
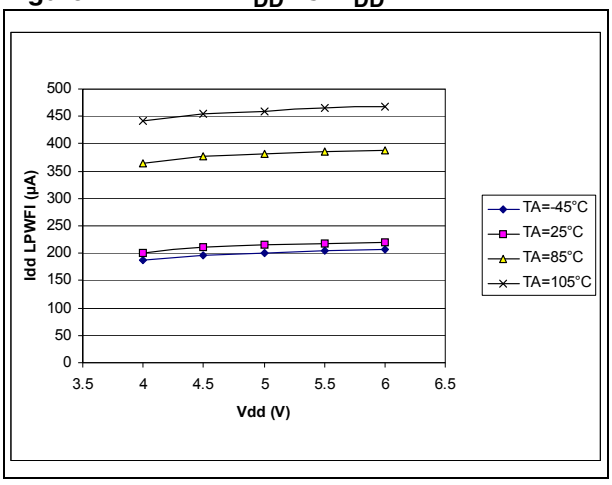


Figure 11. LPWFI I_{DD} vs. V_{DD}



Typical application current consumption

Table 11. Typical consumption in Run mode at 25°C and 85°C

Conditions		f_{MCLK} (MHz)	f_{ADC} (MHz)	Typical I_{DD} (mA)
V_{DD}= 5.5 V, RC oscillator off, PLL on, RTC enabled, 1 Timer (TIM) running, and ADC running in scan mode.	Code executing in RAM	10	10	20
		20		29
		36	9	42
	Code executing in Flash	10	10	22
		20		32
		36	9	48

Table 12. Typical consumption in Run and low power modes at 25°C

Mode	Conditions	f_{MCLK}	Typical I_{DD}
RUN	All peripherals on, RAM execution	36 MHz	76 mA
		24 MHz	56 mA
WFI	Main voltage regulator on, Flash on, EIC on, WIU on, GPIOs on.	36 MHz	33 mA
		24 MHz	31 mA
SLOW	PLL off, main voltage regulator on	4 MHz	11 mA
	CLOCK2/16, main voltage regulator on	250 kHz	8 mA
	CLOCK2/16, main voltage regulator off	250 kHz	3 mA
	RC oscillator running in low frequency, main crystal oscillator off, main voltage regulator off	29 kHz	2.5 mA
LPWFI	CLOCK2/16, main voltage regulator off, LP voltage regulator = 2 mA, Flash in power down mode.	250 kHz	528 µA
STOP	Main voltage regulator off, RTC on, RC oscillator off, LP voltage regulator = 6 mA	-	378 µA
	Main voltage regulator off, RTC off, RC oscillator off, LP voltage regulator = 6 mA	-	83 µA
	Main voltage regulator off, RTC off, RC oscillator off, LP voltage regulator = 4 mA	-	64 µA
	Main voltage regulator off, RTC off, RC oscillator off, LP voltage regulator = 2 mA	-	44 µA
HALT	RTC off, LP voltage regulator = 2 mA	-	44 µA

Main oscillator characteristics

V_{DD} = 5 V ± 10%, T_A = -40° C to T_{Amax}, unless otherwise specified.

Table 14. Main oscillator characteristics

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
f_{OSC}	Oscillator frequency		4		8	MHz
g_m	Oscillator transconductance		1.5		4.2	mA/V
V_{OSC} 1)	Oscillation amplitude	f_{OSC} = 4 MHz, T_A= 25° C	-	2.4	-	V
		f_{OSC} = 8 MHz, T_A= 25° C		1.-		
V_{AV} 1)	Oscillator operating point	Sine wave middle, T_A= 25° C	-	0.77	-	v
t_{STUP} 1)	Oscillator start-up time	External crystal, V_{DD} = 5.5 V, f_{OSC} = 4 MHz, T_A=-40° C	-	-	12	ms
		External crystal, V_{DD} = 5.0 V, f_{OSC} = 4 MHz, T_A=25° C	-	5.5	-	ms
		External crystal, V_{DD} = 5.5 V, f_{OSC} = 6 MHz, T_A=-40° C	-	-	8	ms
		External crystal, V_{DD} = 5.0 V, f_{OSC} = 6 MHz, T_A=25° C	-	3.3	-	ms
		External crystal, V_{DD} = 5.5 V, f_{OSC} = 8 MHz, T_A=-40° C	-	-	7	ms
		External crystal, V_{DD} = 5.0 V, f_{OSC} = 8 MHz, T_A= 25° C	-	2.7	-	ms

RC/backup oscillator characteristics

V_{DD} = 5V ± 10%, T_A = -40°C to T_{Amax}, unless otherwise specified.

Table 15. RC oscillator characteristics

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
f_{RC}	RC frequency	High frequency mode [1]		2.35		MHz
		Low frequency mode[1]		29		kHz
f_{RCHF}	RC high frequency	CMU_RCCTL = 0x0	3			MHz
		CMU_RCCTL = 0xF			2.3	MHz
f_{RCLF}	RC low frequency	CMU_RCCTL = 0x0	35			kHz
		CMU_RCCTL = 0xF			30	kHz
f_{RCHFS}[2]	RC high frequency stability	Fixed CMU_RCCTL			10	%
f_{RCLFS}[2]	RC low frequency stability	Fixed CMU_RCCTL			23	%
t_{RCSTUP}	RC start-up time	Stable V_{DD}, f_{RC} = 2.35 MHz, T_A = 25°C		2.35		µs

1) CMU_RCCTL = 0x8

2) RC frequency shift versus average value (%)

4.3.4 EMC characteristics

Susceptibility tests are performed on a sample basis during product characterization.

Functional EMS (electromagnetic susceptibility)

Based on a simple running application on the product (toggling 2 LEDs through I/O ports), the product is stressed by two electromagnetic events until a failure occurs (indicated by the LEDs).

- **ESD**: Electrostatic discharge (positive and negative) is applied on all pins of the device until a functional disturbance occurs. This test conforms with the IEC 1000-4-2 standard.
- **FTB**: A burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test conforms with the IEC 1000-4-4 standard.

A device reset allows normal operations to be resumed. The test results are given in the table below based on the EMS levels and classes defined in application note AN1709.

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations:

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical data corruption (control registers...)

Prequalification trials:

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the RESET pin or the oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Table 19. EMS data

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD}=5 V, T_A=+25° C, f_{MCLK}=36 MHz conforms to IEC 1000-4-2	4A
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD}=5 V, T_A=+25° C, f_{MCLK}=36 MHz conforms to IEC 1000-4-4	4A

4.3.5 I/O port pin characteristics

General characteristics

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified.

Table 23. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Input low level voltage [1]	TTL ports			0.8	V
V_{IH}	Input high level voltage [1]		2.0			
$I_{INJ(PIN)}$	Injected current on any I/O pin				±10	mA
$\Sigma I_{INJ(PIN)}$ [2]	Total injected current (sum of all I/O and control pins)				±75	mA
I_{lkg}	Input leakage current [3]	$V_{SS} \leq V_{IN} \leq V_{DD}$			±1	µA
I_S	Static current consumption [4]	Floating input mode		200		µA
R_{PU}	Weak pull-up equivalent resistor[5]	$V_{IN}=V_{SS}$	55	120	220	kΩ
R_{PD}	Weak pull-down equivalent resistor[5]	$V_{IN}=V_{DD}$	55	120	220	kΩ
C_{IO}	I/O pin capacitance			5		pF

1. Data based on characterization results, not tested in production.
2. When the current limitation is not possible, the V_{IN} absolute maximum rating must be respected, otherwise refer to $I_{INJ(PIN)}$ specification. A positive injection is induced by $V_{IN}>V_{33}$ while a negative injection is induced by $V_{IN}<V_{SS}$. Refer to *Section 4.2 on page 22* for more details.
3. Leakage could be higher than max. if negative current is injected on adjacent pins.
4. Configuration not recommended, all unused pins must be kept at a fixed voltage: using the output mode of the I/O for example or an external pull-up or pull-down resistor. Data based on design simulation and/or technology characteristics, not tested in production.
6. The R_{PU} pull-up and R_{PD} pull-down equivalent resistor are based on a resistive transistor (corresponding I_{PU} and I_{PD} current characteristics described in *Figure 19*).

Analog power supply and reference pins

The V_{DDA} and V_{SSA} pins are the analog power supply of the A/D converter cell. They act as the high and low reference voltages for the conversion.

Separation of the digital and analog power pins allow board designers to improve A/D performance. Conversion accuracy can be impacted by voltage drops and noise in the event of heavily loaded or badly decoupled power supply lines (see*: General PCB design guidelines*).

General PCB design guidelines

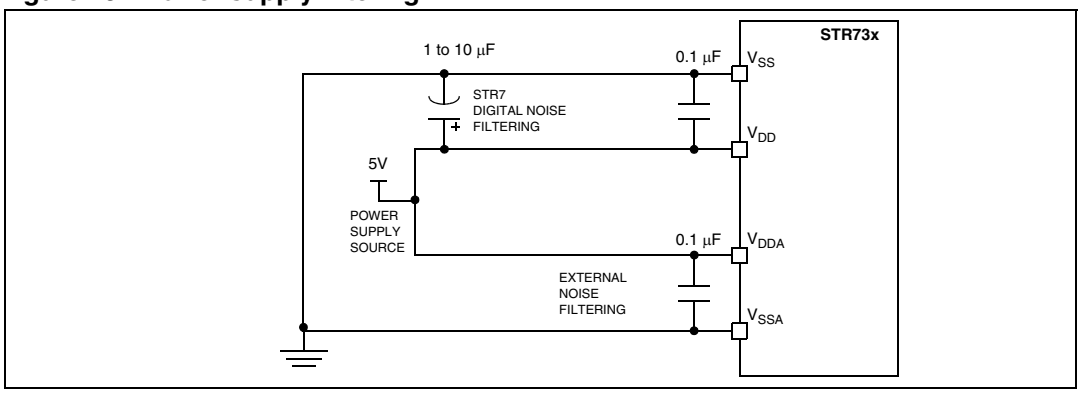
To obtain best results, some general design and layout rules should be followed when designing the application PCB to shield the noise-sensitive, analog physical interface from noise-generating CMOS logic signals.

- Use separate digital and analog planes. The analog ground plane should be connected to the digital ground plane via a single point on the PCB.
- Filter power to the analog power planes. It is recommended to connect capacitors, with good high frequency characteristics, between the power and ground lines, placing 0.1 µF and optionally, if needed 10 pF capacitors as close as possible to the STR7 power supply pins and a 1 to 10 µF capacitor close to the power source (see *Figure 23*).
- The analog and digital power supplies should be connected in a star network. Do not use a resistor, as V_{DDA} is used as a reference voltage by the A/D converter and any resistance would cause a voltage drop and a loss of accuracy.
- Properly place components and route the signal traces on the PCB to shield the analog inputs. Analog signals paths should run over the analog ground plane and be as short as possible. Isolate analog signals from digital signals that may switch while the analog inputs are being sampled by the A/D converter. Do not toggle digital outputs near the A/D input being converted.

Software filtering of spurious conversion results

For EMC performance reasons, it is recommended to filter A/D conversion outliers using software filtering techniques.

Figure 23. Power supply filtering



5.2 Thermal characteristics

The average chip-junction temperature, T_J, in degrees Celsius, may be calculated using the following equation:

$$T_J = T_A + (P_D \times \Theta_{JA}) \quad (1)$$

Where:

- T_A is the ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D is the sum of P_{INT} and $P_{I/O}$ ($P_D = P_{INT} + P_{I/O}$),
- P_{INT} is the product of I_{DD} and V_{DD}, expressed in Watts. This is the chip internal power,
- $P_{I/O}$ represents the power dissipation on input and output pins; user determined.

Most of the time for the applications $P_{I/O} < P_{INT}$ and may be neglected. On the other hand, $P_{I/O}$ may be significant if the device is configured to drive continuously external modules and/or memories.

An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is given by:

$$P_D = K / (T_J + 273°C) \quad (2)$$

Therefore (solving equations 1 and 2):

$$K = P_D \times (T_A + 273°C) + \Theta_{JA} \times P_D^2 \quad (3)$$

Where:

- K is a constant for the particular part, which may be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J may be obtained by solving equations (1) and (2) iteratively for any value of T_A

Table 28. Thermal characteristics

Symbol	Description	Package	Value (typical)	Unit
Θ_{JA}	Thermal resistance junction-ambient	LFBGA144	50	°C/W
		TQFP144	40	
		TQFP100	40	

6 Order codes

Table 29. Order codes

Partnumber	Flash Kbytes	Package	RAM Kbytes	TIM timers	6x PWM module	CAN periph	A/D chan.	Wake-up lines	I/O ports	Temp. range
STR730FZ1T6	128	TQFP144 20x20	16	10	1	3	16	32	112	-40 to +85°C
STR730FZ2T6	256									
STR730FZ1H6	128	LFBGA144 10x10								
STR730FZ2H6	256									
STR735FZ1T6	128	TQFP144 20x20				0				
STR735FZ2T6	256									
STR735FZ1H6	128	LFBGA144 10x10								
STR735FZ2H6	256									
STR731FV0T6	64	TQFP100 14x14		6		3	12	18	72	
STR731FV1T6	128									
STR731FV2T6	256									
STR736FV0T6	64	TQFP100 14x14				0				
STR736FV1T6	128									
STR736FV2T6	256									
STR730FZ1T7	128	TQFP144 20x20	16	10	1	3	16	32	112	-40 to +105°C
STR730FZ2T7	256									
STR730FZ1H7	128	LFBGA144 10x10								
STR730FZ2H7	256									
STR735FZ1T7	128	TQFP144 20x20				0				
STR735FZ2T7	256									
STR735FZ1H7	128	LFBGA144 10x10								
STR735FZ2H7	256									
STR731FV0T7	64	TQFP100 14x14		6		3	12	18	72	
STR731FV1T7	128									
STR731FV2T7	256									
STR736FV0T7	64	TQFP100 14x14				0				
STR736FV1T7	128									
STR736FV2T7	256									

7 Known limitations

7.1 Low power wait for interrupt mode

When the STR73x device is put in Low Power Wait For Interrupt mode (LPWFI), the Flash goes into low power mode or power down mode, depending on the setting of the PWD bit in the Flash Control Register 0 (default is '0', Low Power mode). This default mode can create excessive voltage conditions on the transistor gates and may affect the long term behavior of the Low Power mode circuitry.

Workaround

There is no workaround. If Low Power Wait For Interrupt mode is used, it is strongly suggested to configure the Flash to enter power down mode (bit PWD = '1').

7.2 PLL free running mode at high temperature

When the STR73x device is operated and an ambient temperature (T_A) of more than 55° C and the main system clock (f_{MCLK}) is sourced by the PLL in free running mode, the device may not work properly.

Workaround

At high temperature (more than 55° C), it is recommended to use the internal RC oscillator as a backup clock source rather than the PLL free running mode.

8 Revision history

Table 30. Document revision history

Date	Revision	Description of changes
19-Sep-2005	1	First release
02-Nov-2005	2	Removed Table 8 power consumption in LP modes Updated PLL frequency in *Section 1.1* and *Table 12*
08-Mar-2006	3	*Section 3.4: Preliminary power consumption data* updated *Section 3.5: DC electrical characteristics* updated *Section 7: Known limitations* added
04-Jun-2006	4	*Section 4: Electrical parameters* updated *Section 7: Known limitations* updated Added temperature range -40°C to 85°C in *Section 6: Order codes*
19-Jun-2006	5	Changed Flash data retention to 20 years at 85°C in *Table 18 on page 34*.
08-Sep-2006	6	Changed *Table 24: Output driving current on page 39* Added *Figure 14: VOL standard ports vs IOL @ VDD 5 V* thru *Figure 18: VOL P6.0 pin vs IOL @ VDD 5 V on page 40*. Added *Figure 20: NRSTIN RPU vs. VDD*
08-Jun-2008	7	Inch values rounded to 4 decimal digits in *Section 5.1: Package mechanical data* Modified BSPI speed in *Section 2.1: On-chip peripherals*