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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM7®
Core Size	32-Bit Single-Core
Speed	36MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	112
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/str735fz2t6

Contents

clock/calendar/alarm function. When the STR73xF is in LPWFI mode the RTC keeps running, powered by the low power voltage regulator.

UARTs

The 4 UARTs allow full duplex, asynchronous, communications with external devices with independently programmable TX and RX baud rates up to 625 Kbaud.

Buffered serial peripheral interfaces (BSPI)

Each of the three BSPIs allow full duplex, synchronous communications with external devices, master or slave communication at up to 6 Mb/s in master mode and up to 4.5 Mb/s in slave mode (@36 MHz system clock).

I^2C interfaces

The two I^2C Interfaces provide multi-master and slave functions, support normal and fast I^2C mode (400 kHz) and 7 or 10-bit addressing modes.

A/D converter

The 10-bit analog to digital converter, converts up to 16 channels in single-shot or continuous conversion modes (12 channels in 100-pin devices). The minimum conversion time is 3 µs.

Watchdog

The 16-bit watchdog timer protects the application against hardware or software failures and ensures recovery by generating a reset.

I/O ports

Up to 112 I/O ports (72 in 100-pin devices) are programmable as general purpose input/output or alternate function.

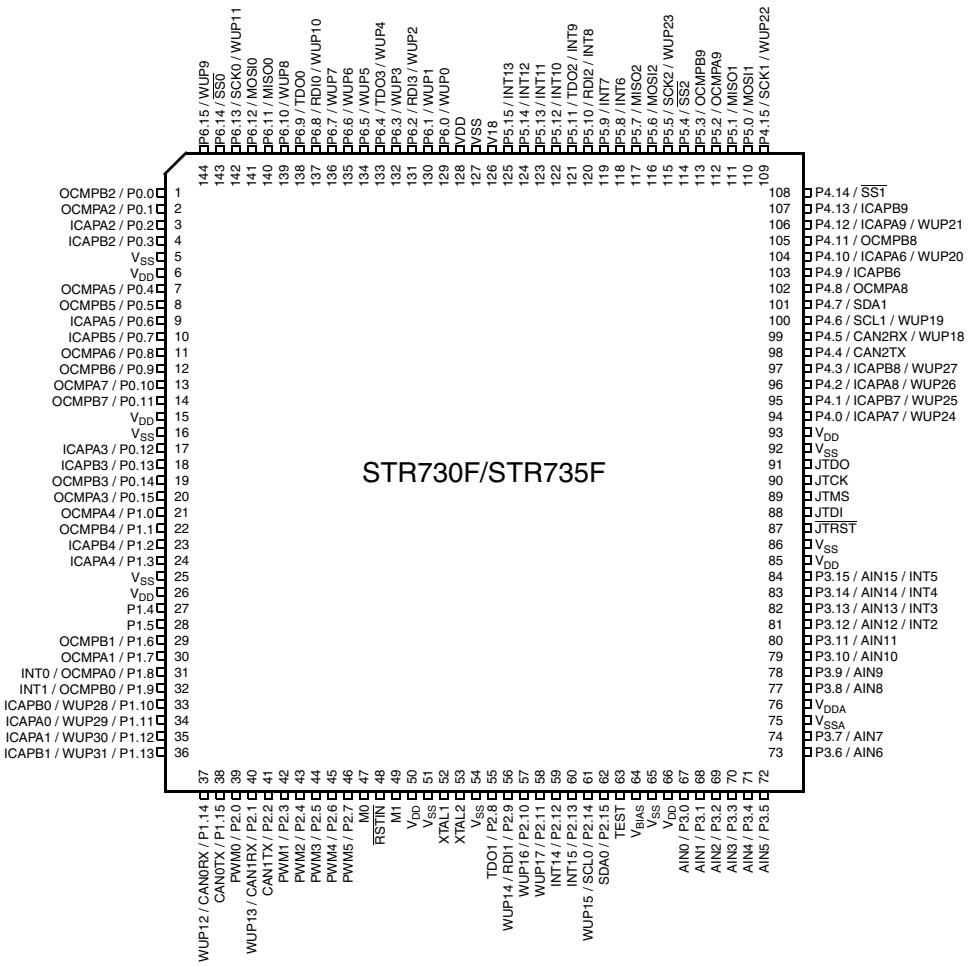
External interrupts and wake-up lines

16 external interrupts lines are available for application use. In addition, up to 32 external Wake-up lines (18 in 100-pin devices) can be used as general purpose interrupts or to wake-up the application from STOP mode.

3.2 Pin description

3.2.1 STR730F/STR735F (TQFP144)

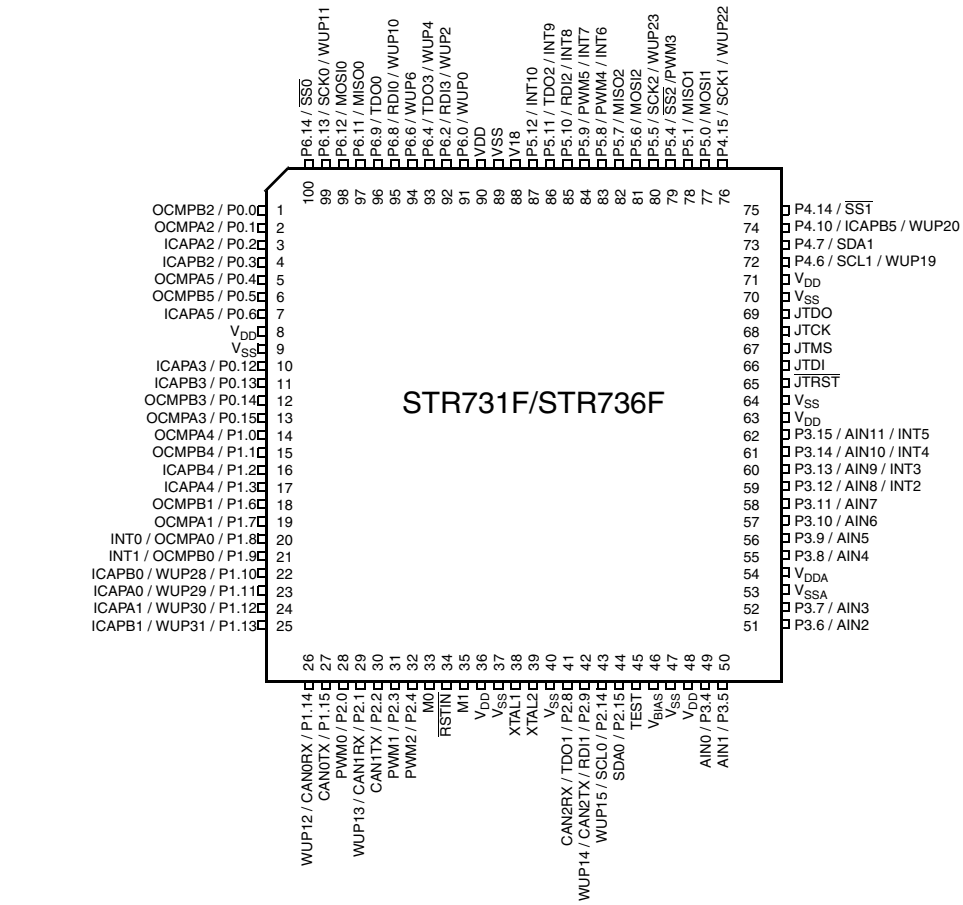
Figure 3. STR730F/STR735F pin configuration (top view)



Note: CAN alternate functions not available on STR735F.

3.2.3 STR731F/STR736F (TQFP100)

Figure 4. STR731F/STR736F pin configuration (top view)



Note: CAN alternate functions not available on STR736F.

Table 4. STR73xF pin description

Pin n°			Pin name	Type	Input			Output			Main function (after reset)	Alternate function
TQFP144	LFBGA144	TQFP100			Input Level	pu/pd	interrupt	Capability	OD	PP		
73	M12	51	P3.6/AIN6	I/O	T_T			2mA	X	X	Port 3.6	ADC: analog input 6 (AIN2 in TQFP100)
74	L11	52	P3.7/AIN7	I/O	T_T			2mA	X	X	Port 3.7	ADC: analog input 7 (AIN3 in TQFP100)
75	K11	53	V_{SSA}	S							Reference ground for A/D converter	
76	K10	54	V_{DDA}	S							Reference voltage for A/D converter	
77	J12	55	P3.8/AIN8	I/O	T_T			2mA	X	X	Port 3.8	ADC: analog input 8 (AIN4 in TQFP100)
78	J11	56	P3.9/AIN9	I/O	T_T			2mA	X	X	Port 3.9	ADC: analog input 9 (AIN5 in TQFP100)
79	L12	57	P3.10/AIN10	I/O	T_T			2mA	X	X	Port 3.10	ADC: analog input 10 (AIN6 in TQFP100)
80	K12	58	P3.11/AIN11	I/O	T_T			2mA	X	X	Port 3.11	ADC: analog input 11 (AIN7 in TQFP100)
81	J10	59	P3.12/AIN12	I/O	T_T		INT2	2mA	X	X	Port 3.12	ADC: analog input 12 (AIN8 in TQFP100)
82	J9	60	P3.13/AIN13	I/O	T_T		INT3	2mA	X	X	Port 3.13	ADC: analog input 13 (AIN9 in TQFP100)
83	H12	61	P3.14/AIN14	I/O	T_T		INT4	2mA	X	X	Port 3.14	ADC: analog input 14 (AIN10 in TQFP100)
84	H11	62	P3.15/AIN15	I/O	T_T		INT5	2mA	X	X	Port 3.15	ADC: analog input 15 (AIN11 in TQFP100)
85	H10	63	V_{DD}	S							Supply voltage (5 V)	
86	H9	64	V_{SS}	S							Ground	
87	G12	65	JTRST	I	T_T	pu						JTAG reset Input
88	F12	66	JTDI	I	T_T	pu						JTAG data input
89	H8	67	JTMS	I	T_T	pu						JTAG mode selection Input
90	G11	68	JTCK	I	T_T	pd						JTAG clock Input
91	G10	69	JTDO	O				4mA				JTAG data output. **Note:** Reset state = HiZ
92	G9	70	V_{SS}	S								Ground
93	G8	71	V_{DD}	S								Supply voltage (5 V)
94	G7		P4.0/ICAPA7	I/O	T_T		WUP24	2mA	X	X	Port 4.0	TIM7: input capture A input
95	F11		P4.1/ICAPB7	I/O	T_T		WUP25	2mA	X	X	Port 4.1	TIM7: input capture B input
96	F10		P4.2/ICAPA8	I/O	T_T		WUP26	2mA	X	X	Port 4.2	TIM8: input capture A input

Table 4. STR73xF pin description

Pin n°			Pin name	Type	Input			Output			Main function (after reset)	Alternate function	
TQFP144	LFBGA144	TQFP100			Input Level	pu/pd	interrupt	Capability	OD	PP			
97	F9		P4.3/ICAPB8	I/O	T_T		WUP27	2mA	X	X	Port 4.3	TIM8: input capture B input	
98	F8		P4.4/CAN2TX	I/O	T_T			2mA	X	X	Port 4.4	CAN2: transmit data output	
99	E12		P4.5/CAN2RX	I/O	T_T		WUP18	2mA	X	X	Port 4.5	CAN2: receive data input	
100	E11	72	P4.6/SCL1	I/O	T_T		WUP19	2mA	X	X	Port 4.6	I2C1: serial clock	
101	C12	73	P4.7/SDA1	I/O	T_T			2mA	X	X	Port 4.7	I2C1: serial data	
102	B12		P4.8/OCMPA8	I/O	T_T			2mA	X	X	Port 4.8	TIM8: output compare A output	
103	E10		P4.9/ICAPB6	I/O	T_T			2mA	X	X	Port 4.9	TIM6: input capture B input	
104	E9	74	P4.10/ICAPA6/ICAPB5	I/O	T_T		WUP20	2mA	X	X	Port 4.10	TIM6: input capture A input (144-pin pkg only)	TIM5: input capture B input (TQFP100 only)
105	D12		P4.11/OCMPB8	I/O	T_T			2mA	X	X	Port 4.11	TIM8: output compare B output	
106	D11		P4.12/ICAPA9	I/O	T_T		WUP21	2mA	X	X	Port 4.12	TIM9: input capture A input	
107	D10		P4.13/ICAPB9	I/O	T_T			2mA	X	X	Port 4.13	TIM9: input capture B input	
108	C11	75	P4.14/$\overline{SS}$1	I/O	T_T			2mA	X	X	Port 4.14	BSPI1: slave select	
109	B11	76	P4.15/SCK1	I/O	T_T		WUP22	2mA	X	X	Port 4.15	BSPI1: serial clock	
110	B10	77	P5.0/MOSI1	I/O	T_T			2mA	X	X	Port 5.0	BSPI1: master output/slave input	
111	C10	78	P5.1/MISO1	I/O	T_T			2mA	X	X	Port 5.1	BSPI1: master input/Slave output	
112	A9		P5.2/OCMPA9	I/O	T_T			2mA	X	X	Port 5.2	TIM9: output compare A output	
113	B9		P5.3/OCMPB9	I/O	T_T			2mA	X	X	Port 5.3	TIM9: output compare B output	
114	C9	79	P5.4/$\overline{SS}$2/PWM3	I/O	T_T			2mA	X	X	Port 5.4	BSPI2: slave select	PWM3: PWM output (TQFP100 only)
115	D9	80	P5.5/SCK2	I/O	T_T		WUP23	2mA	X	X	Port 5.5	BSPI2: serial clock	
116	A11	81	P5.6/MOSI2	I/O	T_T			2mA	X	X	Port 5.6	BSPI2: master output/slave input	
117	A10	82	P5.7/MISO2	I/O	T_T			2mA	X	X	Port 5.7	BSPI2: master input/slave output	
118	A8	83	P5.8/PWM4	I/O	T_T		INT6	2mA	X	X	Port 5.8	PWM4: PWM output (TQFP100 only)	

4.2 Absolute maximum ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 5. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DD} - V_{SS}	External 5 V Supply voltage	-0.3	6.0	V
V_{SSA}	Reference ground for A/D converter	V_{SS}	V_{SS}	V
V_{DDA}- V_{SSA}	Reference voltage for A/D converter	-0.3	V_{DD}+0.3	V
V_{IN}	Input voltage on any pin	-0.3	V_{DD}+0.3	
$\lvert\Delta V_{DDx}\rvert$	Variations between different 5 V power pins	-	0.3	mV
$\lvert V_{SSX}$ - $V_{SS}\rvert$	Variations between all the different ground pins	-	0.3	
$V_{ESD(HBM)}$	Electrostatic discharge voltage (Human Body Model)	see *: Absolute maximum ratings (electrical sensitivity) on page 36*		
$V_{ESD(MM)}$	Electrostatic discharge voltage (Machine Model)			

Table 6. Current characteristics

Symbol	Ratings	Max.	Unit
I_{VDD}	Total current into V_{DD} power lines (source) 1)	100	mA
I_{VSS}	Total current out of V_{SS} ground lines (sink) 1)	100	
I_{IO}	Output current sunk by any I/O and control pin	10	
	Output current source by any I/O and control pin	10	
$I_{INJ(PIN)}$ 2) & 3)	Injected current on any other pin 4) &5)	±10	
$\Sigma I_{INJ(PIN)}$ 2)	Total injected current (sum of all I/O and control pins) 4)	±75	

1. All 5 V power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external 5 V supply
2. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$.
3. Negative injection disturbs the analog performance of the device. See note in *Section 4.3.6: 10-bit ADC characteristics on page 43*.
4. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values). These results are based on characterization with $\Sigma I_{INJ(PIN)}$ maximum current injection on four I/O port pins of the device.

5.) In 144-pin devices, only +10 mA on P0.3, P1.13, P3.6 and P4.13 pins (negative injection not allowed).

4.3.1 Supply current characteristics

The current consumption is measured as described in *Figure 6* and *Figure 7*.

Total current consumption

The MCU is placed under the following conditions:

- All I/O pins in input mode with a static value at V_{DD} or V_{SS} (no load)
- All peripherals are disabled except if explicitly mentioned.

Subject to general operating conditions for V_{DD}, and T_A.

Table 10. Total current consumption

Symbol	Parameter	Conditions	Typ [1]	Max [2]	Unit
I_{DD}	RUN mode[3]	Formula, f_{MCLK} in MHz, RAM execution	7 + 1.9 f_{MCLK}		mA
		f_{MCLK} = 36 MHz, RAM execution	76		mA
		f_{MCLK} = 36 MHz, Flash execution	86		mA
	WFI mode	f_{OSC} = 4 MHz, f_{MCLK}= f_{OSC}/16 = 250 kHz Main voltage regulator ON, LP voltage regulator = 2 mA, RTC and WDG on, other modules off.	6.7	8	mA
	LPWFI mode	f_{RC} = high frequency (CMU_RCCTL= 0x8), f_{MCLK}= f_{RC} /16, LP voltage regulator = 2 mA, other modules off.	220	350	µA
	STOP mode	f_{OSC} = 4 MHz, RC oscillator on f_{RC} = high frequency (CMU_RCCTL= 0x0) LP voltage regulator = 6 mA, RTC and WUT ON, other modules off. Internal wake-up possible.	500	700	µA
		f_{RC} = high frequency (CMU_RCCTL= 0xF), LP voltage regulator = 2mA. WUT ON, other modules off. Internal wake-up possible.	150	220	
		LP voltage regulator = 2 mA, WIU on, Other modules off, external wake-up.	50	140	
	HALT mode	LP voltage regulator = 2 mA.	50	140	µA

1. Typical data are based on T_A=25° C, V_{DD}=5 V
2. Data based on characterization results, tested in production at V_{DD} max. and T_A = 25° C.
3. I/O in static configuration (not toggling). RUN mode is almost **independent of temperature**. On the contrary RUN mode current is **highly dependent on the application**. The I_{DDRUN} value can be significantly reduced by the application in the following ways: switch-off unused peripherals (default), reduce peripheral frequency through internal prescaler, fetch the most frequently-used functions from RAM and use low power mode when possible.

Figure 8. STOP I_{DD} vs. VDD

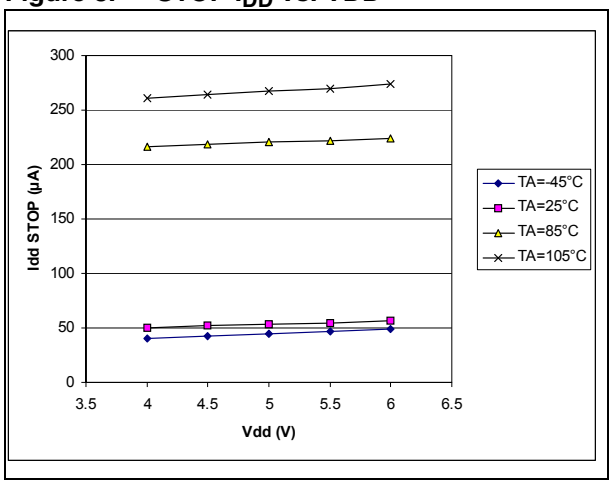


Figure 9. HALT I_{DD} vs. V_{DD}

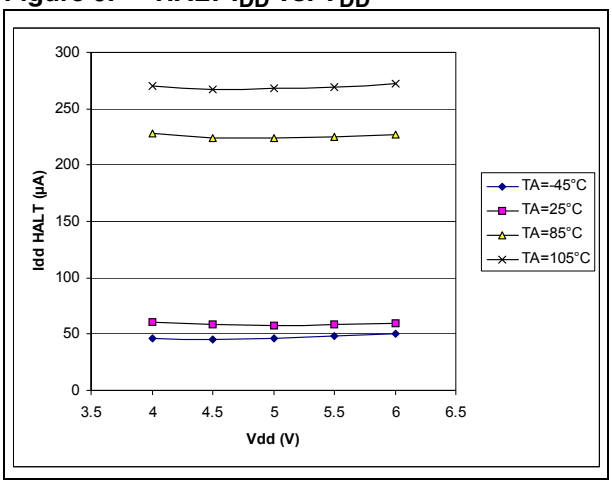


Figure 10. WFI I_{DD} vs. V_{DD}

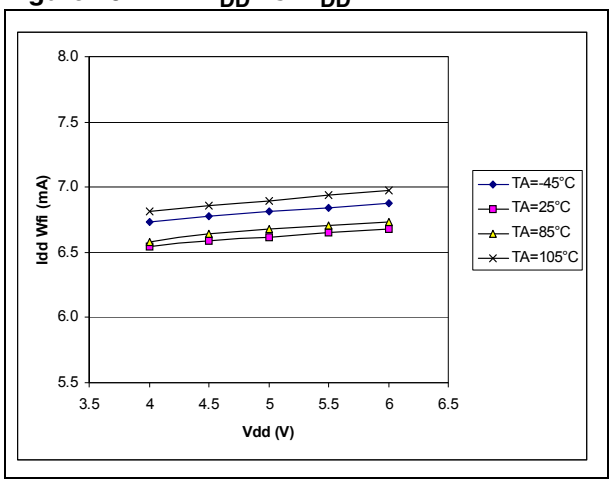
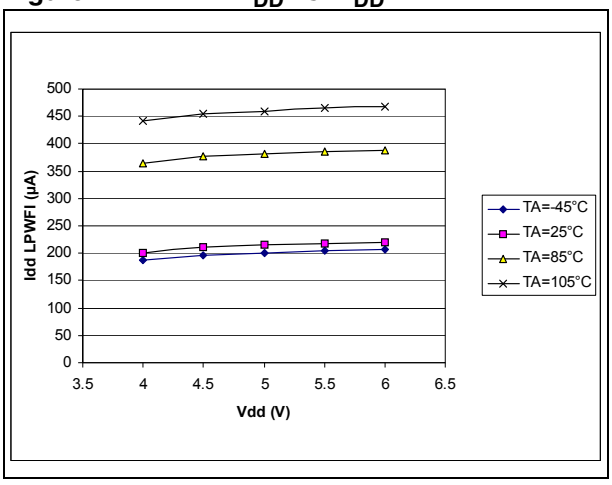


Figure 11. LPWFI I_{DD} vs. V_{DD}



On-chip peripherals

Table 13. Peripheral current consumption at T_A= 25°C

Symbol	Parameter	Conditions	Typ	Unit
$I_{DD(RC)}$	RC (backup oscillator) supply current	High frequency	120	µA
		Low frequency	60	µA
$I_{DD(TIM)}$	TIM timer supply current [1]	f_{MCLK}=36 MHz	350	µA
$I_{DD(BSPI)}$	BSPI supply current [1]		1.1	mA
$I_{DD(UART)}$	UART supply current [1]		850	µA
$I_{DD(I2C)}$	I2C supply current [1]		430	µA
$I_{DD(ADC)}$	ADC supply current when converting [2]		5	mA
$I_{DD(EIC)}$	EIC supply current		2.88	mA
$I_{DD(CAN)}$	CAN supply current [1]		2.95	mA
$I_{DD(GPIO)}$	GPIO supply current		150	µA
$I_{DD(TB)}$	TB supply current		250	µA
$I_{DD(PWM)}$	PWM supply current		240	µA
$I_{DD(RTC)}$	RTC supply current		370	µA
$I_{DD(DMA)}$	DMA supply current		2.5	mA
$I_{DD(ARB)}$	Native arbiter supply current		180	µA
$I_{DD(AHB)}$	AHB arbiter supply current		570	µA
$I_{DD(WUT)}$	WUT supply current		300	µA
$I_{DD(WIU)}$	WIU supply current		460	µA

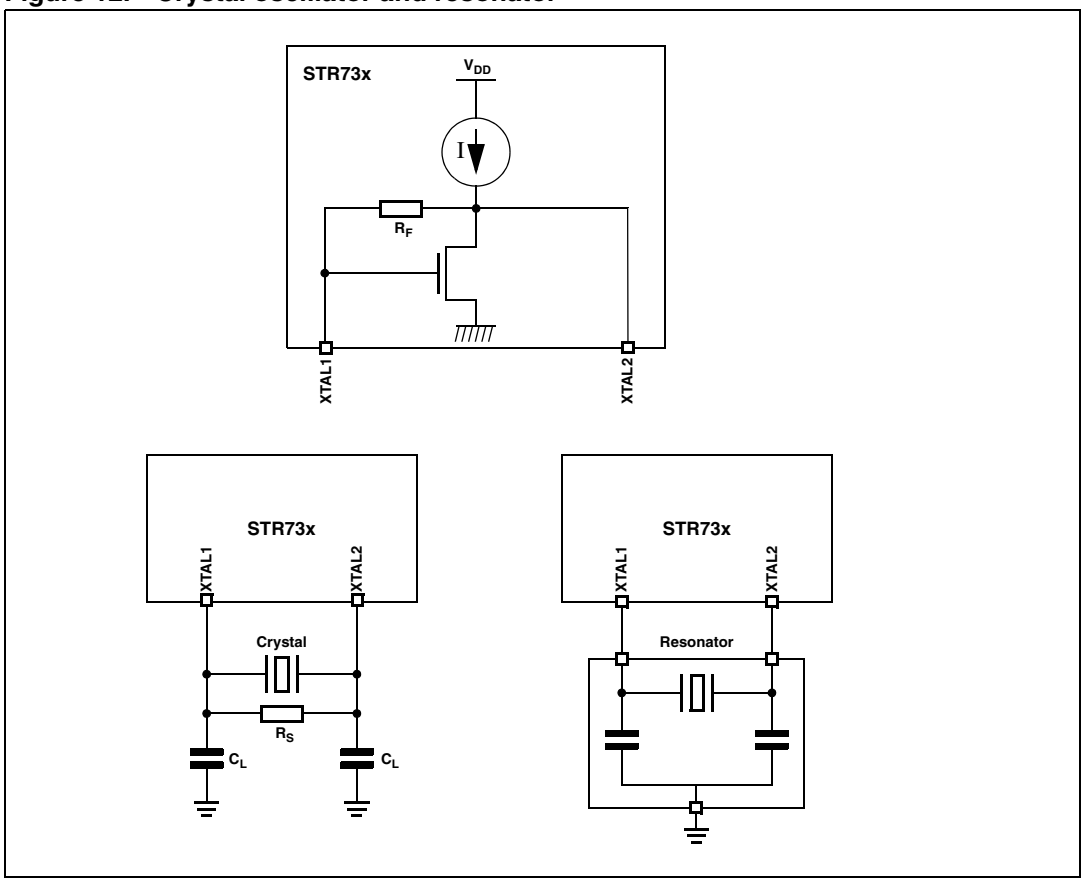
1. Data based on a differential I_{DD} measurement between the on-chip peripheral when kept under reset, not clocked and the on-chip peripheral when clocked and not kept under reset. This measurement does not include the pad toggling consumption.
2. Data based on a differential I_{DD} measurement between reset configuration and continuous A/D conversions.

4.3.2 Clock and timing characteristics

Crystal / ceramic resonator oscillator

The STR73xF can operate with a crystal oscillator or resonator clock source. *Figure 12* describes a simple model of the internal oscillator driver as well as example of connection for an oscillator or a resonator.

Figure 12. Crystal oscillator and resonator



Note: 1 XTAL2 must not be used to directly drive external circuits.

2 For test or boot purpose, XTAL2 can be used as an high impedance input pin to provide an external clock to the device. XTAL1 should be grounded, and XTAL2 connected to a wave signal generator providing a 0 to VDD signal. Directly driving XTAL2 may results in deteriorated jitter and duty cycle.

Main oscillator characteristics

V_{DD} = 5 V ± 10%, T_A = -40° C to T_{Amax}, unless otherwise specified.

Table 14. Main oscillator characteristics

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
f_{OSC}	Oscillator frequency		4		8	MHz
g_m	Oscillator transconductance		1.5		4.2	mA/V
V_{OSC} 1)	Oscillation amplitude	f_{OSC} = 4 MHz, T_A= 25° C	-	2.4	-	V
		f_{OSC} = 8 MHz, T_A= 25° C		1.-		
V_{AV} 1)	Oscillator operating point	Sine wave middle, T_A= 25° C	-	0.77	-	v
t_{STUP} 1)	Oscillator start-up time	External crystal, V_{DD} = 5.5 V, f_{OSC} = 4 MHz, T_A=-40° C	-	-	12	ms
		External crystal, V_{DD} = 5.0 V, f_{OSC} = 4 MHz, T_A=25° C	-	5.5	-	ms
		External crystal, V_{DD} = 5.5 V, f_{OSC} = 6 MHz, T_A=-40° C	-	-	8	ms
		External crystal, V_{DD} = 5.0 V, f_{OSC} = 6 MHz, T_A=25° C	-	3.3	-	ms
		External crystal, V_{DD} = 5.5 V, f_{OSC} = 8 MHz, T_A=-40° C	-	-	7	ms
		External crystal, V_{DD} = 5.0 V, f_{OSC} = 8 MHz, T_A= 25° C	-	2.7	-	ms

Table 14. Main oscillator characteristics (continued)

Symbol	Parameter	Conditions		Value			Unit
				Min	Typ	Max	
R_F [1]	Feedback resistor	f_{OSC} = 4 MHz Cp[2] = 10 pF	C_1[3] = C_2 [4]= 10 pF	150	555	-	Ω
			$C_1 = C_2$ = 20 pF	490	1035	-	
			$C_1 = C_2$ = 30 pF	490	1030	-	
			$C_1 = C_2$ = 40 pF	380	850	-	
		f_{OSC} = 5 MHz Cp = 10 pF	$C_1 = C_2$ = 10 pF	160	470	-	
			$C_1 = C_2$ = 20 pF	415	800	-	
			$C_1 = C_2$ = 30 pF	340	735	-	
			$C_1 = C_2$ = 40 pF	260	580	-	
		f_{OSC} = 6 MHz Cp = 10 pF	$C_1 = C_2$ = 10 pF	160	415	-	
			$C_1 = C_2$ = 20 pF	325	640	-	
			$C_1 = C_2$ = 30 pF	250	550	-	
			$C_1 = C_2$ = 40 pF	180	420	-	
		f_{OSC} = 7 MHz Cp = 10 pF	$C_1 = C_2$ = 10 pF	160	375	-	
			$C_1 = C_2$ = 20 pF	260	525	-	
			$C_1 = C_2$ = 30 pF	185	420	-	
			$C_1 = C_2$ = 40 pF	135	315	-	
		f_{OSC} = 8 MHz Cp = 10 pF	$C_1 = C_2$ = 10 pF	155	340	-	
			$C_1 = C_2$ = 20 pF	210	435	-	
			$C_1 = C_2$ = 30 pF	145	335	-	
			$C_1 = C_2$ = 40 pF	100	245	-	

1. Min and max values are guaranteed by characterization, not tested in production.
2. C_P represents the total capacitance between XTAL1 and XTAL2, including the shunt capacitance of the external quartz crystal as well as the total board parasitic cross-capacitance between XTAL1 track and XTAL2 track.
3. C_1 represents the total capacitance between XTAL1 and ground, including the external capacitance tied to XTAL1 pin (C_L) as well as the total parasitic capacitance between XTAL1 track and ground (this includes application board track capacitance to ground and device pin capacitance).
4. C_2 represents the total capacitance between XTAL2 and ground, including the external capacitance tied to XTAL1 pin (C_L) as well as the total parasitic capacitance between XTAL2 track and ground (this includes application board track capacitance to ground and device pin capacitance).

4.3.4 EMC characteristics

Susceptibility tests are performed on a sample basis during product characterization.

Functional EMS (electromagnetic susceptibility)

Based on a simple running application on the product (toggling 2 LEDs through I/O ports), the product is stressed by two electromagnetic events until a failure occurs (indicated by the LEDs).

- **ESD**: Electrostatic discharge (positive and negative) is applied on all pins of the device until a functional disturbance occurs. This test conforms with the IEC 1000-4-2 standard.
- **FTB**: A burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test conforms with the IEC 1000-4-4 standard.

A device reset allows normal operations to be resumed. The test results are given in the table below based on the EMS levels and classes defined in application note AN1709.

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations:

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical data corruption (control registers...)

Prequalification trials:

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the RESET pin or the oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Table 19. EMS data

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD}=5 V, T_A=+25° C, f_{MCLK}=36 MHz conforms to IEC 1000-4-2	4A
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD}=5 V, T_A=+25° C, f_{MCLK}=36 MHz conforms to IEC 1000-4-4	4A

4.3.5 I/O port pin characteristics

General characteristics

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified.

Table 23. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Input low level voltage [1]	TTL ports			0.8	V
V_{IH}	Input high level voltage [1]		2.0			
$I_{INJ(PIN)}$	Injected current on any I/O pin				±10	mA
$\Sigma I_{INJ(PIN)}$ [2]	Total injected current (sum of all I/O and control pins)				±75	mA
I_{lkg}	Input leakage current [3]	$V_{SS} \leq V_{IN} \leq V_{DD}$			±1	µA
I_S	Static current consumption [4]	Floating input mode		200		µA
R_{PU}	Weak pull-up equivalent resistor[5]	$V_{IN}=V_{SS}$	55	120	220	kΩ
R_{PD}	Weak pull-down equivalent resistor[5]	$V_{IN}=V_{DD}$	55	120	220	kΩ
C_{IO}	I/O pin capacitance			5		pF

1. Data based on characterization results, not tested in production.
2. When the current limitation is not possible, the V_{IN} absolute maximum rating must be respected, otherwise refer to $I_{INJ(PIN)}$ specification. A positive injection is induced by $V_{IN}>V_{33}$ while a negative injection is induced by $V_{IN}<V_{SS}$. Refer to *Section 4.2 on page 22* for more details.
3. Leakage could be higher than max. if negative current is injected on adjacent pins.
4. Configuration not recommended, all unused pins must be kept at a fixed voltage: using the output mode of the I/O for example or an external pull-up or pull-down resistor. Data based on design simulation and/or technology characteristics, not tested in production.
6. The R_{PU} pull-up and R_{PD} pull-down equivalent resistor are based on a resistive transistor (corresponding I_{PU} and I_{PD} current characteristics described in *Figure 19*).

Figure 15. V_{OH} JTDO pin vs I_{OL} @ V_{DD} 5 V

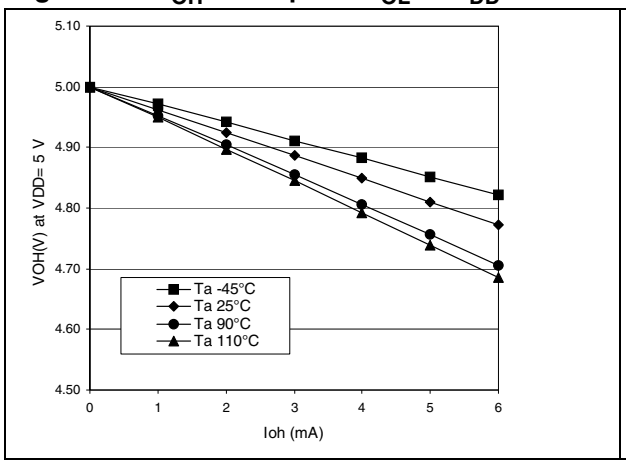


Figure 16. V_{OL} JTDO pin vs I_{OL} @ V_{DD} 5 V

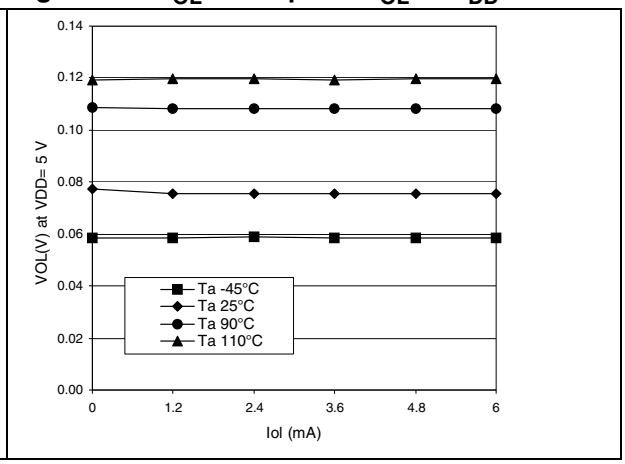


Figure 17. V_{OH} P6.0 pin vs I_{OL} @ V_{DD} 5 V

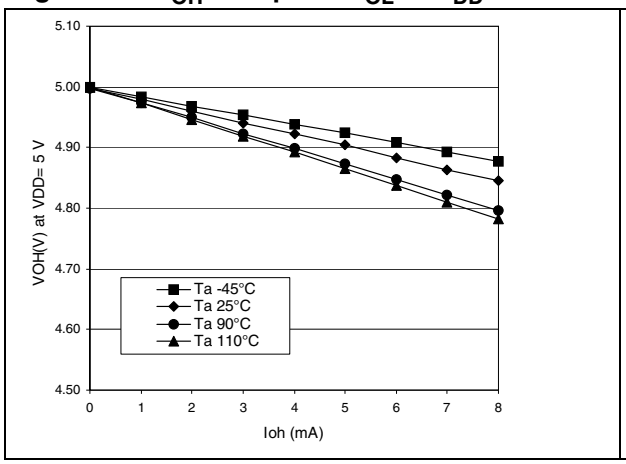


Figure 18. V_{OL} P6.0 pin vs I_{OL} @ V_{DD} 5 V

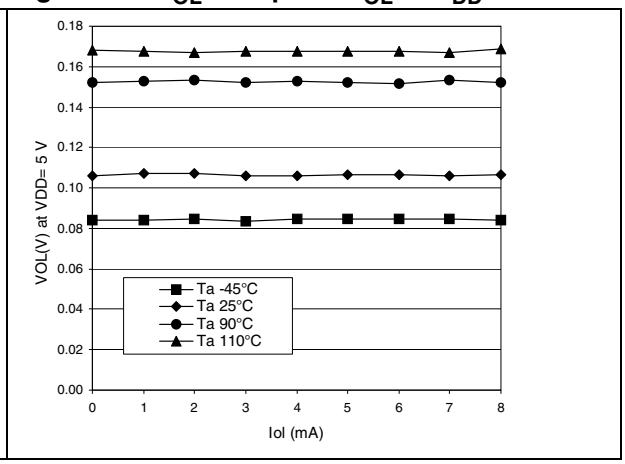


Figure 20. NRSTIN R_{PU} vs. V_{DD}

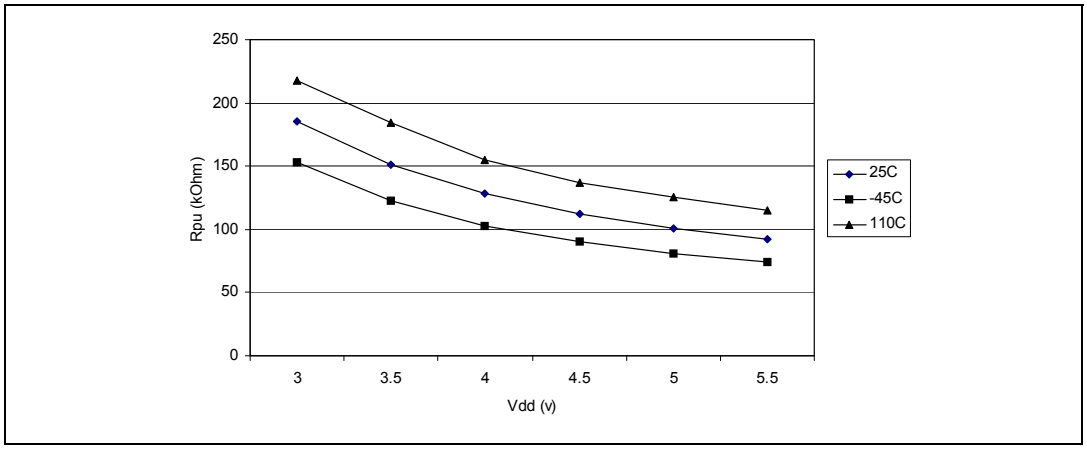
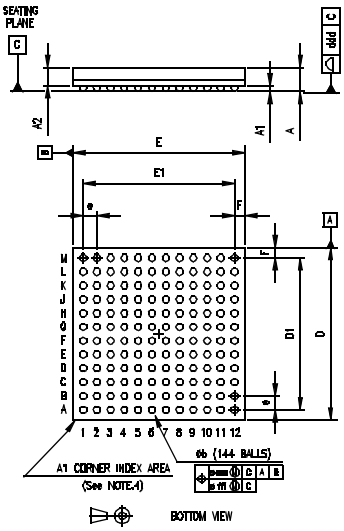


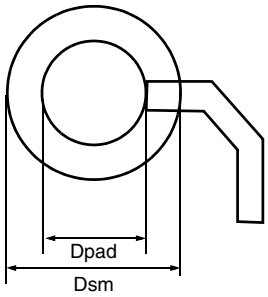
Figure 26. 144-ball low profile fine pitch ball grid array package



Dim.	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	1.21		1.70	0.0476		0.0669
A1	0.21			0.0083		
A2		1.085			0.0427	
b	0.35	0.40	0.45	0.0138	0.0157	0.0177
D	9.85	10.00	10.15	0.3878	0.3937	0.3996
D1		8.80			0.3465	
E	9.85	10.00	10.15	0.3878	0.3937	0.3996
E1		8.80			0.3465	
e		0.80			0.0315	
F		0.60			0.0236	
ddd			0.10			0.0039
eee			0.15			0.0059
fff			0.08			0.0031
	Number of Pins					
N	144					

[1] Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 27. Recommended PCB design rules (0.80/0.75mm pitch BGA)



Dpad	0.37 mm
Dsm	0.52 mm typ. (depends on solder mask registration tolerance
Solder paste	0.37 mm aperture diameter
– Non solder mask defined pads are recommended – 4 to 6 mils screen print	

5.2 Thermal characteristics

The average chip-junction temperature, T_J, in degrees Celsius, may be calculated using the following equation:

$$T_J = T_A + (P_D \times \Theta_{JA}) \quad (1)$$

Where:

- T_A is the ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D is the sum of P_{INT} and $P_{I/O}$ ($P_D = P_{INT} + P_{I/O}$),
- P_{INT} is the product of I_{DD} and V_{DD}, expressed in Watts. This is the chip internal power,
- $P_{I/O}$ represents the power dissipation on input and output pins; user determined.

Most of the time for the applications $P_{I/O} < P_{INT}$ and may be neglected. On the other hand, $P_{I/O}$ may be significant if the device is configured to drive continuously external modules and/or memories.

An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is given by:

$$P_D = K / (T_J + 273°C) \quad (2)$$

Therefore (solving equations 1 and 2):

$$K = P_D \times (T_A + 273°C) + \Theta_{JA} \times P_D^2 \quad (3)$$

Where:

- K is a constant for the particular part, which may be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J may be obtained by solving equations (1) and (2) iteratively for any value of T_A

Table 28. Thermal characteristics

Symbol	Description	Package	Value (typical)	Unit
Θ_{JA}	Thermal resistance junction-ambient	LFBGA144	50	°C/W
		TQFP144	40	
		TQFP100	40	

8 Revision history

Table 30. Document revision history

Date	Revision	Description of changes
19-Sep-2005	1	First release
02-Nov-2005	2	Removed Table 8 power consumption in LP modes Updated PLL frequency in *Section 1.1* and *Table 12*
08-Mar-2006	3	*Section 3.4: Preliminary power consumption data* updated *Section 3.5: DC electrical characteristics* updated *Section 7: Known limitations* added
04-Jun-2006	4	*Section 4: Electrical parameters* updated *Section 7: Known limitations* updated Added temperature range -40°C to 85°C in *Section 6: Order codes*
19-Jun-2006	5	Changed Flash data retention to 20 years at 85°C in *Table 18 on page 34*.
08-Sep-2006	6	Changed *Table 24: Output driving current on page 39* Added *Figure 14: VOL standard ports vs IOL @ VDD 5 V* thru *Figure 18: VOL P6.0 pin vs IOL @ VDD 5 V on page 40*. Added *Figure 20: NRSTIN RPU vs. VDD*
08-Jun-2008	7	Inch values rounded to 4 decimal digits in *Section 5.1: Package mechanical data* Modified BSPI speed in *Section 2.1: On-chip peripherals*