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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM7®
Core Size	32-Bit Single-Core
Speed	36MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	72
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/str736fv0t6

3 Block diagram

Figure 1. STR730F/STR735F block diagram

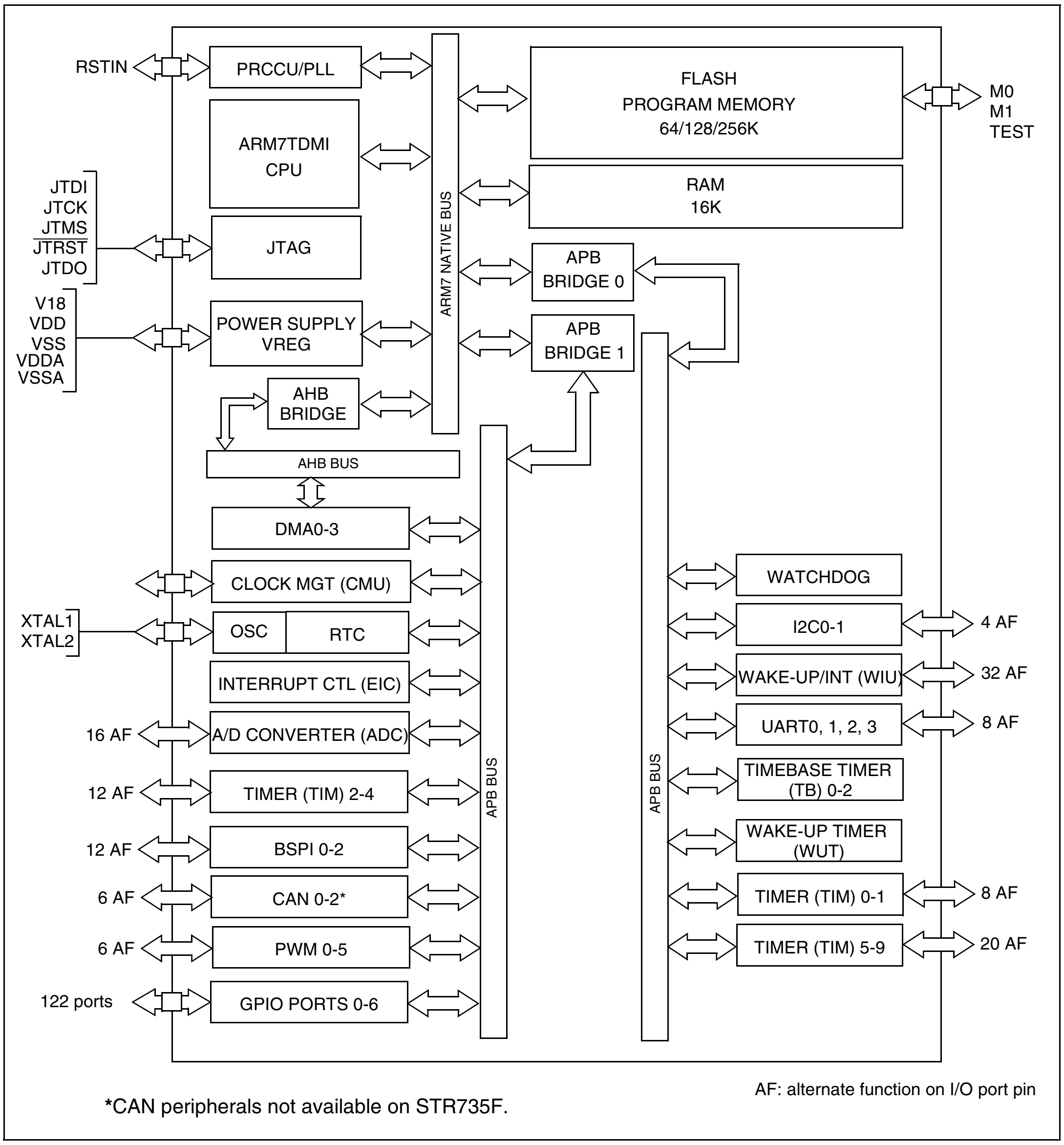
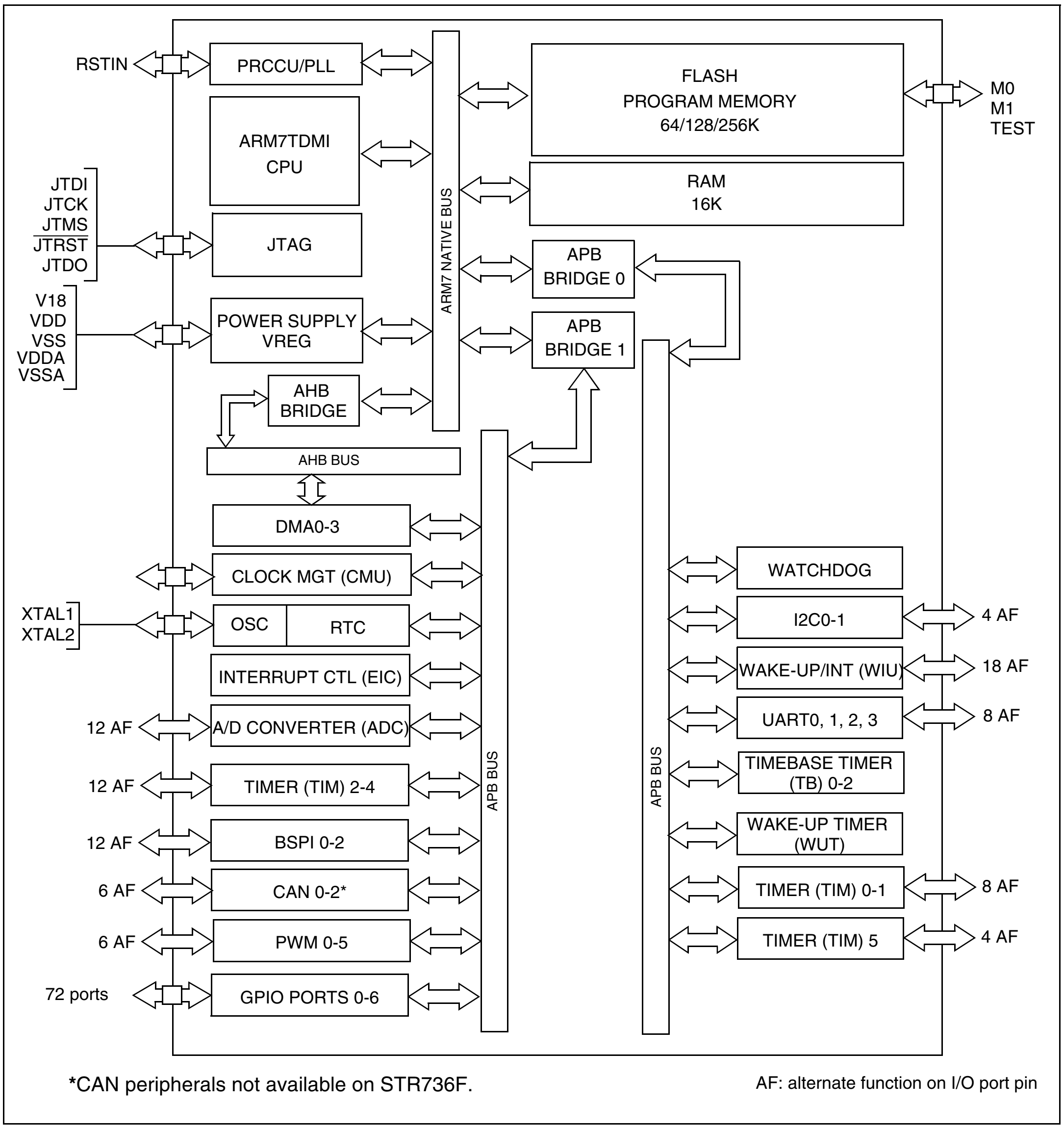


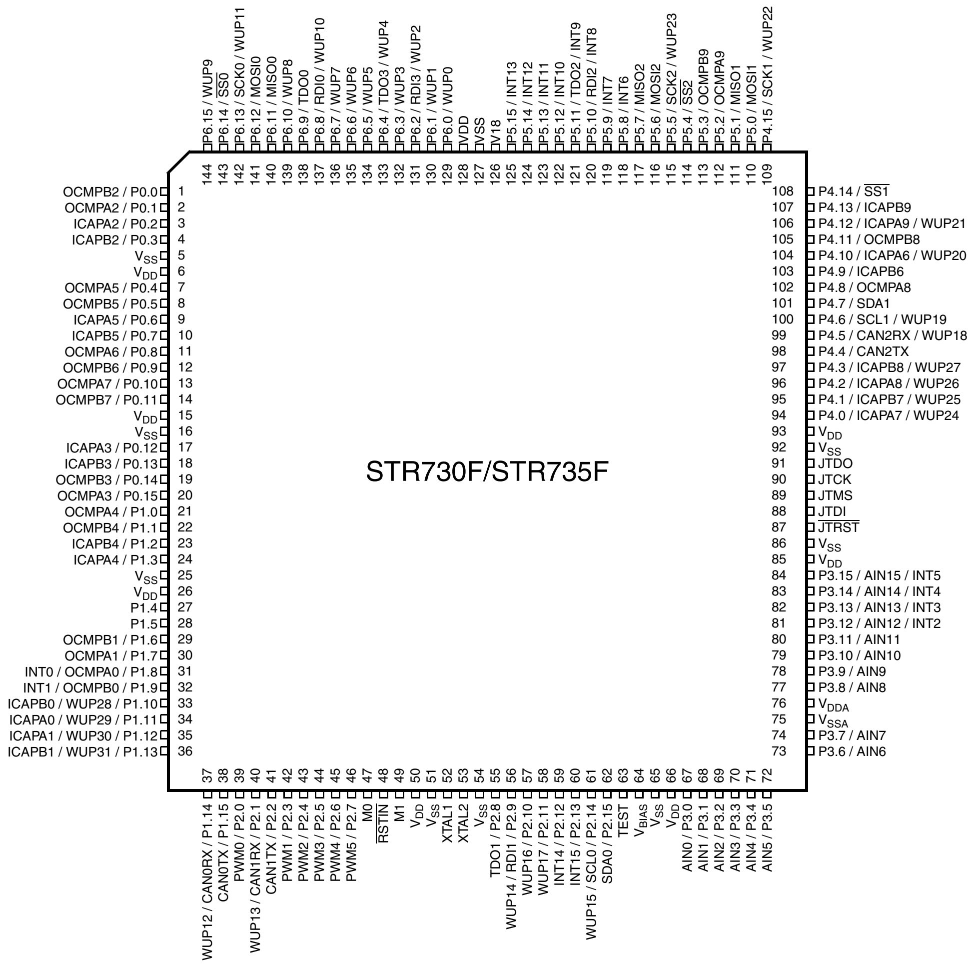
Figure 2. STR731F/STR736 block diagram



3.2 Pin description

3.2.1 STR730F/STR735F (TQFP144)

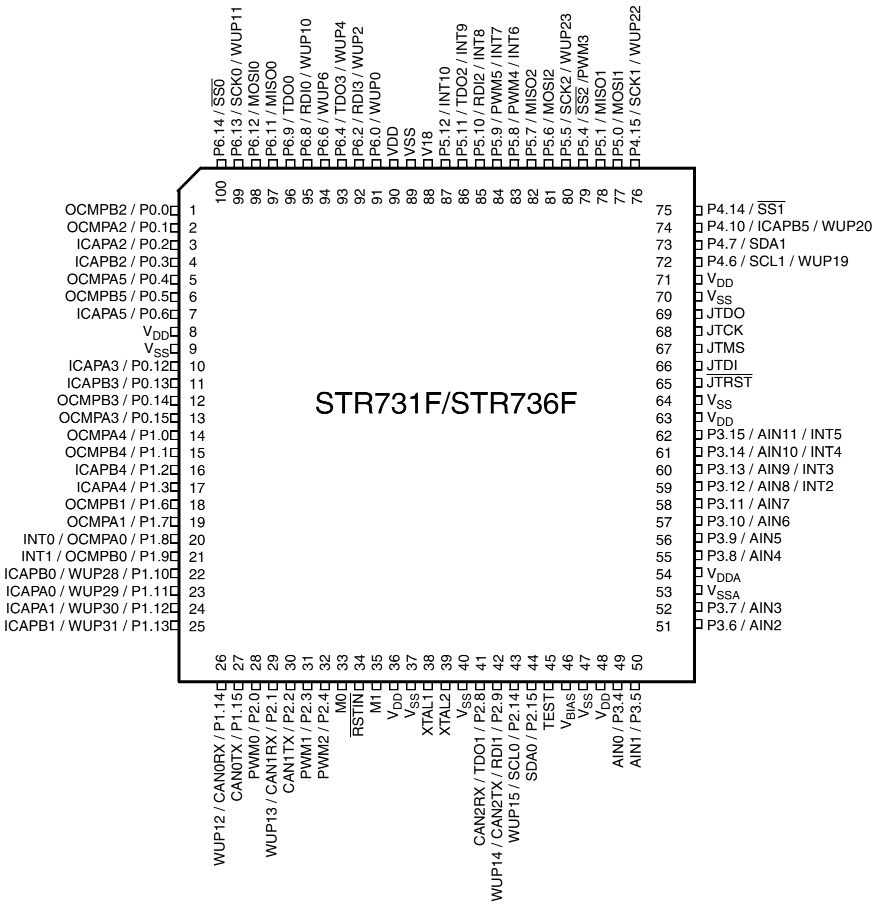
Figure 3. STR730F/STR735F pin configuration (top view)



Note: CAN alternate functions not available on STR735F.

3.2.3 STR731F/STR736F (TQFP100)

Figure 4. STR731F/STR736F pin configuration (top view)



Note: CAN alternate functions not available on STR736F.

Table 4. STR73xF pin description

Pin n°			Pin name	Type	Input			Output			Main function (after reset)	Alternate function	
TQFP144	LFBGA144	TQFP100			Input Level	pu/pd	interrupt	Capability	OD	PP			
50	J5	36	V_{DD}	S							Supply voltage (5 V)		
51	M6	37	V_{SS}	S							Ground		
52	M7	38	XTAL1	I							Oscillator amplifier circuit input and internal clock generator input.		
53	H5	39	XTAL2	O							Oscillator amplifier circuit output.		
54	L6	40	V_{SS}	S							Ground		
55	K6	41	P2.8/TDO1/CAN2RX	I/O	T_T			2mA	X	X	Port 2.8	UART1: transmit data output	CAN2: receive data input (TQFP100 only)
56	J6	42	P2.9/RDI1/CAN2TX	I/O	T_T		WUP14	2mA	X	X	Port 2.9	UART1: receive data input	CAN2: transmit data output (TQFP100 only)
57	H6		P2.10	I/O	T_T		WUP16	2mA	X	X	Port 2.10		
58	G6		P2.11	I/O	T_T		WUP17	2mA	X	X	Port 2.11		
59	L7		P2.12	I/O	T_T		INT14	2mA	X	X	Port 2.12		
60	K7		P2.13	I/O	T_T		INT15	2mA	X	X	Port 2.13		
61	J7	43	P2.14/SCL0	I/O	T_T		WUP15	2mA	X	X	Port 2.14	I2C0: serial clock	
62	H7	44	P2.15/SDA0	I/O	T_T			2mA	X	X	Port 2.15	I2C0: serial data	
63	M8	45	Test	I		pd					Reserved pin. Must be tied to ground		
64	L8	46	V_{BIAS}	S							Internal RC oscillator bias. A 1.3 MΩ external resistor has to be connected to this pin when a 32 kHZ RC oscillator frequency is used.		
65	M10	47	V_{SS}	S							Ground		
66	M11	48	V_{DD}	S							Supply voltage (5 V)		
67	K8		P3.0/AIN0	I/O	T_T			2mA	X	X	Port 3.0	ADC: analog input 0	
68	J8		P3.1/AIN1	I/O	T_T			2mA	X	X	Port 3.1	ADC: analog input 1	
69	M9		P3.2/AIN2	I/O	T_T			2mA	X	X	Port 3.2	ADC: analog input 2	
70	L9		P3.3/AIN3	I/O	T_T			2mA	X	X	Port 3.3	ADC: analog input 3	
71	K9	49	P3.4/AIN4	I/O	T_T			2mA	X	X	Port 3.4	ADC: analog input 4 (AIN0 in TQFP100)	
72	L10	50	P3.5/AIN5	I/O	T_T			2mA	X	X	Port 3.5	ADC: Analog input 5 (AIN1 in TQFP100)	

Table 4. STR73xF pin description

Pin n°			Pin name	Type	Input			Output			Main function (after reset)	Alternate function
TQFP144	LFBGA144	TQFP100			Input Level	pu/pd	interrupt	Capability	OD	PP		
73	M12	51	P3.6/AIN6	I/O	T_T			2mA	X	X	Port 3.6	ADC: analog input 6 (AIN2 in TQFP100)
74	L11	52	P3.7/AIN7	I/O	T_T			2mA	X	X	Port 3.7	ADC: analog input 7 (AIN3 in TQFP100)
75	K11	53	V_{SSA}	S							Reference ground for A/D converter	
76	K10	54	V_{DDA}	S							Reference voltage for A/D converter	
77	J12	55	P3.8/AIN8	I/O	T_T			2mA	X	X	Port 3.8	ADC: analog input 8 (AIN4 in TQFP100)
78	J11	56	P3.9/AIN9	I/O	T_T			2mA	X	X	Port 3.9	ADC: analog input 9 (AIN5 in TQFP100)
79	L12	57	P3.10/AIN10	I/O	T_T			2mA	X	X	Port 3.10	ADC: analog input 10 (AIN6 in TQFP100)
80	K12	58	P3.11/AIN11	I/O	T_T			2mA	X	X	Port 3.11	ADC: analog input 11 (AIN7 in TQFP100)
81	J10	59	P3.12/AIN12	I/O	T_T		INT2	2mA	X	X	Port 3.12	ADC: analog input 12 (AIN8 in TQFP100)
82	J9	60	P3.13/AIN13	I/O	T_T		INT3	2mA	X	X	Port 3.13	ADC: analog input 13 (AIN9 in TQFP100)
83	H12	61	P3.14/AIN14	I/O	T_T		INT4	2mA	X	X	Port 3.14	ADC: analog input 14 (AIN10 in TQFP100)
84	H11	62	P3.15/AIN15	I/O	T_T		INT5	2mA	X	X	Port 3.15	ADC: analog input 15 (AIN11 in TQFP100)
85	H10	63	V_{DD}	S							Supply voltage (5 V)	
86	H9	64	V_{SS}	S							Ground	
87	G12	65	JTRST	I	T_T	pu						JTAG reset Input
88	F12	66	JTDI	I	T_T	pu						JTAG data input
89	H8	67	JTMS	I	T_T	pu						JTAG mode selection Input
90	G11	68	JTCK	I	T_T	pd						JTAG clock Input
91	G10	69	JTDO	O				4mA				JTAG data output. **Note:** Reset state = HiZ
92	G9	70	V_{SS}	S								Ground
93	G8	71	V_{DD}	S								Supply voltage (5 V)
94	G7		P4.0/ICAPA7	I/O	T_T		WUP24	2mA	X	X	Port 4.0	TIM7: input capture A input
95	F11		P4.1/ICAPB7	I/O	T_T		WUP25	2mA	X	X	Port 4.1	TIM7: input capture B input
96	F10		P4.2/ICAPA8	I/O	T_T		WUP26	2mA	X	X	Port 4.2	TIM8: input capture A input

4 Electrical parameters

4.1 Parameter conditions

Unless otherwise specified, all voltages are referred to V_{SS}.

4.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A=25° C and T_A=T_{Amax} (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3Σ).

4.1.2 Typical values

Unless otherwise specified, typical data are based on T_A=25° C and V_{DD}=5 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2Σ).

4.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

4.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 6*.

4.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 7*.

Figure 6. Pin loading conditions

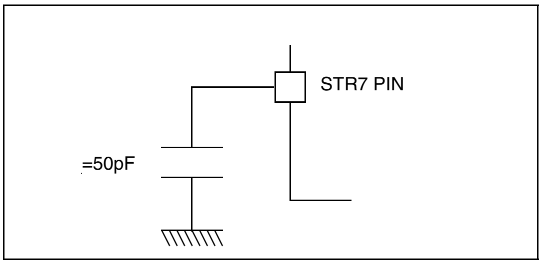
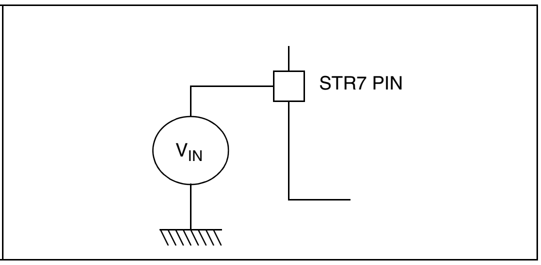


Figure 7. Pin input voltage



4.2 Absolute maximum ratings

Stresses above those listed as "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 5. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DD} - V_{SS}	External 5 V Supply voltage	-0.3	6.0	V
V_{SSA}	Reference ground for A/D converter	V_{SS}	V_{SS}	V
V_{DDA}- V_{SSA}	Reference voltage for A/D converter	-0.3	V_{DD}+0.3	V
V_{IN}	Input voltage on any pin	-0.3	V_{DD}+0.3	
$\lvert\Delta V_{DDx}\rvert$	Variations between different 5 V power pins	-	0.3	mV
$\lvert V_{SSX}$ - $V_{SS}\rvert$	Variations between all the different ground pins	-	0.3	
$V_{ESD(HBM)}$	Electrostatic discharge voltage (Human Body Model)	see *: Absolute maximum ratings (electrical sensitivity) on page 36*		
$V_{ESD(MM)}$	Electrostatic discharge voltage (Machine Model)			

Table 6. Current characteristics

Symbol	Ratings	Max.	Unit
I_{VDD}	Total current into V_{DD} power lines (source) [1]	100	mA
I_{VSS}	Total current out of V_{SS} ground lines (sink) [1]	100	
I_{IO}	Output current sunk by any I/O and control pin	10	
	Output current source by any I/O and control pin	10	
$I_{INJ(PIN)}$ [2) & 3)]	Injected current on any other pin [4) &5)]	±10	
$\Sigma I_{INJ(PIN)}$ [2)]	Total injected current (sum of all I/O and control pins) [4)]	±75	

1. All 5 V power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external 5 V supply
2. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by V_{IN}>V_{DD} while a negative injection is induced by V_{IN}<V_{SS}.
3. Negative injection disturbs the analog performance of the device. See note in *Section 4.3.6: 10-bit ADC characteristics on page 43*.
4. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values). These results are based on characterization with $\Sigma I_{INJ(PIN)}$ maximum current injection on four I/O port pins of the device.

5.) In 144-pin devices, only +10 mA on P0.3, P1.13, P3.6 and P4.13 pins (negative injection not allowed).

Table 7. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-55 to +150	°C
T_J	Maximum junction temperature (see *Section 5.2: Thermal characteristics on page 48*)		

4.3.1 Supply current characteristics

The current consumption is measured as described in *Figure 6* and *Figure 7*.

Total current consumption

The MCU is placed under the following conditions:

- All I/O pins in input mode with a static value at V_{DD} or V_{SS} (no load)
- All peripherals are disabled except if explicitly mentioned.

Subject to general operating conditions for V_{DD}, and T_A.

Table 10. Total current consumption

Symbol	Parameter	Conditions	Typ [1)]	Max [2)]	Unit
I_{DD}	RUN mode[3)]	Formula, f_{MCLK} in MHz, RAM execution	7 + 1.9 f_{MCLK}		mA
		f_{MCLK} = 36 MHz, RAM execution	76		mA
		f_{MCLK} = 36 MHz, Flash execution	86		mA
	WFI mode	f_{OSC} = 4 MHz, f_{MCLK}= f_{OSC}/16 = 250 kHz Main voltage regulator ON, LP voltage regulator = 2 mA, RTC and WDG on, other modules off.	6.7	8	mA
	LPWFI mode	f_{RC} = high frequency (CMU_RCCTL= 0x8), f_{MCLK}= f_{RC} /16, LP voltage regulator = 2 mA, other modules off.	220	350	µA
	STOP mode	f_{OSC} = 4 MHz, RC oscillator on f_{RC} = high frequency (CMU_RCCTL= 0x0) LP voltage regulator = 6 mA, RTC and WUT ON, other modules off. Internal wake-up possible.	500	700	µA
		f_{RC} = high frequency (CMU_RCCTL= 0xF), LP voltage regulator = 2mA. WUT ON, other modules off. Internal wake-up possible.	150	220	
		LP voltage regulator = 2 mA, WIU on, Other modules off, external wake-up.	50	140	
	HALT mode	LP voltage regulator = 2 mA.	50	140	µA

1. Typical data are based on T_A=25° C, V_{DD}=5 V
2. Data based on characterization results, tested in production at V_{DD} max. and T_A = 25° C.
3. I/O in static configuration (not toggling). RUN mode is almost **independent of temperature**. On the contrary RUN mode current is **highly dependent on the application**. The I_{DDRUN} value can be significantly reduced by the application in the following ways: switch-off unused peripherals (default), reduce peripheral frequency through internal prescaler, fetch the most frequently-used functions from RAM and use low power mode when possible.

RC/backup oscillator characteristics

V_{DD} = 5V ± 10%, T_A = -40°C to T_{Amax}, unless otherwise specified.

Table 15. RC oscillator characteristics

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
f_{RC}	RC frequency	High frequency mode [1]		2.35		MHz
		Low frequency mode[1]		29		kHz
f_{RCHF}	RC high frequency	CMU_RCCTL = 0x0	3			MHz
		CMU_RCCTL = 0xF			2.3	MHz
f_{RCLF}	RC low frequency	CMU_RCCTL = 0x0	35			kHz
		CMU_RCCTL = 0xF			30	kHz
f_{RCHFS}[2]	RC high frequency stability	Fixed CMU_RCCTL			10	%
f_{RCLFS}[2]	RC low frequency stability	Fixed CMU_RCCTL			23	%
t_{RCSTUP}	RC start-up time	Stable V_{DD}, f_{RC} = 2.35 MHz, T_A = 25°C		2.35		µs

1) CMU_RCCTL = 0x8

2) RC frequency shift versus average value (%)

PLL electrical characteristics

V_{DD} = 5 V ± 10%, T_A = -40° C to T_{Amax}, unless otherwise specified

Table 16. PLL characteristics

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
f_{PLLIN}(1)	PLL reference clock	FREF_RANGE = '0' FREF_RANGE = '1'	1.5 3.0		3.0 5.0	MHz
f_{PLLOUT}	PLL output clock	MX = "00" MX = "01" MX = "10" MX = "11"	20 x f_{PLLIN} 12 x f_{PLLIN} 28 x f_{PLLIN} 16 x f_{PLLIN}			MHz
f_{MCLK}	System clock	DX = 1..7	f_{PLLOUT}/DX		36	MHz
f_{FREE} (2)	PLL free running frequency	FREF_RANGE = '0', MX0 = '1' FREF_RANGE = '0', MX0 = '0' FREF_RANGE = '1', MX0 = '1' FREF_RANGE = '1', MX0 = '0'		120 240 240 480		kHz
t_{LOCK}(3)	PLL lock time	Stable oscillator (f_{PLLIN} = 4 MHz), stable V_{DD}		100	300	µs
Δt_{PKJIT}	PLL jitter (pk to pk)	f_{PLLIN} = 4 MHz (pulse generator)			1.5	ns

1. f_{PLLIN} is obtained from f_{OSC} directly or through an optional divider by 2.
2. Typical data are based on T_A=25°C, V_{DD}=5V
3. Max value is guaranteed by characterization, not tested in production.

Table 17. Low-power mode wake-up timing

Symbol	Parameter	Conditions	Typ	Unit
t_{WUHALT}	Wake-up from HALT mode		200	µs
t_{WUSTOP}	Wake-up from STOP mode	RC high frequency in STOP mode	180	µs
		RC low frequency in STOP mode	234	µs
$t_{WULPWFI}$ 1)	Wake-up from LPWFI mode	Main voltage regulator on RC oscillator off f_{OSC} = 4 MHz, f_{MCLK}= f_{OSC}/16 RAM or FLASH execution	27	µs
		Main voltage regulator on RC oscillator = high frequency Flash execution	46	µs
		Main voltage regulator on RC oscillator = low frequency Flash execution	3.6	ms

1. Flash memory programmed to enter Power Down mode during LPWFI.

4.3.5 I/O port pin characteristics

General characteristics

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified.

Table 23. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Input low level voltage [1]	TTL ports			0.8	V
V_{IH}	Input high level voltage [1]		2.0			
$I_{INJ(PIN)}$	Injected current on any I/O pin				±10	mA
$\Sigma I_{INJ(PIN)}$ [2]	Total injected current (sum of all I/O and control pins)				±75	mA
I_{lkg}	Input leakage current [3]	$V_{SS} \leq V_{IN} \leq V_{DD}$			±1	µA
I_S	Static current consumption [4]	Floating input mode		200		µA
R_{PU}	Weak pull-up equivalent resistor[5]	$V_{IN}=V_{SS}$	55	120	220	kΩ
R_{PD}	Weak pull-down equivalent resistor[5]	$V_{IN}=V_{DD}$	55	120	220	kΩ
C_{IO}	I/O pin capacitance			5		pF

1. Data based on characterization results, not tested in production.
2. When the current limitation is not possible, the V_{IN} absolute maximum rating must be respected, otherwise refer to $I_{INJ(PIN)}$ specification. A positive injection is induced by $V_{IN}>V_{33}$ while a negative injection is induced by $V_{IN}<V_{SS}$. Refer to *Section 4.2 on page 22* for more details.
3. Leakage could be higher than max. if negative current is injected on adjacent pins.
4. Configuration not recommended, all unused pins must be kept at a fixed voltage: using the output mode of the I/O for example or an external pull-up or pull-down resistor. Data based on design simulation and/or technology characteristics, not tested in production.
6. The R_{PU} pull-up and R_{PD} pull-down equivalent resistor are based on a resistive transistor (corresponding I_{PU} and I_{PD} current characteristics described in *Figure 19*).

Figure 15. V_{OH} JTDO pin vs I_{OL} @ V_{DD} 5 V

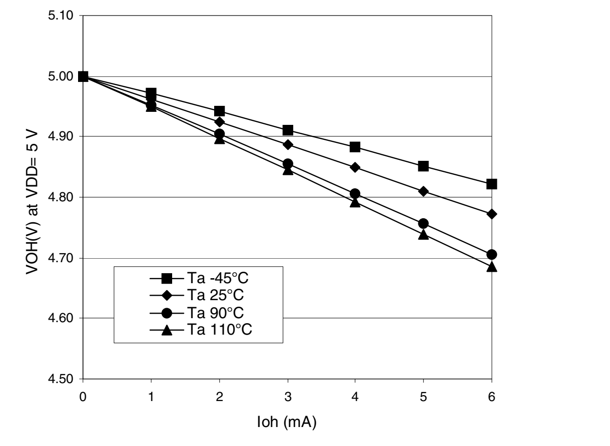


Figure 16. V_{OL} JTDO pin vs I_{OL} @ V_{DD} 5 V

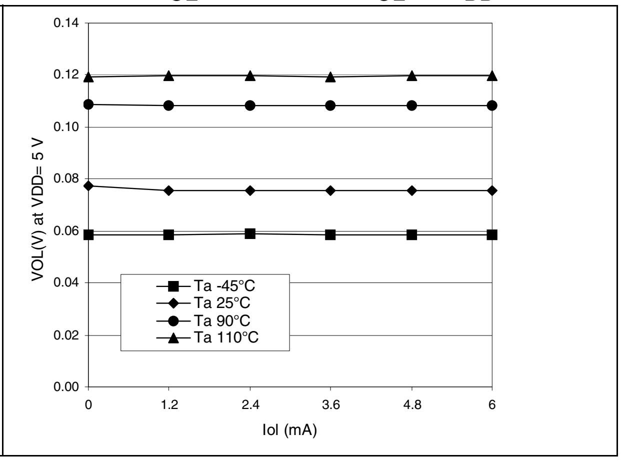


Figure 17. V_{OH} P6.0 pin vs I_{OL} @ V_{DD} 5 V

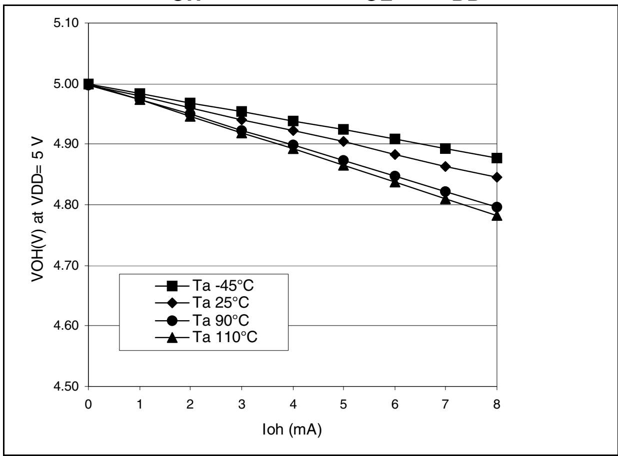
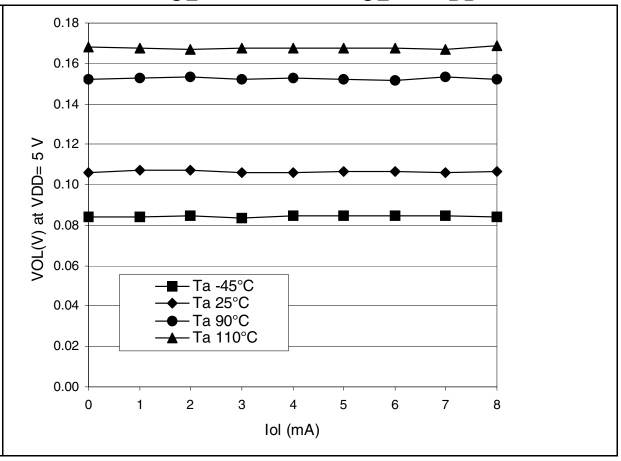


Figure 18. V_{OL} P6.0 pin vs I_{OL} @ V_{DD} 5 V



NRSTIN pin

The NRSTIN pin input driver is CMOS. A permanent pull-up is present which is the same as R_{PU} (see *: General characteristics on page 38*)

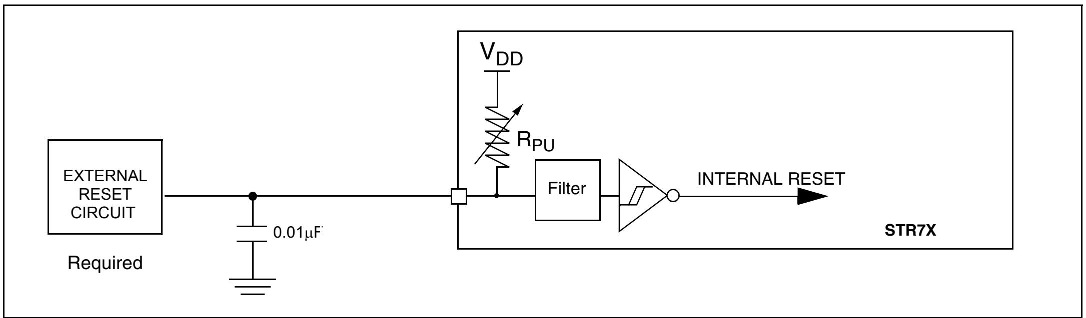
Subject to general operating conditions for V_{DD} and T_A unless otherwise specified.

Table 25. Reset pin characteristics

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
$V_{IL(NRSTIN)}$	NRSTIN Input low level voltage [1]				0.3 V_{DD}	V
$V_{IH(NRSTIN)}$	NRSTIN Input high level voltage [1]		0.7 V_{DD}			
$V_{hys(NRSTIN)}$	NRSTIN Schmitt trigger voltage hysteresis [2]			800		mV
$V_{F(RSTINn)}$	NRSTIN Input filtered pulse[3]				500	ns
$V_{NF(RSTINn)}$	NRSTIN Input not filtered pulse[3]		2			µs
$V_{RP(RSTINn)}$	NRSTIN removal after Power-up[3]		100			µs

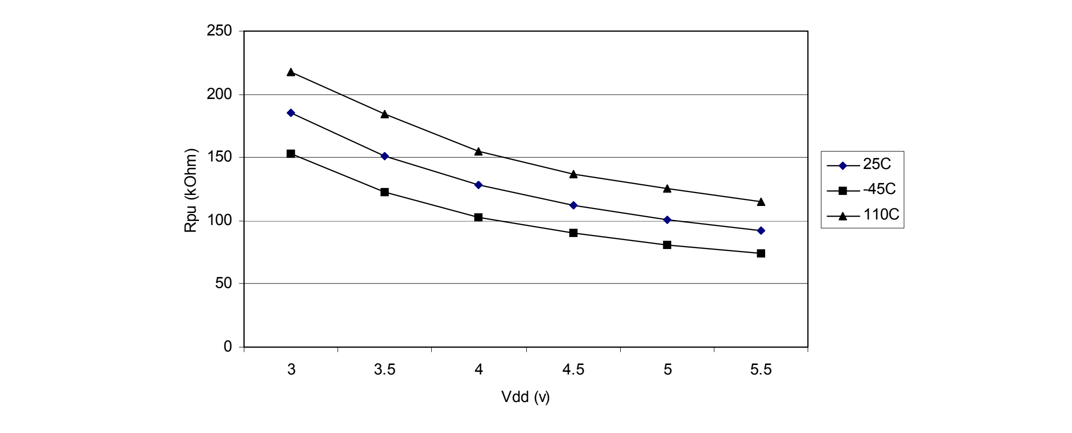
1. Data based on characterization results, not tested in production.
2. Hysteresis voltage between Schmitt trigger switching levels.
3. Data guaranteed by design, not tested in production.

Figure 19. Recommended NRSTIN pin protection[1]



1. The R_{PU} pull-up equivalent resistor is based on a resistive transistor.
2. The reset network protects the device against parasitic resets.
3. The user must ensure that the level on the NRSTIN pin can go below the $V_{IL(NRSTIN)}$ max. level specified in *Table 25*. Otherwise the reset will not be taken into account internally.

Figure 20. NRSTIN R_{PU} vs. V_{DD}



4.3.6 10-bit ADC characteristics

Subject to general operating conditions for V_{DDA}, f_{MCLK}, and T_A unless otherwise specified.

Table 26. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
f_{ADC}			0.4		10	MHz
V_{AIN}	Conversion voltage range [2]		V_{SSA}		V_{DDA}	V
I_{lkg}	Negative input leakage current on analog pins	$V_{IN}<V_{SS}$, $\lvert I_{IN}\rvert < 400$ µA on adjacent analog pin		5	6	µA
C_{ADC}	Internal sample and hold capacitor				3.5	pF
t_{CAL} [2]	Calibration time	f_{ADC} = 10 MHz	580.2			µs
			5802			$1/f_{ADC}$
t_S [3]	Sampling time	f_{ADC} = 10 MHz	1		14	µs
t_{CONV}	Total conversion time (including sampling time)	f_{ADC} = 10 MHz	3			µs
			30 (10 for sampling +20 for successive approximation)			$1/f_{ADC}$
I_{ADC}	Running mode	Normal mode			5	mA
	Power-down mode				1	µA

1. Unless otherwise specified, typical data are based on T_A=25°C and V_{DDA}-V_{SS}=5.0V. They are given only as design guidelines and are not tested.
2. Calibration is recommended once after each power-up.
3. During the sample time the input capacitance C_{AIN} (6.8 max) can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_S. After the end of the sample time t_S, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_S depend on programming.

Table 27. ADC accuracy with f_{MCLK} = 20 MHz, f_{ADC}=10 MHz, R_{AIN} < 10 kΩ RAIN, V_{DDA}=5 V. This assumes that the ADC is calibrated[2)]

Symbol	Parameter	Conditions	Typ	Max	Unit
$\lvert E_T \rvert$	Total unadjusted error [1)]		1.0	2.0	LSB
$\lvert E_O \rvert$	Offset error [1)]		0.15	1.0	
$\lvert E_G \rvert$	Gain error [1)]		0.97	1.1	
$\lvert E_D \rvert$	Differential linearity error[1)]		0.7	1.0	
$\lvert E_L \rvert$	Integral linearity error [1)]		0.76	1.5	

1. ADC accuracy vs. negative injection current: Injecting negative current on any of the standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current. The effect of negative injection current on robust pins is specified in *Section 4.3.5*.
   Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 4.3.5* does not affect the ADC accuracy.
2. Calibration is needed once after each power-up.

Figure 21. ADC accuracy characteristics

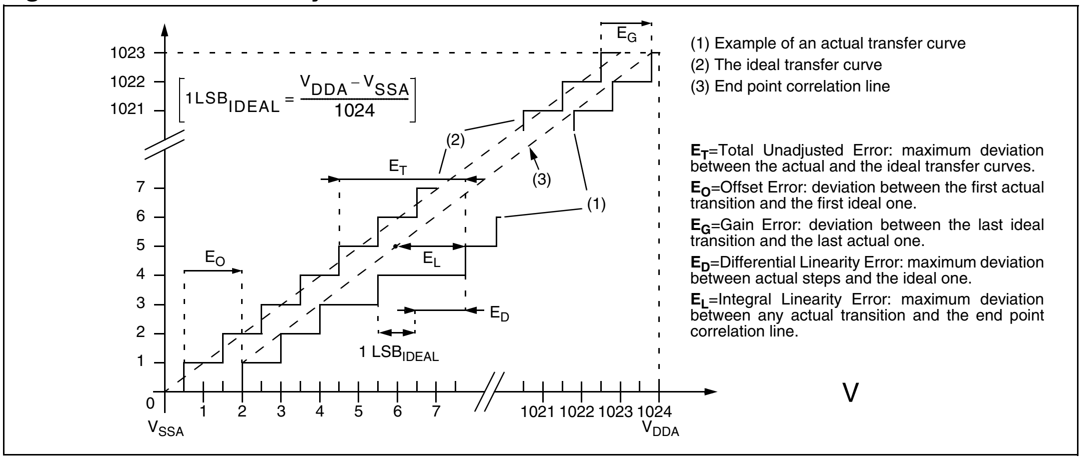
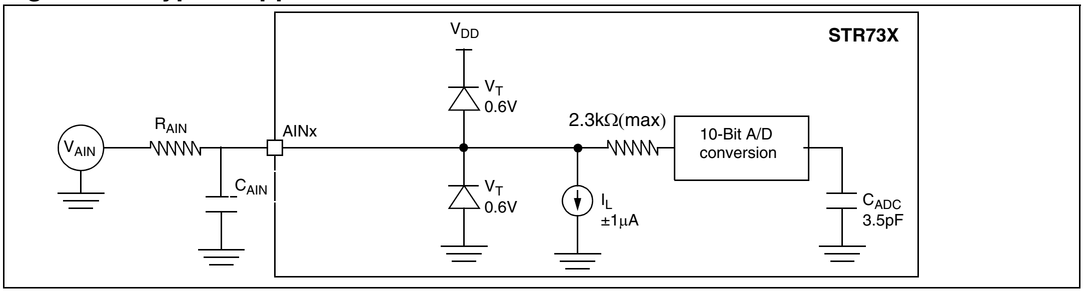


Figure 22. Typical application with ADC



Analog power supply and reference pins

The V_{DDA} and V_{SSA} pins are the analog power supply of the A/D converter cell. They act as the high and low reference voltages for the conversion.

Separation of the digital and analog power pins allow board designers to improve A/D performance. Conversion accuracy can be impacted by voltage drops and noise in the event of heavily loaded or badly decoupled power supply lines (see*: General PCB design guidelines*).

General PCB design guidelines

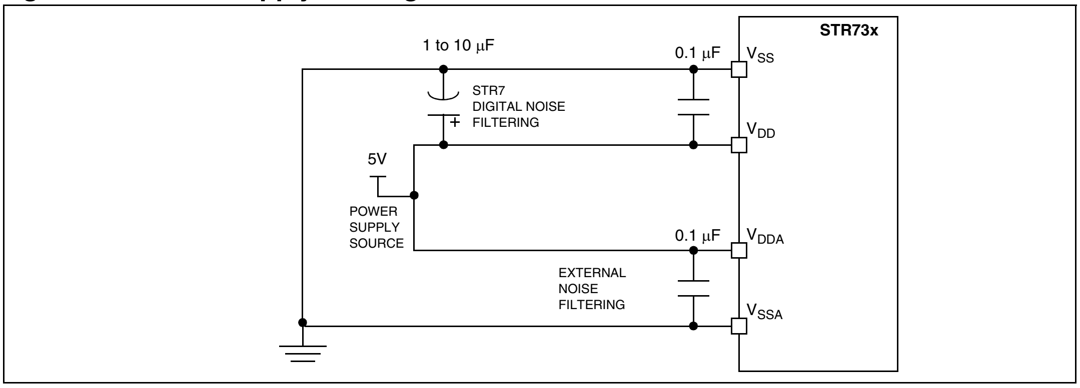
To obtain best results, some general design and layout rules should be followed when designing the application PCB to shield the noise-sensitive, analog physical interface from noise-generating CMOS logic signals.

- Use separate digital and analog planes. The analog ground plane should be connected to the digital ground plane via a single point on the PCB.
- Filter power to the analog power planes. It is recommended to connect capacitors, with good high frequency characteristics, between the power and ground lines, placing 0.1 µF and optionally, if needed 10 pF capacitors as close as possible to the STR7 power supply pins and a 1 to 10 µF capacitor close to the power source (see *Figure 23*).
- The analog and digital power supplies should be connected in a star network. Do not use a resistor, as V_{DDA} is used as a reference voltage by the A/D converter and any resistance would cause a voltage drop and a loss of accuracy.
- Properly place components and route the signal traces on the PCB to shield the analog inputs. Analog signals paths should run over the analog ground plane and be as short as possible. Isolate analog signals from digital signals that may switch while the analog inputs are being sampled by the A/D converter. Do not toggle digital outputs near the A/D input being converted.

Software filtering of spurious conversion results

For EMC performance reasons, it is recommended to filter A/D conversion outliers using software filtering techniques.

Figure 23. Power supply filtering



5.2 Thermal characteristics

The average chip-junction temperature, T_J, in degrees Celsius, may be calculated using the following equation:

$$T_J = T_A + (P_D \times \Theta_{JA}) \quad (1)$$

Where:

- T_A is the ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D is the sum of P_{INT} and $P_{I/O}$ ($P_D = P_{INT} + P_{I/O}$),
- P_{INT} is the product of I_{DD} and V_{DD}, expressed in Watts. This is the chip internal power,
- $P_{I/O}$ represents the power dissipation on input and output pins; user determined.

Most of the time for the applications $P_{I/O} < P_{INT}$ and may be neglected. On the other hand, $P_{I/O}$ may be significant if the device is configured to drive continuously external modules and/or memories.

An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is given by:

$$P_D = K / (T_J + 273°C) \quad (2)$$

Therefore (solving equations 1 and 2):

$$K = P_D \times (T_A + 273°C) + \Theta_{JA} \times P_D^2 \quad (3)$$

Where:

- K is a constant for the particular part, which may be determined from equation (3) by measuring P_D (at equilibrium) for a known $T_{A.}$ Using this value of K, the values of P_D and T_J may be obtained by solving equations (1) and (2) iteratively for any value of T_A

Table 28. Thermal characteristics

Symbol	Description	Package	Value (typical)	Unit
Θ_{JA}	Thermal resistance junction-ambient	LFBGA144	50	°C/W
		TQFP144	40	
		TQFP100	40	