Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM7®
Core Size	32-Bit Single-Core
Speed	36MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	72
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/str736fv2t7

2 Overview

Table 2. Product overview

Features	STR730FZx		STR735FZx		STR731FVx			STR736FVx		
Flash memory - bytes	128K	256K	128K	256K	64K	128K	256K	64K	128K	256K
RAM - bytes	16 K				16 K					
Peripheral functions	10 TIM timers, 112 I/Os, 32 wake-up lines, 16 ADC				6 TIM timers, 72 I/Os, 18 wake-up lines, 12 ADC channels					
CAN peripherals	3		0		3			0		
Operating voltage	4.5 to 5.5 V									
Operating temperature	-40 to +85°C/-40 to +105° C									
Packages	**T**=TQFP144 20 x 20 **H**=LFBGA144 10 x10				**T**=TQFP100 14x14					

Package choice: reduced pin-count TQFP100 or feature-rich 144-pin TQFP or LFBGA

The STR73xF family is available in 3 packages. The TQFP144 and LFBGA144 versions have the full set of all features. The 100-pin version has fewer timers, I/Os and ADC channels. Refer to the Device Summary on Page 1 for a comparison of the I/Os available on each package.

The family includes versions with and without CAN.

High speed Flash memory

The Flash program memory is organized in 32-bit wide memory cells which can be used for storing both code and data constants. It is accessed by CPU with zero wait states @ 36 MHz.

The STR7 embedded Flash memory can be programmed using in-circuit programming or in-application programming.

The Flash memory endurance is 10K write/erase cycles and the data retention is 20 years @ 85° C.

IAP (in-application programming): IAP is the ability to re-program the Flash memory of a microcontroller while the user program is running.

ICP (in-circuit programming): ICP is the ability to program the Flash memory of a microcontroller using JTAG protocol while the device is mounted on the user application board.

The Flash memory can be protected against different types of unwanted access (read/write/erase). There are two types of protection:

- Sector write protection
- Flash debug protection (locks JTAG access)

Flexible power management

To minimize power consumption, you can program the STR73xF to switch to SLOW, WFI LPWFI, STOP or HALT modes depending on the current system activity in the application.

Flexible clock control

Two clock sources are used to drive the microcontroller, a main clock driven by an external crystal or ceramic resonator and an internal backup RC oscillator that operates at 2 MHz or 32 kHz. The embedded PLL can be configured to generate an internal system clock of up to 36 MHz. The PLL output frequency can be programmed using a wide selection of multipliers and dividers.

Voltage regulators

The STR73xF requires an external 4.5 to 5.5 V power supply. There are two internal Voltage Regulators for generating the 1.8 V power supply needed by the core and peripherals. The main VR is switched off and the Low Power VR switched on when the application puts the STR73xF in Low Power Wait for Interrupt (LPWFI) mode.

Low voltage detectors

The voltage regulator and Flash modules each have an embedded LVD that monitors the internal 1.8 V supply. If the voltage drops below a certain threshold, the LVD will reset the STR73xF.

Note: An external power-on reset must be provided ensure the microcontroller starts-up correctly.

2.1 On-chip peripherals

CAN interfaces

The three CAN modules are compliant with the CAN specification V2.0 part B (active). The bit rate can be programmed up to 1 MBaud. These are not available in the STR735 and STR736.

DMA

4 DMA controllers, each with 4 data streams manage memory to memory, peripheral to peripheral, peripheral to memory and memory to peripheral transfers. The DMA requests are connected to TIM timers, BSPI0, BSPI1, BSPI2 and ADC. One of the streams can be configured to be triggered by a software request, independently from any peripheral activity.

16-bit timers (TIM)

Each of the ten timers (six in 100-pin devices) have a 16-bit free-running counter with 7-bit prescaler, up to two input capture/output compare functions, a pulse counter function, and a PWM channel with selectable frequency. This provides a total of 16 independent PWMs (12 in 100-pin devices) when added with the PWM modules (see next paragraph).

PWM modules (PWM)

The six 16-bit PWM modules have independently programmable periods and duty-cycles, with 5+3 bit prescaler factor.

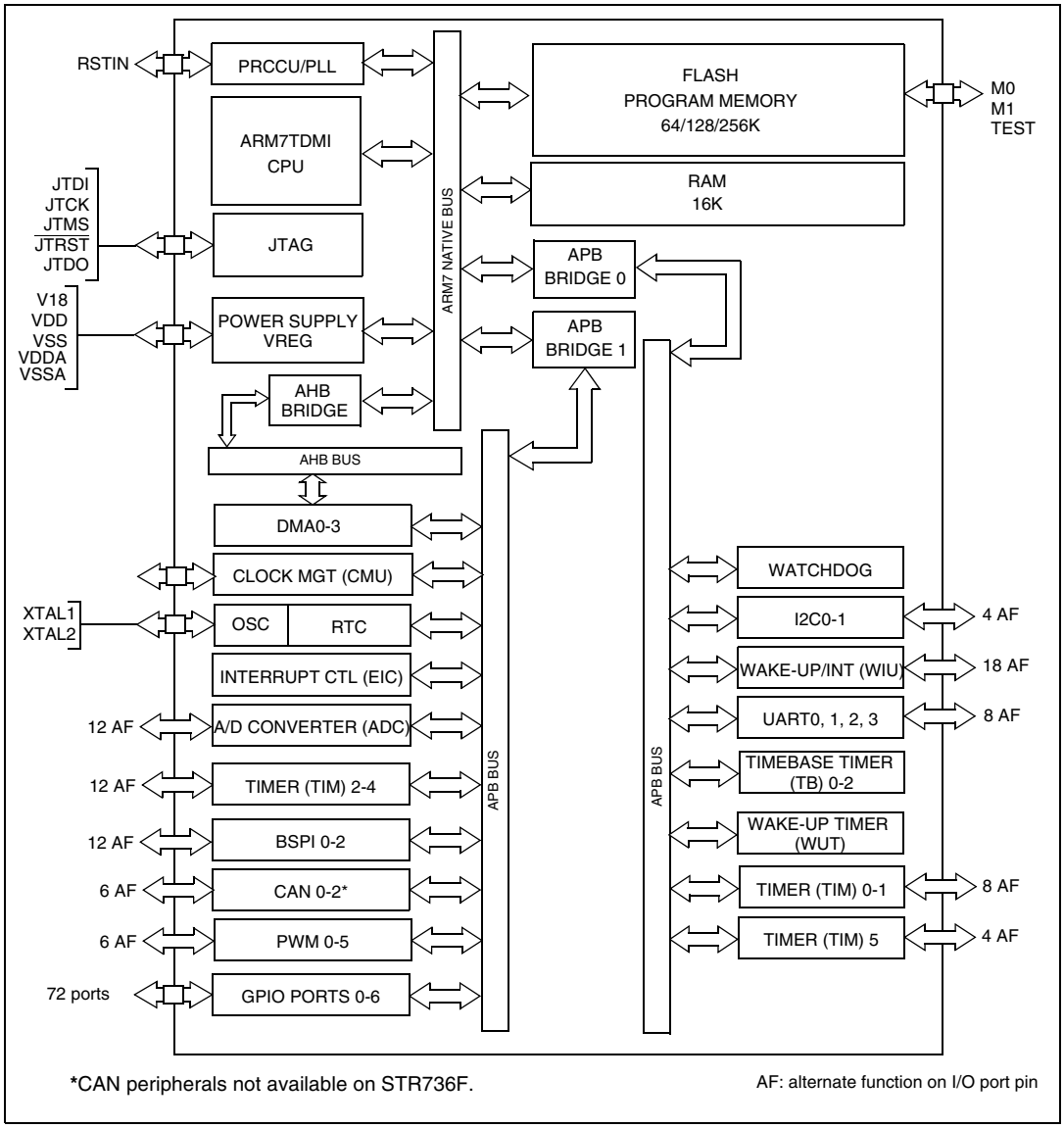
Timebase timers (TB)

The three 16-bit timebase timers with 8-bit prescaler for general purpose time triggering operations.

Real-time clock (RTC)

The RTC provides a set of continuously running counters driven by separate clock signal derived from the main oscillator. The RTC can be used as a general timebase or

Figure 2. STR731F/STR736 block diagram



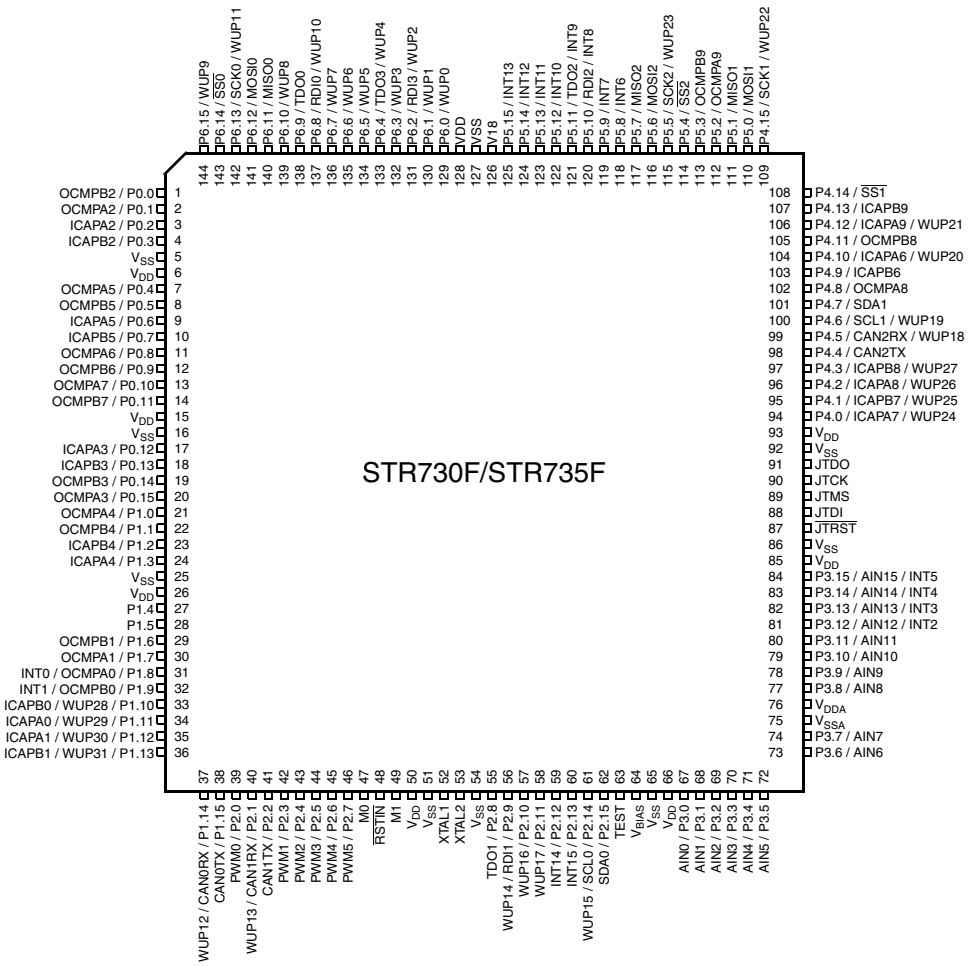
*CAN peripherals not available on STR736F.

AF: alternate function on I/O port pin

3.2 Pin description

3.2.1 STR730F/STR735F (TQFP144)

Figure 3. STR730F/STR735F pin configuration (top view)



Note: CAN alternate functions not available on STR735F.

3.2.2 STR730F/STR735F (LFBGA144)

Table 3. STR730F/STR735F LFBGA ball connections

Ball	Name	Ball	Name	Ball	Name	Ball	Name
A1	P0.0 / OCMPB2	B1	P0.4 / OCMPA5	C1	P0.5 / OCMPB5	D1	V_{SS}
A2	P6.10 / WUP8	B2	P0.1 / OCMPA2	C2	P0.2 / ICAPA2	D2	V_{DD}
A3	P6.9 / TDO0	B3	P6.15 / WUP9	C3	P0.3 / ICAPB2	D3	P0.6 / ICAPA5
A4	P6.12 / MOSI0	B4	P6.13 / SCKO / WUP11	C4	P6.14 / SSO	D4	P0.7 /ICAPB5
A5	P6.6 / WUP6	B5	P6.7 / WUP7	C5	P6.8 / RDI0 / WUP10	D5	P6.11 / MISO0
A6	V_{18}	B6	P6.2 / WUP2 / RDI3	C6	P6.3 / WUP3	D6	P6.4 / WUP4 /TDO3
A7	P5.15 / INT13	B7	P5.14 / INT12	C7	V_{SS}	D7	VDD
A8	P5.8 / INT6	B8	P5.9 / INT7	C8	P5.10 / INT8 / RDI2	D8	P5.12 / INT10
A9	P5.2 / OCMPA9	B9	P5.3 / OCMPB9	C9	P5.4 / SS2	D9	P5.5 / SCK2 / WUP23
A10	P5.7 / MISO2	B10	P5.0 / MOSI1	C10	P5.1 / MISO1	D10	P4.13 / ICAPB9
A11	P5.6 / MOSI2	B11	P4.15 / SCK1 / WUP22	C11	P4.14 / SS1	D11	P4.12 / ICAPA9 / WUP21
A12	P5.11 / TDO2 / INT9	B12	P4.8 / OCMPA8	C12	P4.7 / SDA1	D12	P4.11 / OCMPB8
E1	P0.8 / OCMPA6	F1	V_{DD}	G1	V_{SS}	H1	V_{DD}
E2	P0.9 / OCMPB6	F2	P0.13 / ICAPB3	G2	P1.2 / ICAPB4	H2	P1.8 / OCMPA0 / INT0
E3	P0.10 / OCMPA7	F3	P0.14 / OCMPB3	G3	P1.3 / ICAPA4	H3	P1.9 / OCMPB0 / INT1
E4	P0.11 / OCMPB7	F4	P0.15 / OCMPA3	G4	V_{SS}	H4	P1.10 / ICAPB0 / WUP28
E5	P0.12 / ICAPA3	F5	P1.0 / OCMPA4	G5	P1.5	H5	XTAL2
E6	P6.5 / WUP5	F6	P1.1 / OCMPB4	G6	P2.11 / WUP17	H6	P2.10 / WUP16
E7	P6.0 / WUP0	F7	P6.1 / WUP1	G7	P4.0 / ICAPA7 / WUP24	H7	P2.15 / SDA 0
E8	P5.13 / INT11	F8	P4.4 / CAN2TX[1)]	G8	VDD	H8	JTMS
E9	P4.10 / ICAPA6 / WUP20	F9	P4.3 / ICAPB8 / WUP27	G9	VSS	H9	VSS
E10	P4.9 / ICAPB6	F10	P4.2 / ICAPA8 / WUP26	G10	JTDO	H10	VDD
E11	P4.6 / SCL1 / WUP19	F11	P4.1 / ICAPB7 / WUP25	G11	JTCK	H11	P3.15 / AIN15 / INT5
E12	P4.5 / WUP18 / CAN2RX[1)]	F12	JTDI	G12	nJTRST	H12	P3.14 / AIN14 / INT4
J1	P1.4	K1	P1.6 / OCMPB1	L1	P1.7 / OCMPA1	M1	P1.14 / CAN0RX[1)] / WUP12
J2	P1.11 / ICAPA0 / WUP29	K2	P1.13 / ICAPB1 / WUP31	L2	P1.15 / CAN0TX[1)]	M2	P2.4 / PWM2
J3	P1.12 / ICAPA1 / WUP30	K3	P2.1 / CAN1RX[1)] / WUP13	L3	P2.0 / PWM0	M3	P2.5 / PWM3
J4	P2.7 / PWM5	K4	P2.6 / PWM4	L4	P2.3 / PWM1	M4	P2.2 / CAN1TX[1)]
J5	V_{DD}	K5	M1	L5	RSTIN	M5	M0
J6	P2.9 / RDI1 / WUP14	K6	P2.8 / TDO1	L6	V_{SS}	M6	V_{SS}
J7	P2.14 / SCL 0 / WUP15	K7	P2.13 / INT15	L7	P2.12 / INT14	M7	XTAL1
J8	P3.1 / AIN1	K8	P3.0 / AIN0	L8	VBIAS	M8	TST
J9	P3.13 / AIN13 / INT3	K9	P3.4 / AIN4	L9	P3.3 / AIN3	M9	P3.2 / AIN2
J10	P3.12 / AIN12 / INT2	K10	V_{DDA}	L10	P3.5 / AIN5	M10	V_{SS}
J11	P3.9 / AIN9	K11	V_{SSA}	L11	P3.7 / AIN7	M11	V_{DD}
J12	P3.8 / AIN8	K12	P3.11 / AIN11	L12	P3.10 / AIN10	M12	P3.6 / AIN6

Note: CAN alternate functions not available on STR735F.

Table 4. STR73xF pin description

Pin n°			Pin name	Type	Input			Output			Main function (after reset)	Alternate function
TQFP144	LFBGA144	TQFP100			Input Level	pu/pd	interrupt	Capability	OD	PP		
73	M12	51	P3.6/AIN6	I/O	T_T			2mA	X	X	Port 3.6	ADC: analog input 6 (AIN2 in TQFP100)
74	L11	52	P3.7/AIN7	I/O	T_T			2mA	X	X	Port 3.7	ADC: analog input 7 (AIN3 in TQFP100)
75	K11	53	V_{SSA}	S							Reference ground for A/D converter	
76	K10	54	V_{DDA}	S							Reference voltage for A/D converter	
77	J12	55	P3.8/AIN8	I/O	T_T			2mA	X	X	Port 3.8	ADC: analog input 8 (AIN4 in TQFP100)
78	J11	56	P3.9/AIN9	I/O	T_T			2mA	X	X	Port 3.9	ADC: analog input 9 (AIN5 in TQFP100)
79	L12	57	P3.10/AIN10	I/O	T_T			2mA	X	X	Port 3.10	ADC: analog input 10 (AIN6 in TQFP100)
80	K12	58	P3.11/AIN11	I/O	T_T			2mA	X	X	Port 3.11	ADC: analog input 11 (AIN7 in TQFP100)
81	J10	59	P3.12/AIN12	I/O	T_T		INT2	2mA	X	X	Port 3.12	ADC: analog input 12 (AIN8 in TQFP100)
82	J9	60	P3.13/AIN13	I/O	T_T		INT3	2mA	X	X	Port 3.13	ADC: analog input 13 (AIN9 in TQFP100)
83	H12	61	P3.14/AIN14	I/O	T_T		INT4	2mA	X	X	Port 3.14	ADC: analog input 14 (AIN10 in TQFP100)
84	H11	62	P3.15/AIN15	I/O	T_T		INT5	2mA	X	X	Port 3.15	ADC: analog input 15 (AIN11 in TQFP100)
85	H10	63	V_{DD}	S							Supply voltage (5 V)	
86	H9	64	V_{SS}	S							Ground	
87	G12	65	JTRST	I	T_T	pu						JTAG reset Input
88	F12	66	JTDI	I	T_T	pu						JTAG data input
89	H8	67	JTMS	I	T_T	pu						JTAG mode selection Input
90	G11	68	JTCK	I	T_T	pd						JTAG clock Input
91	G10	69	JTDO	O				4mA				JTAG data output. **Note:** Reset state = HiZ
92	G9	70	V_{SS}	S								Ground
93	G8	71	V_{DD}	S								Supply voltage (5 V)
94	G7		P4.0/ICAPA7	I/O	T_T		WUP24	2mA	X	X	Port 4.0	TIM7: input capture A input
95	F11		P4.1/ICAPB7	I/O	T_T		WUP25	2mA	X	X	Port 4.1	TIM7: input capture B input
96	F10		P4.2/ICAPA8	I/O	T_T		WUP26	2mA	X	X	Port 4.2	TIM8: input capture A input

Table 4. STR73xF pin description

Pin n°			Pin name	Type	Input			Output			Main function (after reset)	Alternate function	
TQFP144	LFBGA144	TQFP100			Input Level	pu/pd	interrupt	Capability	OD	PP			
97	F9		P4.3/ICAPB8	I/O	T_T		WUP27	2mA	X	X	Port 4.3	TIM8: input capture B input	
98	F8		P4.4/CAN2TX	I/O	T_T			2mA	X	X	Port 4.4	CAN2: transmit data output	
99	E12		P4.5/CAN2RX	I/O	T_T		WUP18	2mA	X	X	Port 4.5	CAN2: receive data input	
100	E11	72	P4.6/SCL1	I/O	T_T		WUP19	2mA	X	X	Port 4.6	I2C1: serial clock	
101	C12	73	P4.7/SDA1	I/O	T_T			2mA	X	X	Port 4.7	I2C1: serial data	
102	B12		P4.8/OCMPA8	I/O	T_T			2mA	X	X	Port 4.8	TIM8: output compare A output	
103	E10		P4.9/ICAPB6	I/O	T_T			2mA	X	X	Port 4.9	TIM6: input capture B input	
104	E9	74	P4.10/ICAPA6/ICAPB5	I/O	T_T		WUP20	2mA	X	X	Port 4.10	TIM6: input capture A input (144-pin pkg only)	TIM5: input capture B input (TQFP100 only)
105	D12		P4.11/OCMPB8	I/O	T_T			2mA	X	X	Port 4.11	TIM8: output compare B output	
106	D11		P4.12/ICAPA9	I/O	T_T		WUP21	2mA	X	X	Port 4.12	TIM9: input capture A input	
107	D10		P4.13/ICAPB9	I/O	T_T			2mA	X	X	Port 4.13	TIM9: input capture B input	
108	C11	75	P4.14/$\overline{SS}$1	I/O	T_T			2mA	X	X	Port 4.14	BSPI1: slave select	
109	B11	76	P4.15/SCK1	I/O	T_T		WUP22	2mA	X	X	Port 4.15	BSPI1: serial clock	
110	B10	77	P5.0/MOSI1	I/O	T_T			2mA	X	X	Port 5.0	BSPI1: master output/slave input	
111	C10	78	P5.1/MISO1	I/O	T_T			2mA	X	X	Port 5.1	BSPI1: master input/Slave output	
112	A9		P5.2/OCMPA9	I/O	T_T			2mA	X	X	Port 5.2	TIM9: output compare A output	
113	B9		P5.3/OCMPB9	I/O	T_T			2mA	X	X	Port 5.3	TIM9: output compare B output	
114	C9	79	P5.4/$\overline{SS}$2/PWM3	I/O	T_T			2mA	X	X	Port 5.4	BSPI2: slave select	PWM3: PWM output (TQFP100 only)
115	D9	80	P5.5/SCK2	I/O	T_T		WUP23	2mA	X	X	Port 5.5	BSPI2: serial clock	
116	A11	81	P5.6/MOSI2	I/O	T_T			2mA	X	X	Port 5.6	BSPI2: master output/slave input	
117	A10	82	P5.7/MISO2	I/O	T_T			2mA	X	X	Port 5.7	BSPI2: master input/slave output	
118	A8	83	P5.8/PWM4	I/O	T_T		INT6	2mA	X	X	Port 5.8	PWM4: PWM output (TQFP100 only)	

Table 4. STR73xF pin description

Pin n°			Pin name	Type	Input			Output			Main function (after reset)	Alternate function
TQFP144	LFBGA144	TQFP100			Input Level	pu/pd	interrupt	Capability	OD	PP		
119	B8	84	P5.9/PWM5	I/O	T_T		INT7	2mA	X	X	Port 5.9	PWM5: PWM output (TQFP100 only)
120	C8	85	P5.10/RDI2	I/O	T_T		INT8	2mA	X	X	Port 5.10	UART2: receive data input
121	A12	86	P5.11/TDO2	I/O	T_T		INT9	2mA	X	X	Port 5.11	UART2: transmit data output
122	D8	87	P5.12	I/O	T_T		INT10	2mA	X	X	Port 5.12	
123	E8		P5.13	I/O	T_T		INT11	2mA	X	X	Port 5.13	
124	B7		P5.14	I/O	T_T		INT12	2mA	X	X	Port 5.14	
125	A7		P5.15	I/O	T_T		INT13	2mA	X	X	Port 5.15	
126	A6	88	V_{18}	S								1.8 V decoupling pin: a decoupling capacitor (recommended value: 100 nF) must be connected between this pin and nearest VSS pin.
127	C7	89	V_{SS}	S								Ground
128	D7	90	V_{DD}	S								Supply voltage (5 V)
129	E7	91	P6.0	I/O	T_T		WUP0	8mA	X	X	Port 6.0	
130	F7		P6.1	I/O	T_T		WUP1	2mA	X	X	Port 6.1	
131	B6	92	P6.2/RDI3	I/O	T_T		WUP2	2mA	X	X	Port 6.2	UART3: receive data input
132	C6		P6.3	I/O	T_T		WUP3	2mA	X	X	Port 6.3	
133	D6	93	P6.4/TDO3	I/O	T_T		WUP4	2mA	X	X	Port 6.4	UART3: transmit data output
134	E6		P6.5	I/O	T_T		WUP5	2mA	X	X	Port 6.5	
135	A5	94	P6.6	I/O	T_T		WUP6	2mA	X	X	Port 6.6	
136	B5		P6.7	I/O	T_T		WUP7	2mA	X	X	Port 6.7	
137	C5	95	P6.8/RDI0	I/O	T_T		WUP10	2mA	X	X	Port 6.8	UART0: receive data input
138	A3	96	P6.9/TDO0	I/O	T_T			2mA	X	X	Port 6.9	UART0: transmit data output
139	A2		P6.10	I/O	T_T		WUP8	2mA	X	X	Port 6.10	
140	D5	97	P6.11/MISO0	I/O	T_T			2mA	X	X	Port 6.11	BSPI0: master input/slave output
141	A4	98	P6.12/MOSI0	I/O	T_T			2mA	X	X	Port 6.12	BSPI0: master output/slave input
142	B4	99	P6.13/SCK0	I/O	T_T		WUP11	2mA	X	X	Port 6.13	BSPI0: serial clock
143	C4	100	P6.14/$\overline{SS}$0	I/O	T_T			2mA	X	X	Port 6.14	BSPI0: slave select
144	B3		P6.15	I/O	T_T		WUP9	2mA	X	X	Port 6.15	

4 Electrical parameters

4.1 Parameter conditions

Unless otherwise specified, all voltages are referred to V_{SS}.

4.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A=25° C and T_A=T_{Amax} (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3Σ).

4.1.2 Typical values

Unless otherwise specified, typical data are based on T_A=25° C and V_{DD}=5 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2Σ).

4.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

4.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 6*.

4.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 7*.

Figure 6. Pin loading conditions

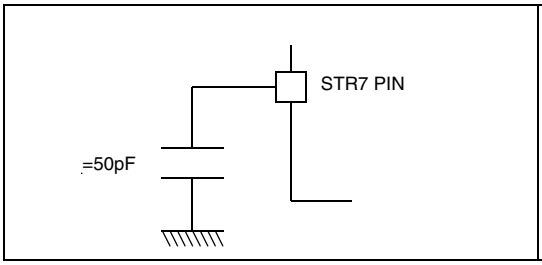


Figure 7. Pin input voltage

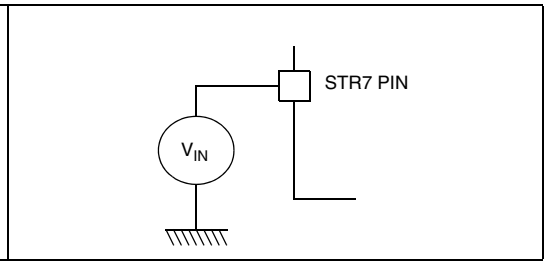


Table 7. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-55 to +150	°C
T_J	Maximum junction temperature (see *Section 5.2: Thermal characteristics on page 48*)		

4.3 Operating conditions

Subject to general operating conditions for V_{DD}, and T_A.

Table 8. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCLK}	Internal CPU and system clock frequency	Accessing SRAM or Flash (zero wait state Flash access up to 36 MHz)	0	36	MHz
V_{DD}	Standard Operating Voltage		4.5	5.5	V
V_{DDA}	Operating analog reference voltage with respect to ground		4.5	V_{DD}+0.1	V
T_A	Ambient temperature range	6 partnumber suffix 7 partnumber suffix	-40 -40	85 105	°C

Table 9. Operating conditions at power-up / power-down

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{VDD}	V_{DD} rise time rate	Subject to general operating conditions for T_A.	-	20	-	ms/V

4.3.1 Supply current characteristics

The current consumption is measured as described in *Figure 6* and *Figure 7*.

Total current consumption

The MCU is placed under the following conditions:

- All I/O pins in input mode with a static value at V_{DD} or V_{SS} (no load)
- All peripherals are disabled except if explicitly mentioned.

Subject to general operating conditions for V_{DD}, and T_A.

Table 10. Total current consumption

Symbol	Parameter	Conditions	Typ [1]	Max [2]	Unit
I_{DD}	RUN mode[3]	Formula, f_{MCLK} in MHz, RAM execution	7 + 1.9 f_{MCLK}		mA
		f_{MCLK} = 36 MHz, RAM execution	76		mA
		f_{MCLK} = 36 MHz, Flash execution	86		mA
	WFI mode	f_{OSC} = 4 MHz, f_{MCLK}= f_{OSC}/16 = 250 kHz Main voltage regulator ON, LP voltage regulator = 2 mA, RTC and WDG on, other modules off.	6.7	8	mA
	LPWFI mode	f_{RC} = high frequency (CMU_RCCTL= 0x8), f_{MCLK}= f_{RC} /16, LP voltage regulator = 2 mA, other modules off.	220	350	µA
	STOP mode	f_{OSC} = 4 MHz, RC oscillator on f_{RC} = high frequency (CMU_RCCTL= 0x0) LP voltage regulator = 6 mA, RTC and WUT ON, other modules off. Internal wake-up possible.	500	700	µA
		f_{RC} = high frequency (CMU_RCCTL= 0xF), LP voltage regulator = 2mA. WUT ON, other modules off. Internal wake-up possible.	150	220	
		LP voltage regulator = 2 mA, WIU on, Other modules off, external wake-up.	50	140	
	HALT mode	LP voltage regulator = 2 mA.	50	140	µA

1. Typical data are based on T_A=25° C, V_{DD}=5 V
2. Data based on characterization results, tested in production at V_{DD} max. and T_A = 25° C.
3. I/O in static configuration (not toggling). RUN mode is almost **independent of temperature**. On the contrary RUN mode current is **highly dependent on the application**. The I_{DDRUN} value can be significantly reduced by the application in the following ways: switch-off unused peripherals (default), reduce peripheral frequency through internal prescaler, fetch the most frequently-used functions from RAM and use low power mode when possible.

Main oscillator characteristics

V_{DD} = 5 V ± 10%, T_A = -40° C to T_{Amax}, unless otherwise specified.

Table 14. Main oscillator characteristics

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
f_{OSC}	Oscillator frequency		4		8	MHz
g_m	Oscillator transconductance		1.5		4.2	mA/V
V_{OSC} 1)	Oscillation amplitude	f_{OSC} = 4 MHz, T_A= 25° C	-	2.4	-	V
		f_{OSC} = 8 MHz, T_A= 25° C		1.-		
V_{AV} 1)	Oscillator operating point	Sine wave middle, T_A= 25° C	-	0.77	-	v
t_{STUP} 1)	Oscillator start-up time	External crystal, V_{DD} = 5.5 V, f_{OSC} = 4 MHz, T_A=-40° C	-	-	12	ms
		External crystal, V_{DD} = 5.0 V, f_{OSC} = 4 MHz, T_A=25° C	-	5.5	-	ms
		External crystal, V_{DD} = 5.5 V, f_{OSC} = 6 MHz, T_A=-40° C	-	-	8	ms
		External crystal, V_{DD} = 5.0 V, f_{OSC} = 6 MHz, T_A=25° C	-	3.3	-	ms
		External crystal, V_{DD} = 5.5 V, f_{OSC} = 8 MHz, T_A=-40° C	-	-	7	ms
		External crystal, V_{DD} = 5.0 V, f_{OSC} = 8 MHz, T_A= 25° C	-	2.7	-	ms

PLL electrical characteristics

V_{DD} = 5 V ± 10%, T_A = -40° C to T_{Amax}, unless otherwise specified

Table 16. PLL characteristics

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
f_{PLLIN} (1)	PLL reference clock	FREF_RANGE = '0' FREF_RANGE = '1'	1.5 3.0		3.0 5.0	MHz
f_{PLLOUT}	PLL output clock	MX = "00" MX = "01" MX = "10" MX = "11"	20 x f_{PLLIN} 12 x f_{PLLIN} 28 x f_{PLLIN} 16 x f_{PLLIN}			MHz
f_{MCLK}	System clock	DX = 1..7	f_{PLLOUT}/DX		36	MHz
f_{FREE} (2)	PLL free running frequency	FREF_RANGE = '0', MX0 = '1' FREF_RANGE = '0', MX0 = '0' FREF_RANGE = '1', MX0 = '1' FREF_RANGE = '1', MX0 = '0'		120 240 240 480		kHz
t_{LOCK} (3)	PLL lock time	Stable oscillator (f_{PLLIN} = 4 MHz), stable V_{DD}		100	300	µs
Δt_{PKJIT}	PLL jitter (pk to pk)	f_{PLLIN} = 4 MHz (pulse generator)			1.5	ns

1. f_{PLLIN} is obtained from f_{OSC} directly or through an optional divider by 2.
2. Typical data are based on T_A=25°C, V_{DD}=5V
3. Max value is guaranteed by characterization, not tested in production.

Table 17. Low-power mode wake-up timing

Symbol	Parameter	Conditions	Typ	Unit
t_{WUHALT}	Wake-up from HALT mode		200	µs
t_{WUSTOP}	Wake-up from STOP mode	RC high frequency in STOP mode	180	µs
		RC low frequency in STOP mode	234	µs
$t_{WULPWFI}$ 1)	Wake-up from LPWFI mode	Main voltage regulator on RC oscillator off f_{OSC} = 4 MHz, f_{MCLK}= f_{OSC}/16 RAM or FLASH execution	27	µs
		Main voltage regulator on RC oscillator = high frequency Flash execution	46	µs
		Main voltage regulator on RC oscillator = low frequency Flash execution	3.6	ms

1. Flash memory programmed to enter Power Down mode during LPWFI.

Electromagnetic interference (EMI)

Based on a simple application running on the product (toggling 2 LEDs through the I/O ports), the product is monitored in terms of emission. This emission test is in line with the norm SAE J 1752/3 which specifies the board and the loading of each pin.

Table 20. EMI data

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{OSC4M}/f_{MCLK}]		Unit
				6/36 MHz	8/8 MHz	
S_{EMI}	Peak level	V_{DD}=5.0V, T_A=+25°C, All packages	0.1 MHz to 30 MHz	23	30	dBµV
			30 MHz to 130 MHz	37	34	
			130 MHz to 1 GHz	20	7	
			SAE EMI Level	4	3.5	-

Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU and DLU) using specific measurement methods, the product is stressed in order to determine its performance in terms of electrical sensitivity. For more details, refer to the application note AN1181.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts*(n+1) supply pin). Two models can be simulated: human body model and machine model. This test conforms to the JESD22-A114A/A115A standard.

Table 21. ESD Absolute Maximum ratings

Symbol	Ratings	Conditions	Maximum value [1]	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A=+25° C	2000	V
$V_{ESD(MM)}$	Electrostatic discharge voltage (machine model)		200	
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)		750 on corner pins, 500 on others	

Notes:

1. Data based on characterization results, not tested in production.

Static and dynamic latch-up

- **LU**: 3 complementary static tests are required on 10 parts to assess the latch-up performance. A supply overvoltage (applied to each power supply pin) and a current injection (applied to each input, output and configurable I/O pin) are performed on each

Output driving current

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified.

Table 24. Output driving current

I/O Type	Symbol	Parameter	Conditions	Min	Max	Unit
Standard	V_{OL} 1)	Output low level voltage for an I/O pin when 8 pins are sunk at same time	I_{IO}=+2 mA		0.4	V
	V_{OH} 2)	Output high level voltage for an I/O pin when 4 pins are sourced at same time	I_{IO}=-2 mA	V_{DD}-0.8		
Med. Current (JTDO)	V_{OL} 1)	Output low level voltage for an I/O pin	I_{IO}=+6 mA		0.4	
	V_{OH} 2)	Output high level voltage for an I/O pin	I_{IO}=-6 mA	V_{DD}-0.8		
High Current P6.0	V_{OL} 1)	Output low level voltage for an I/O pin	I_{IO}=+8 mA		0.4	
	V_{OH} 2)	Output high level voltage for an I/O pin	I_{IO}=-8 mA	V_{DD}-0.8		

1. The I_{IO} current sunk must always respect the absolute maximum rating specified in *Table 6* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
2. The I_{IO} current sourced must always respect the absolute maximum rating specified in *Table 6* and the sum of I_{IO} (I/O ports and control pins) must not exceed IV_{DD}.

Figure 13. V_{OH} standard ports vs I_{OH} @ V_{DD} 5V T_A -45° C

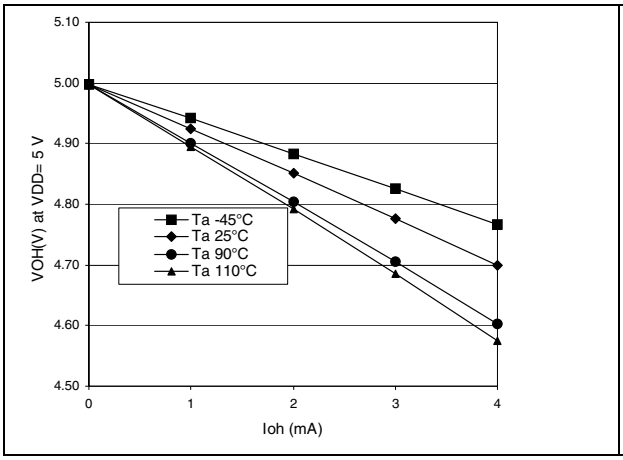


Figure 14. V_{OL} standard ports vs I_{OL} @ V_{DD} 5 V

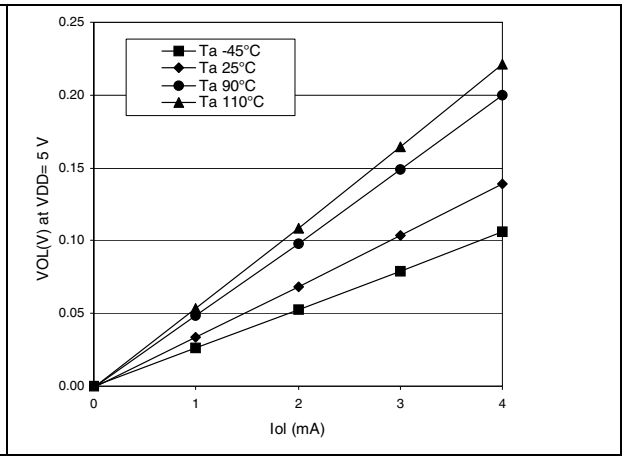


Figure 15. V_{OH} JTDO pin vs I_{OL} @ V_{DD} 5 V

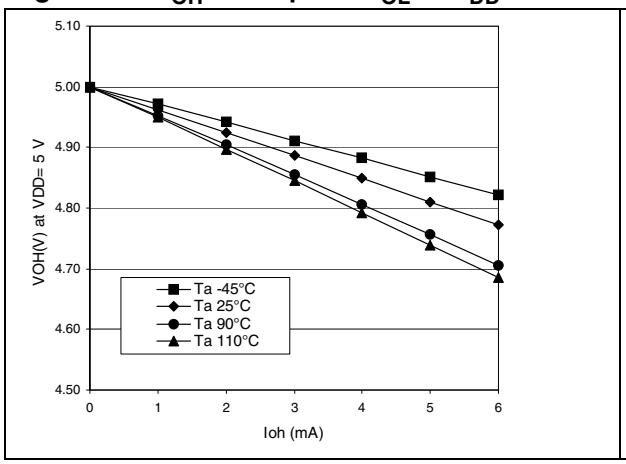


Figure 16. V_{OL} JTDO pin vs I_{OL} @ V_{DD} 5 V

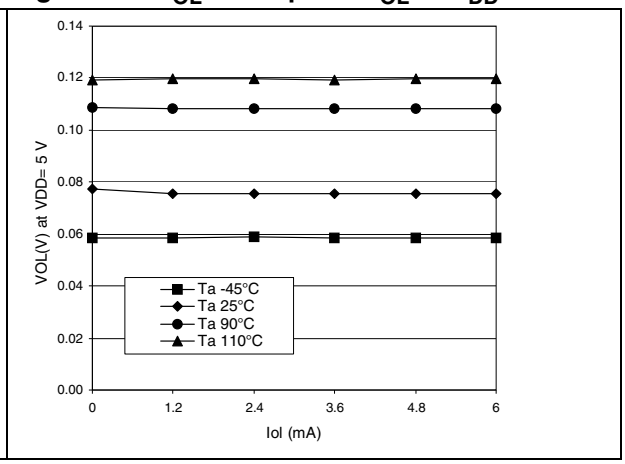


Figure 17. V_{OH} P6.0 pin vs I_{OL} @ V_{DD} 5 V

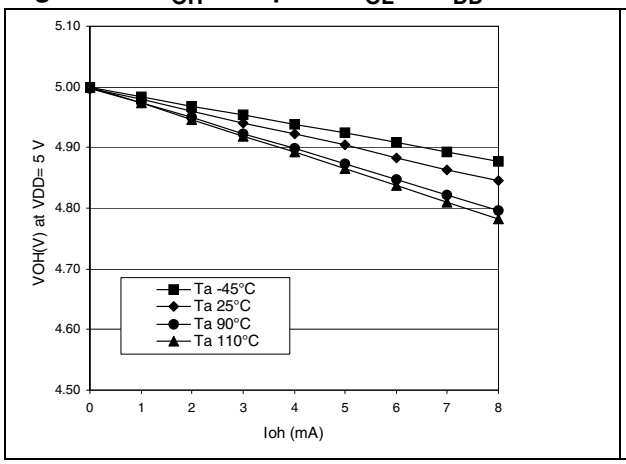
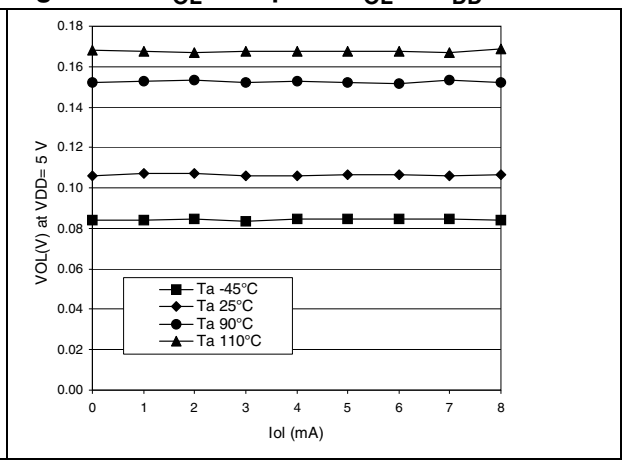


Figure 18. V_{OL} P6.0 pin vs I_{OL} @ V_{DD} 5 V



4.3.6 10-bit ADC characteristics

Subject to general operating conditions for V_{DDA}, f_{MCLK}, and T_A unless otherwise specified.

Table 26. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
f_{ADC}			0.4		10	MHz
V_{AIN}	Conversion voltage range [2]		V_{SSA}		V_{DDA}	V
I_{lkg}	Negative input leakage current on analog pins	$V_{IN}<V_{SS,}$ | I_{IN} |< 400 µA on adjacent analog pin		5	6	µA
C_{ADC}	Internal sample and hold capacitor				3.5	pF
t_{CAL} [2]	Calibration time	f_{ADC} = 10 MHz	580.2			µs
			5802			$1/f_{ADC}$
t_S [3]	Sampling time	f_{ADC} = 10 MHz	1		14	µs
t_{CONV}	Total conversion time (including sampling time)	f_{ADC} = 10 MHz	3			µs
			30 (10 for sampling +20 for successive approximation)			$1/f_{ADC}$
I_{ADC}	Running mode	Normal mode			5	mA
	Power-down mode				1	µA

1. Unless otherwise specified, typical data are based on T_A=25°C and V_{DDA}-V_{SS}=5.0V. They are given only as design guidelines and are not tested.
2. Calibration is recommended once after each power-up.
3. During the sample time the input capacitance C_{AIN} (6.8 max) can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_S. After the end of the sample time t_S, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_S depend on programming.

8 Revision history

Table 30. Document revision history

Date	Revision	Description of changes
19-Sep-2005	1	First release
02-Nov-2005	2	Removed Table 8 power consumption in LP modes Updated PLL frequency in *Section 1.1* and *Table 12*
08-Mar-2006	3	*Section 3.4: Preliminary power consumption data* updated *Section 3.5: DC electrical characteristics* updated *Section 7: Known limitations* added
04-Jun-2006	4	*Section 4: Electrical parameters* updated *Section 7: Known limitations* updated Added temperature range -40°C to 85°C in *Section 6: Order codes*
19-Jun-2006	5	Changed Flash data retention to 20 years at 85°C in *Table 18 on page 34*.
08-Sep-2006	6	Changed *Table 24: Output driving current on page 39* Added *Figure 14: VOL standard ports vs IOL @ VDD 5 V* thru *Figure 18: VOL P6.0 pin vs IOL @ VDD 5 V on page 40*. Added *Figure 20: NRSTIN RPU vs. VDD*
08-Jun-2008	7	Inch values rounded to 4 decimal digits in *Section 5.1: Package mechanical data* Modified BSPI speed in *Section 2.1: On-chip peripherals*

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST’s terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST’S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

UNLESS EXPRESSLY APPROVED IN WRITING BY AN AUTHORIZED ST REPRESENTATIVE, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS "AUTOMOTIVE GRADE" MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER’S OWN RISK.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com