Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, LINbus, SIO, SSU, UART/USART
Peripherals	POR, PWM, Voltage Detect, WDT
Number of I/O	15
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-LSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-LSSOP
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f21322mnsp-u0

Table 1.4 Pin Name Information by Pin Number

Pin Number	Control Pin	Port	I/O Pin Functions for Peripheral Modules					
			Interrupt	Timer	Serial Interface	SSU	I^{2}C bus	A/D Converter, Comparator A, Comparator B
1		P4_2						VREF
2	MODE							
3	$\overline{\text{RESET}}$							
4	XOUT(/XCOUT)	P4_7						
5	VSS/AVSS							
6	XIN(/XCIN)	P4_6						
7	VCC/AVCC							
8		P3_7		TRAO	(RXD2/SCL2/ TXD2/SDA2)	SSO	SDA	
9		P3_5		(TRCIOD)	(CLK2)	SSCK	SCL	
10		P3_4		(TRCIOC)	(RXD2/SCL2/ TXD2/SDA2)	SSI		IVREF3
11		P3_3	$\overline{\text{INT3}}$	(TRCCLK)	($\overline{\text{CTS2}}$/$\overline{\text{RTS2}}$)	$\overline{\text{SCS}}$		IVCMP3
12		P4_5	$\overline{\text{INT0}}$		(RXD2/SCL2)			$\overline{\text{ADTRG}}$
13		P1_7	$\overline{\text{INT1}}$	(TRAIO)				IVCMP1
14		P1_6			(CLK0)			LVCOUT2/IVREF1
15		P1_5	($\overline{\text{INT1}}$)	(TRAIO)	(RXD0)			
16		P1_4		(TRCCLK)	(TXD0)			
17		P1_3	$\overline{\text{KI3}}$	TRBO (/TRCIOC)				AN11/LVCOUT1
18		P1_2	$\overline{\text{KI2}}$	(TRCIOB)				AN10/LVREF
19		P1_1	$\overline{\text{KI1}}$	(TRCIOA/ TRCTRG)				AN9/LVCMP2
20		P1_0	$\overline{\text{KI0}}$	(TRCIOD)				AN8/LVCMP1

Note:
1. Can be assigned to the pin in parentheses by a program.

Table 4.2   SFR Information (2) [1]

Address	Register	Symbol	After Reset
003Ah	Voltage Monitor 2 Circuit Control Register	VW2C	10000010b
003Bh			
003Ch			
003Dh			
003Eh			
003Fh			
0040h			
0041h	Flash Memory Ready Interrupt Control Register	FMRDYIC	XXXXX000b
0042h			
0043h			
0044h			
0045h			
0046h			
0047h	Timer RC Interrupt Control Register	TRCIC	XXXXX000b
0048h			
0049h			
004Ah	Timer RE Interrupt Control Register	TREIC	XXXXX000b
004Bh	UART2 Transmit Interrupt Control Register	S2TIC	XXXXX000b
004Ch	UART2 Receive Interrupt Control Register	S2RIC	XXXXX000b
004Dh	Key Input Interrupt Control Register	KUPIC	XXXXX000b
004Eh	A/D Conversion Interrupt Control Register	ADIC	XXXXX000b
004Fh	SSU Interrupt Control Register / IIC bus Interrupt Control Register [2]	SSUIC / IICIC	XXXXX000b
0050h			
0051h	UART0 Transmit Interrupt Control Register	S0TIC	XXXXX000b
0052h	UART0 Receive Interrupt Control Register	S0RIC	XXXXX000b
0053h			
0054h			
0055h			
0056h	Timer RA Interrupt Control Register	TRAIC	XXXXX000b
0057h			
0058h	Timer RB Interrupt Control Register	TRBIC	XXXXX000b
0059h	INT1 Interrupt Control Register	INT1IC	XX00X000b
005Ah	INT3 Interrupt Control Register	INT3IC	XX00X000b
005Bh			
005Ch			
005Dh	INT0 Interrupt Control Register	INT0IC	XX00X000b
005Eh	UART2 Bus Collision Detection Interrupt Control Register	U2BCNIC	XXXXX000b
005Fh			
0060h			
0061h			
0062h			
0063h			
0064h			
0065h			
0066h			
0067h			
0068h			
0069h			
006Ah			
006Bh			
006Ch			
006Dh			
006Eh			
006Fh			
0070h			
0071h			
0072h	Voltage Monitor 1 / Comparator A1 Interrupt Control Register	VCMP1IC	XXXXX000b
0073h	Voltage Monitor 2 / Comparator A2 Interrupt Control Register	VCMP2IC	XXXXX000b
0074h			
0075h			
0076h			
0077h			
0078h			
0079h			
007Ah			
007Bh			
007Ch			
007Dh			
007Eh			
007Fh			

X: Undefined

Notes:
1. The blank areas are reserved and cannot be accessed by users.
2. Selectable by the IICSEL bit in the SSUIICSR register.

Table 4.3 SFR Information (3) [1]

Address	Register	Symbol	After Reset
0080h	DTC Activation Control Register	DTCTL	00h
0081h			
0082h			
0083h			
0084h			
0085h			
0086h			
0087h			
0088h	DTC Activation Enable Register 0	DTCEN0	00h
0089h	DTC Activation Enable Register 1	DTCEN1	00h
008Ah	DTC Activation Enable Register 2	DTCEN2	00h
008Bh	DTC Activation Enable Register 3	DTCEN3	00h
008Ch			
008Dh	DTC Activation Enable Register 5	DTCEN5	00h
008Eh	DTC Activation Enable Register 6	DTCEN6	00h
008Fh			
0090h			
0091h			
0092h			
0093h			
0094h			
0095h			
0096h			
0097h			
0098h			
0099h			
009Ah			
009Bh			
009Ch			
009Dh			
009Eh			
009Fh			
00A0h	UART0 Transmit / Receive Mode Register	U0MR	00h
00A1h	UART0 Bit Rate Register	U0BRG	XXh
00A2h	UART0 Transmit Buffer Register	U0TB	XXh
00A3h			XXh
00A4h	UART0 Transmit / Receive Control Register 0	U0C0	00001000b
00A5h	UART0 Transmit / Receive Control Register 1	U0C1	00000010b
00A6h	UART0 Receive Buffer Register	U0RB	XXh
00A7h			XXh
00A8h	UART2 Transmit / Receive Mode Register	U2MR	00h
00A9h	UART2 Bit Rate Register	U2BRG	XXh
00AAh	UART2 Transmit Buffer Register	U2TB	XXh
00ABh			XXh
00ACh	UART2 Transmit / Receive Control Register 0	U2C0	00001000b
00ADh	UART2 Transmit / Receive Control Register 1	U2C1	00000010b
00AEh	UART2 Receive Buffer Register	U2RB	XXh
00AFh			XXh
00B0h	UART2 Digital Filter Function Select Register	URXDF	00h
00B1h			
00B2h			
00B3h			
00B4h			
00B5h			
00B6h			
00B7h			
00B8h			
00B9h			
00BAh			
00BBh	UART2 Special Mode Register 5	U2SMR5	00h
00BCh	UART2 Special Mode Register 4	U2SMR4	00h
00BDh	UART2 Special Mode Register 3	U2SMR3	000X0X0Xb
00BEh	UART2 Special Mode Register 2	U2SMR2	X0000000b
00BFh	UART2 Special Mode Register	U2SMR	X0000000b

X: Undefined
Note:
1. The blank areas are reserved and cannot be accessed by users.

Table 4.4   SFR Information (4) [1]

Address	Register	Symbol	After Reset
00C0h	A/D Register 0	AD0	XXh
00C1h			000000XXb
00C2h	A/D Register 1	AD1	XXh
00C3h			000000XXb
00C4h	A/D Register 2	AD2	XXh
00C5h			000000XXb
00C6h	A/D Register 3	AD3	XXh
00C7h			000000XXb
00C8h	A/D Register 4	AD4	XXh
00C9h			000000XXb
00CAh	A/D Register 5	AD5	XXh
00CBh			000000XXb
00CCh	A/D Register 6	AD6	XXh
00CDh			000000XXb
00CEh	A/D Register 7	AD7	XXh
00CFh			000000XXb
00D0h			
00D1h			
00D2h			
00D3h			
00D4h	A/D Mode Register	ADMOD	00h
00D5h	A/D Input Select Register	ADINSEL	11000000b
00D6h	A/D Control Register 0	ADCON0	00h
00D7h	A/D Control Register 1	ADCON1	00h
00D8h			
00D9h			
00DAh			
00DBh			
00DCh			
00DDh			
00DEh			
00DFh			
00E0h			
00E1h	Port P1 Register	P1	XXh
00E2h			
00E3h	Port P1 Direction Register	PD1	00h
00E4h			
00E5h	Port P3 Register	P3	XXh
00E6h			
00E7h	Port P3 Direction Register	PD3	00h
00E8h	Port P4 Register	P4	XXh
00E9h			
00EAh	Port P4 Direction Register	PD4	00h
00EBh			
00ECh			
00EDh			
00EEh			
00EFh			
00F0h			
00F1h			
00F2h			
00F3h			
00F4h			
00F5h			
00F6h			
00F7h			
00F8h			
00F9h			
00FAh			
00FBh			
00FCh			
00FDh			
00FEh			
00FFh			

X: Undefined
Note:
1.   The blank areas are reserved and cannot be accessed by users.

Table 4.5   SFR Information (5) [1]

Address	Register	Symbol	After Reset
0100h	Timer RA Control Register	TRACR	00h
0101h	Timer RA I/O Control Register	TRAIOC	00h
0102h	Timer RA Mode Register	TRAMR	00h
0103h	Timer RA Prescaler Register	TRAPRE	FFh
0104h	Timer RA Register	TRA	FFh
0105h	LIN Control Register 2	LINCR2	00h
0106h	LIN Control Register	LINCR	00h
0107h	LIN Status Register	LINST	00h
0108h	Timer RB Control Register	TRBCR	00h
0109h	Timer RB One-Shot Control Register	TRBOCR	00h
010Ah	Timer RB I/O Control Register	TRBIOC	00h
010Bh	Timer RB Mode Register	TRBMR	00h
010Ch	Timer RB Prescaler Register	TRBPRE	FFh
010Dh	Timer RB Secondary Register	TRBSC	FFh
010Eh	Timer RB Primary Register	TRBPR	FFh
010Fh			
0110h			
0111h			
0112h			
0113h			
0114h			
0115h			
0116h			
0117h			
0118h	Timer RE Second Data Register / Counter Data Register	TRESEC	00h
0119h	Timer RE Minute Data Register / Compare Data Register	TREMIN	00h
011Ah	Timer RE Hour Data Register	TREHR	00h
011Bh	Timer RE Day of Week Data Register	TREWK	00h
011Ch	Timer RE Control Register 1	TRECR1	00h
011Dh	Timer RE Control Register 2	TRECR2	00h
011Eh	Timer RE Count Source Select Register	TRECSR	00001000b
011Fh			
0120h	Timer RC Mode Register	TRCMR	01001000b
0121h	Timer RC Control Register 1	TRCCR1	00h
0122h	Timer RC Interrupt Enable Register	TRCIER	01110000b
0123h	Timer RC Status Register	TRCSR	01110000b
0124h	Timer RC I/O Control Register 0	TRCIOR0	10001000b
0125h	Timer RC I/O Control Register 1	TRCIOR1	10001000b
0126h	Timer RC Counter	TRC	00h
0127h			00h
0128h	Timer RC General Register A	TRCGRA	FFh
0129h			FFh
012Ah	Timer RC General Register B	TRCGRB	FFh
012Bh			FFh
012Ch	Timer RC General Register C	TRCGRC	FFh
012Dh			FFh
012Eh	Timer RC General Register D	TRCGRD	FFh
012Fh			FFh
0130h	Timer RC Control Register 2	TRCCR2	00011000b
0131h	Timer RC Digital Filter Function Select Register	TRCDF	00h
0132h	Timer RC Output Master Enable Register	TRCOER	01111111b
0133h	Timer RC Trigger Control Register	TRCADCR	00h
0134h			
0135h			
0136h			
0137h			
0138h			
0139h			
013Ah			
013Bh			
013Ch			
013Dh			
013Eh			
013Fh			

Note:
1.   The blank areas are reserved and cannot be accessed by users.

Table 4.7   SFR Information (7) [1]

Address	Register	Symbol	After Reset
0180h	Timer RA Pin Select Register	TRASR	00h
0181h	Timer RC Pin Select Register	TRBRCSR	00h
0182h	Timer RC Pin Select Register 0	TRCPSR0	00h
0183h	Timer RC Pin Select Register 1	TRCPSR1	00h
0184h			
0185h			
0186h			
0187h			
0188h	UART0 Pin Select Register	U0SR	00h
0189h			
018Ah	UART2 Pin Select Register 0	U2SR0	00h
018Bh	UART2 Pin Select Register 1	U2SR1	00h
018Ch	SSU / IIC Pin Select Register	SSUIICSR	00h
018Dh			
018Eh	INT Interrupt Input Pin Select Register	INTSR	00h
018Fh	I/O Function Pin Select Register	PINSR	00h
0190h			
0191h			
0192h			
0193h	SS Bit Counter Register	SSBR	11111000b
0194h	SS Transmit Data Register L / IIC bus Transmit Data Register [2]	SSTDR / ICDRT	FFh
0195h	SS Transmit Data Register H [2]	SSTDRH	FFh
0196h	SS Receive Data Register L / IIC bus Receive Data Register [2]	SSRDR / ICDRR	FFh
0197h	SS Receive Data Register H [2]	SSRDRH	FFh
0198h	SS Control Register H / IIC bus Control Register 1 [2]	SSCRH / ICCR1	00h
0199h	SS Control Register L / IIC bus Control Register 2 [2]	SSCRL / ICCR2	01111101b
019Ah	SS Mode Register / IIC bus Mode Register [2]	SSMR / ICMR	00010000b / 00011000b
019Bh	SS Enable Register / IIC bus Interrupt Enable Register [2]	SSER / ICIER	00h
019Ch	SS Status Register / IIC bus Status Register [2]	SSSR / ICSR	00h / 0000X000b
019Dh	SS Mode Register 2 / Slave Address Register [2]	SSMR2 / SAR	00h
019Eh			
019Fh			
01A0h			
01A1h			
01A2h			
01A3h			
01A4h			
01A5h			
01A6h			
01A7h			
01A8h			
01A9h			
01AAh			
01ABh			
01ACh			
01ADh			
01AEh			
01AFh			
01B0h			
01B1h			
01B2h	Flash Memory Status Register	FST	10000X00b
01B3h			
01B4h	Flash Memory Control Register 0	FMR0	00h
01B5h	Flash Memory Control Register 1	FMR1	00h
01B6h	Flash Memory Control Register 2	FMR2	00h
01B7h			
01B8h			
01B9h			
01BAh			
01BBh			
01BCh			
01BDh			
01BEh			
01BFh			

X: Undefined
Notes:
1. The blank areas are reserved and cannot be accessed by users.
2. Selectable by the IICSEL bit in the SSUIICSR register.
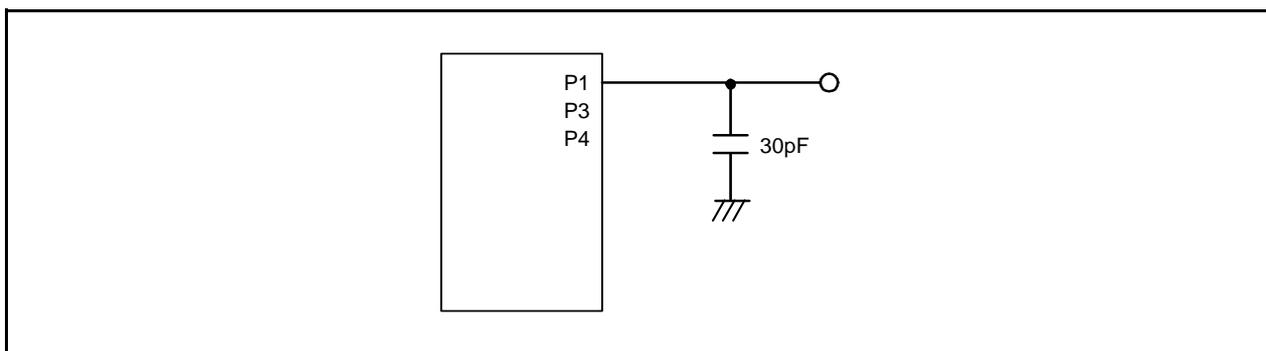
Figure 5.1   Ports P1, P3, P4 Timing Measurement Circuit

Table 5.3   A/D Converter Characteristics

Symbol	Parameter		Conditions		Standard			Unit
					Min.	Typ.	Max.	
−	Resolution		V_{ref} = AV_{CC}		−	−	10	Bit
−	Absolute accuracy	10-bit mode	V_{ref} = AV_{CC} = 5.0 V	AN8 to AN11 input	−	−	±3	LSB
			V_{ref} = AV_{CC} = 3.3 V	AN8 to AN11 input	−	−	±5	LSB
			V_{ref} = AV_{CC} = 3.0 V	AN8 to AN11 input	−	−	±5	LSB
			V_{ref} = AV_{CC} = 2.2 V	AN8 to AN11 input	−	−	±5	LSB
		8-bit mode	V_{ref} = AV_{CC} = 5.0 V	AN8 to AN11 input	−	−	±2	LSB
			V_{ref} = AV_{CC} = 3.3 V	AN8 to AN11 input	−	−	±2	LSB
			V_{ref} = AV_{CC} = 3.0 V	AN8 to AN11 input	−	−	±2	LSB
			V_{ref} = AV_{CC} = 2.2 V	AN8 to AN11 input	−	−	±2	LSB
ϕAD	A/D conversion clock		4.0 V ≤ V_{ref} = AV_{CC} ≤ 5.5 V [2]		2	−	20	MHz
			3.2 V ≤ V_{ref} = AV_{CC} ≤ 5.5 V [2]		2	−	16	MHz
			2.7 V ≤ V_{ref} = AV_{CC} ≤ 5.5 V [2]		2	−	10	MHz
			2.2 V ≤ V_{ref} = AV_{CC} ≤ 5.5 V [2]		2	−	5	MHz
−	Tolerance level impedance				−	3	−	kΩ
t_{CONV}	Conversion time	10-bit mode	V_{ref} = AV_{CC} = 5.0 V, ϕAD = 20 MHz		2.2	−	−	µs
		8-bit mode	V_{ref} = AV_{CC} = 5.0 V, ϕAD = 20 MHz		2.2	−	−	µs
t_{SAMP}	Sampling time		ϕAD = 20 MHz		0.8	−	−	µs
IV_{ref}	V_{ref} current		V_{CC} = 5 V, XIN = f1 = ϕAD = 20 MHz		−	45	−	µA
V_{ref}	Reference voltage				2.2	−	AV_{CC}	V
V_{IA}	Analog input voltage [3]				0	−	V_{ref}	V
OCVREF	On-chip reference voltage		2 MHz ≤ ϕAD ≤ 4 MHz		1.19	1.34	1.49	V

Notes:
1. V_{CC}/AV_{CC} = V_{ref} = 2.2 to 5.5 V, V_{SS} = 0 V and T_{opr} = −20 to 85°C (N version) / −40 to 85°C (D version), unless otherwise specified.
2. The A/D conversion result will be undefined in wait mode, stop mode, when the flash memory stops, and in low-current-consumption mode. Do not perform A/D conversion in these states or transition to these states during A/D conversion.
3. When the analog input voltage is over the reference voltage, the A/D conversion result will be 3FFh in 10-bit mode and FFh in 8-bit mode.

Table 5.6   Flash Memory (Program ROM) Electrical Characteristics

Symbol	Parameter	Conditions	Standard Min.	Standard Typ.	Standard Max.	Unit
–	Program/erase endurance [2]		1,000 [3]	–	–	times
–	Byte program time		–	80	500	μs
–	Block erase time		–	0.3	–	s
$t_{d(SR-SUS)}$	Time delay from suspend request until suspend		–	–	5 + CPU clock × 3 cycles	ms
–	Interval from erase start/restart until following suspend request		0	–	–	μs
–	Time from suspend until erase restart		–	–	30+CPU clock × 1 cycle	μs
$t_{d(CMDRST-READY)}$	Time from when command is forcibly terminated until reading is enabled		–	–	30+CPU clock × 1 cycle	μs
–	Program, erase voltage		2.7	–	5.5	V
–	Read voltage		1.8	–	5.5	V
–	Program, erase temperature		0	–	60	°C
–	Data hold time [7]	Ambient temperature = 55°C	20	–	–	year

Notes:
1. V_{CC} = 2.7 to 5.5 V and T_{opr} = 0 to 60°C, unless otherwise specified.
2. Definition of programming/erasure endurance
    The programming and erasure endurance is defined on a per-block basis.
    If the programming and erasure endurance is n (n = 1,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
    However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
4. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
5. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
7. The data hold time includes time that the power supply is off or the clock is not supplied.

Table 5.7   Flash Memory (Data flash Block A to Block D) Electrical Characteristics

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
−	Program/erase endurance [2]		10,000 [3]	−	−	times
−	Byte program time (program/erase endurance ≤ 1,000 times)		−	160	1,500	μs
−	Byte program time (program/erase endurance > 1,000 times)		−	300	1,500	μs
−	Block erase time (program/erase endurance ≤ 1,000 times)		−	0.2	1	s
−	Block erase time (program/erase endurance > 1,000 times)		−	0.3	1	s
$t_{d(SR-SUS)}$	Time delay from suspend request until suspend		−	−	5 + CPU clock × 3 cycles	ms
−	Interval from erase start/restart until following suspend request		0	−	−	μs
−	Time from suspend until erase restart		−	−	30+CPU clock × 1 cycle	μs
$t_{d(CMDRST-READY)}$	Time from when command is forcibly terminated until reading is enabled		−	−	30+CPU clock × 1 cycle	μs
−	Program, erase voltage		2.7	−	5.5	V
−	Read voltage		1.8	−	5.5	V
−	Program, erase temperature		−20 [7]	−	85	°C
−	Data hold time [8]	Ambient temperature = 55 °C	20	−	−	year

Notes:
1. V_{CC} = 2.7 to 5.5 V and T_{opr} = −20 to 85°C (N version) / −40 to 85°C (D version), unless otherwise specified.
2. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
   However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
4. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. In addition, averaging the erasure endurance between blocks A to D can further reduce the actual erasure endurance. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
5. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
7. −40°C for D version.
8. The data hold time includes time that the power supply is off or the clock is not supplied.
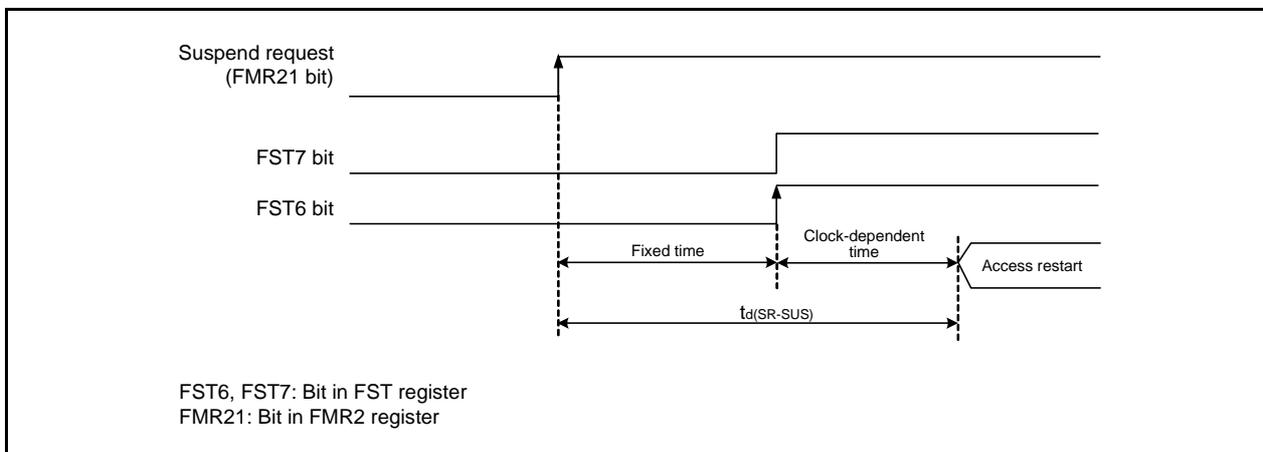
Figure 5.2   Time delay until Suspend

Table 5.8   Voltage Detection 0 Circuit Electrical Characteristics

| Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det0}	Voltage detection level Vdet0_0 [2]		1.80	1.90	2.05	V
	Voltage detection level Vdet0_1 [2]		2.15	2.35	2.50	V
	Voltage detection level Vdet0_2 [2]		2.70	2.85	3.05	V
	Voltage detection level Vdet0_3 [2]		3.55	3.80	4.05	V
−	Voltage detection 0 circuit response time [4]	At the falling of Vcc from 5 V to (Vdet0_0 − 0.1) V	−	6	150	μs
−	Voltage detection circuit self power consumption	VCA25 = 1, Vcc = 5.0 V	−	1.5	−	μA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts [3]		−	−	100	μs

Notes:
1. The measurement condition is Vcc = 1.8 V to 5.5 V and Topr = −20 to 85°C (N version) / −40 to 85°C (D version).
2. Select the voltage detection level with bits VDSEL0 and VDSEL1 in the OFS register.
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA25 bit in the VCA2 register to 0.
4. Time until the voltage monitor 0 reset is generated after the voltage passes Vdet0.

Table 5.9   Voltage Detection 1 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det1}	Voltage detection level Vdet1_0 [2]	At the falling of Vcc	2.00	2.20	2.40	V
	Voltage detection level Vdet1_1 [2]	At the falling of Vcc	2.15	2.35	2.55	V
	Voltage detection level Vdet1_2 [2]	At the falling of Vcc	2.30	2.50	2.70	V
	Voltage detection level Vdet1_3 [2]	At the falling of Vcc	2.45	2.65	2.85	V
	Voltage detection level Vdet1_4 [2]	At the falling of Vcc	2.60	2.80	3.00	V
	Voltage detection level Vdet1_5 [2]	At the falling of Vcc	2.75	2.95	3.15	V
	Voltage detection level Vdet1_6 [2]	At the falling of Vcc	2.85	3.10	3.40	V
	Voltage detection level Vdet1_7 [2]	At the falling of Vcc	3.00	3.25	3.55	V
	Voltage detection level Vdet1_8 [2]	At the falling of Vcc	3.15	3.40	3.70	V
	Voltage detection level Vdet1_9 [2]	At the falling of Vcc	3.30	3.55	3.85	V
	Voltage detection level Vdet1_A [2]	At the falling of Vcc	3.45	3.70	4.00	V
	Voltage detection level Vdet1_B [2]	At the falling of Vcc	3.60	3.85	4.15	V
	Voltage detection level Vdet1_C [2]	At the falling of Vcc	3.75	4.00	4.30	V
	Voltage detection level Vdet1_D [2]	At the falling of Vcc	3.90	4.15	4.45	V
	Voltage detection level Vdet1_E [2]	At the falling of Vcc	4.05	4.30	4.60	V
	Voltage detection level Vdet1_F [2]	At the falling of Vcc	4.20	4.45	4.75	V
−	Hysteresis width at the rising of Vcc in voltage detection 1 circuit	Vdet1_0 to Vdet1_5 selected	−	0.07	−	V
		Vdet1_6 to Vdet1_F selected	−	0.10	−	V
−	Voltage detection 1 circuit response time [3]	At the falling of Vcc from 5 V to (Vdet1_0 − 0.1) V	−	60	150	μs
−	Voltage detection circuit self power consumption	VCA26 = 1, Vcc = 5.0 V	−	1.7	−	μA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts [4]		−	−	100	μs

Notes:
1. The measurement condition is Vcc = 1.8 V to 5.5 V and Topr = −20 to 85°C (N version) / −40 to 85°C (D version).
2. Select the voltage detection level with bits VD1S0 to VD1S3 in the VD1LS register.
3. Time until the voltage monitor 1 interrupt request is generated after the voltage passes Vdet1.
4. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.

Table 5.10   Voltage Detection 2 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det2}	Voltage detection level Vdet2_0 [2]	At the falling of V_{CC}	3.70	4.00	4.30	V
	Voltage detection level Vdet2_EXT [2]	At the falling of LVCMP2	1.20	1.34	1.48	V
–	Hysteresis width at the rising of Vcc in voltage detection 2 circuit		–	0.10	–	V
–	Voltage detection 2 circuit response time [3]	At the falling of Vcc from 5 V to (Vdet2_0 − 0.1) V	–	20	150	μs
–	Voltage detection circuit self power consumption	VCA27 = 1, Vcc = 5.0 V	–	1.7	–	μA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts [4]		–	–	100	μs

Notes:
  1. The measurement condition is V_{CC} = 1.8 V to 5.5 V and T_{opr} = −20 to 85°C (N version) / −40 to 85°C (D version).
  2. The voltage detection level varies with detection targets. Select the level with the VCA24 bit in the VCA2 register.
  3. Time until the voltage monitor 2 interrupt request is generated after the voltage passes V_{det2}.
  4. Necessary time until the voltage detection circuit operates after setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.

Table 5.11   Power-on Reset Circuit [2]

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
t_{rth}	External power V_{CC} rise gradient	[1]	0	–	50,000	mV/ms

Notes:
  1. The measurement condition is T_{opr} = −20 to 85°C (N version) / −40 to 85°C (D version), unless otherwise specified.
  2. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS register to 0.

Notes:
  1. V_{det0} indicates the voltage detection level of the voltage detection 0 circuit. Refer to **6. Voltage Detection Circuit** of User's Manual: Hardware for details.
  2. $t_{w(por)}$ indicates the duration the external power V_{CC} must be held below the valid voltage (0.5 V) to enable a power-on reset. When turning on the power after it falls with voltage monitor 0 reset disabled, maintain $t_{w(por)}$ for 1 ms or more.

Figure 5.3   Power-on Reset Circuit Electrical Characteristics
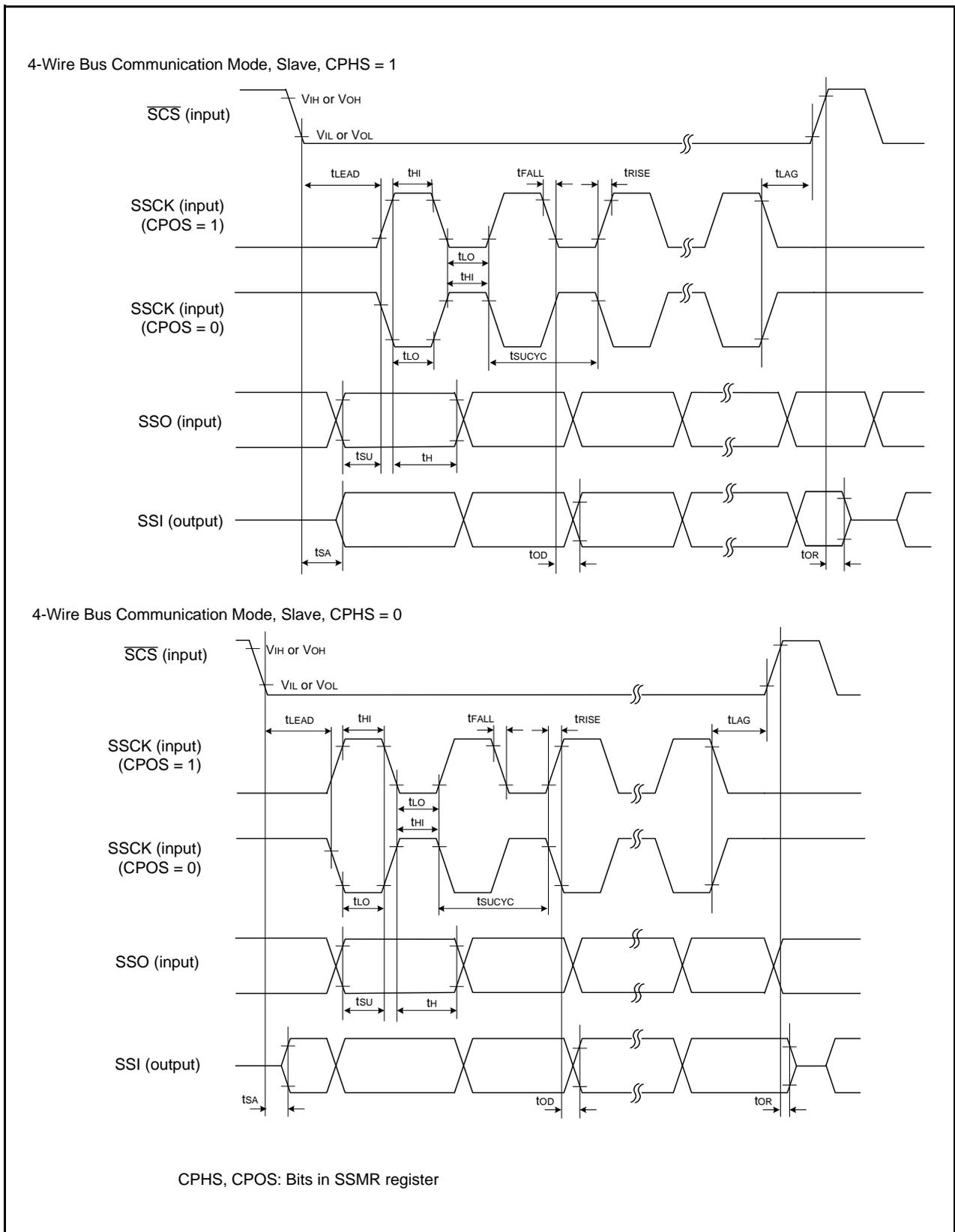
Figure 5.5   I/O Timing of Synchronous Serial Communication Unit (SSU) (Slave)
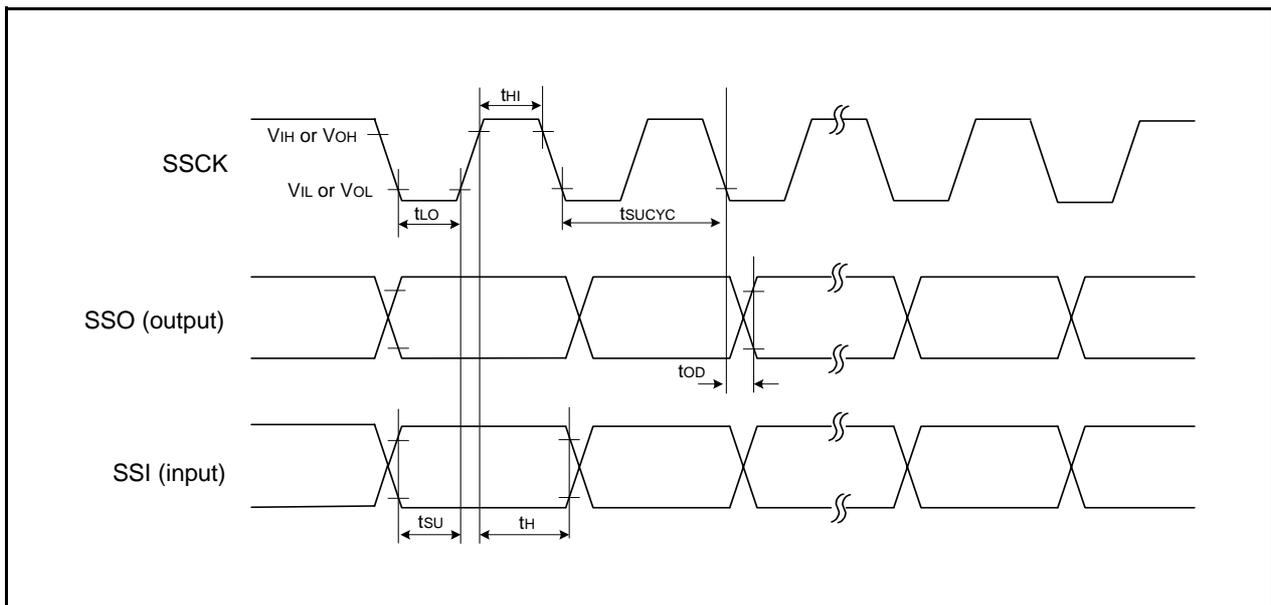
Figure 5.6   I/O Timing of Synchronous Serial Communication Unit (SSU) (Clock Synchronous Communication Mode)

Table 5.17   Electrical Characteristics (1) [4.2 V ≤ Vcc ≤ 5.5 V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
VOH	Output "H" voltage	Other than XOUT	Drive capacity High Vcc = 5 V	IOH = −20 mA	Vcc − 2.0	–	Vcc	V
			Drive capacity Low Vcc = 5 V	IOH = −5 mA	Vcc − 2.0	–	Vcc	V
		XOUT	Vcc = 5 V	IOH = −200 μA	1.0	–	Vcc	V
VOL	Output "L" voltage	Other than XOUT	Drive capacity High Vcc = 5 V	IOL = 20 mA	–	–	2.0	V
			Drive capacity Low Vcc = 5 V	IOL = 5 mA	–	–	2.0	V
		XOUT	Vcc = 5 V	IOL = 200 μA	–	–	0.5	V
VT+-VT-	Hysteresis	INT0, INT1, INT3, KI0, KI1, KI2, KI3, TRAIO, TRCIOA, TRCIOB, TRCIOC, TRCIOD, TRCTRG, TRCCLK, ADTRG, RXD0, RXD2, CLK0, CLK2, SSI, SCL, SDA, SSO	Vcc = 5.0 V		0.1	1.2	–	V
		RESET	Vcc = 5.0 V		0.1	1.2	–	V
IIH	Input "H" current		VI = 5 V, Vcc = 5.0 V		–	–	5.0	μA
IIL	Input "L" current		VI = 0 V, Vcc = 5.0 V		–	–	−5.0	μA
RPULLUP	Pull-up resistance		VI = 0 V, Vcc = 5.0 V		25	50	100	kΩ
RfXIN	Feedback resistance	XIN			–	0.3	–	MΩ
RfXCIN	Feedback resistance	XCIN			–	8	–	MΩ
VRAM	RAM hold voltage		During stop mode		1.8	–	–	V

Note:
1.   4.2 V ≤ Vcc ≤ 5.5 V and Topr = −20 to 85°C (N version) / −40 to 85°C (D version), f(XIN) = 20 MHz, unless otherwise specified.

Timing Requirements
(Unless Otherwise Specified: Vcc = 5 V, Vss = 0 V at Topr = 25°C)

Table 5.19   External Clock Input (XOUT, XCIN)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{C(XOUT)}$	XOUT input cycle time	50	–	ns
$t_{WH(XOUT)}$	XOUT input "H" width	24	–	ns
$t_{WL(XOUT)}$	XOUT input "L" width	24	–	ns
$t_{C(XCIN)}$	XCIN input cycle time	14	–	μs
$t_{WH(XCIN)}$	XCIN input "H" width	7	–	μs
$t_{WL(XCIN)}$	XCIN input "L" width	7	–	μs
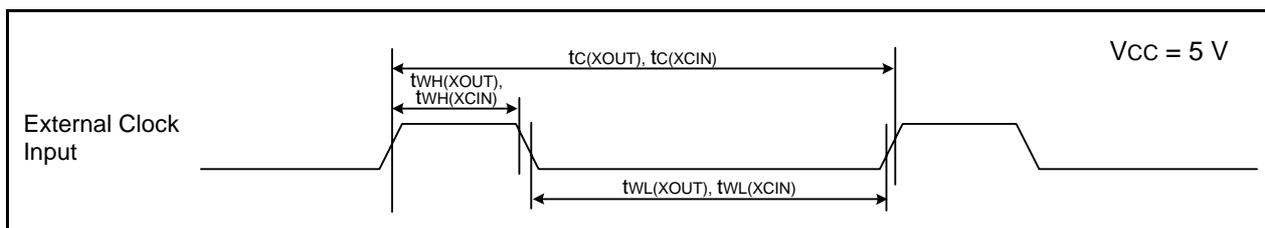
Figure 5.8   External Clock Input Timing Diagram when Vcc = 5 V

Table 5.20   TRAIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{C(TRAIO)}$	TRAIO input cycle time	100	–	ns
$t_{WH(TRAIO)}$	TRAIO input "H" width	40	–	ns
$t_{WL(TRAIO)}$	TRAIO input "L" width	40	–	ns
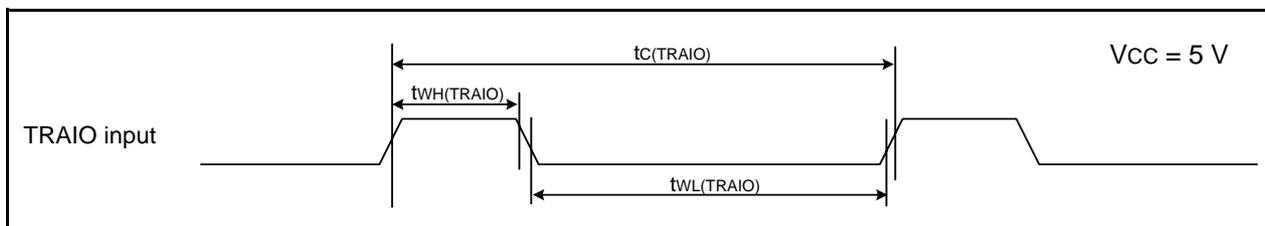
Figure 5.9   TRAIO Input Timing Diagram when Vcc = 5 V

Table 5.21   Serial Interface

Symbol	Parameter		Standard		Unit
			Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	When external clock is selected	200	–	ns
$t_{W(CKH)}$	CLKi input "H" width		100	–	ns
$t_{W(CKL)}$	CLKi input "L" width		100	–	ns
$t_{d(C-Q)}$	TXDi output delay time		–	90	ns
$t_{h(C-Q)}$	TXDi hold time		0	–	ns
$t_{su(D-C)}$	RXDi input setup time		10	–	ns
$t_{h(C-D)}$	RXDi input hold time		90	–	ns
$t_{d(C-Q)}$	TXDi output delay time	When internal clock is selected	–	10	ns
$t_{su(D-C)}$	RXDi input setup time		90	–	ns
$t_{h(C-D)}$	RXDi input hold time		90	–	ns

i = 0, 2
Note:
  1. Vcc = 5 V and Topr = −20 to 85 °C (N version)/−40 to 85 °C (D version), unless otherwise specified.
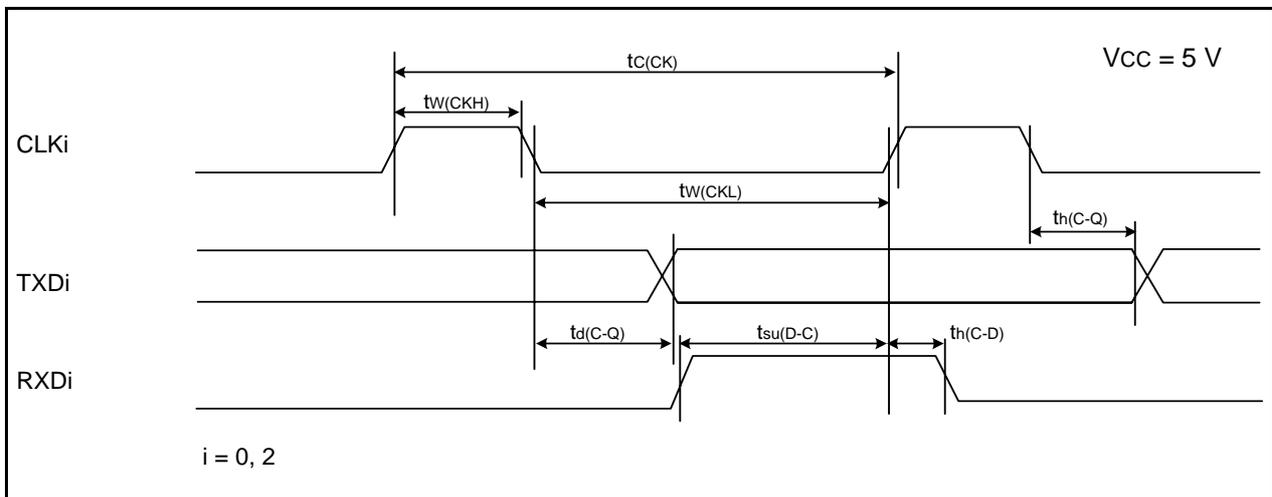
Figure 5.10   Serial Interface Timing Diagram when VCC = 5 V

Table 5.22   External Interrupt $\overline{INT}i$ (i = 0, 1, 3) Input, Key Input Interrupt $\overline{KI}i$ (i = 0 to 3)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INT}i$ input "H" width, $\overline{KI}i$ input "H" width	250 [1]	–	ns
$t_{W(INL)}$	$\overline{INT}i$ input "L" width, $\overline{KI}i$ input "L" width	250 [2]	–	ns

Notes:
  1. When selecting the digital filter by the $\overline{INT}i$ input filter select bit, use an $\overline{INT}i$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
  2. When selecting the digital filter by the $\overline{INT}i$ input filter select bit, use an $\overline{INT}i$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
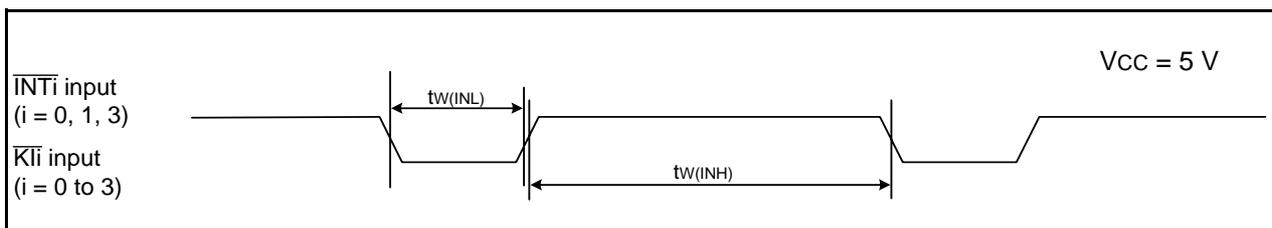
Figure 5.11   Input Timing Diagram for External Interrupt INTi and Key Input Interrupt KIi when Vcc = 5 V

Table 5.24   Electrical Characteristics (4) [2.7 V ≤ Vcc < 3.3 V]
(T$_{opr}$ = −20 to 85°C (N version) / −40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
I$_{CC}$	Power supply current (V$_{CC}$ = 2.7 to 3.3 V) Single-chip mode, output pins are open, other pins are V$_{SS}$	High-speed clock mode	XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	−	3.5	10	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	−	1.5	7.5	mA
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz No division	−	7.0	15	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	−	3.0	−	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 10 MHz Low-speed on-chip oscillator on = 125 kHz No division	−	4.0	−	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 10 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	−	1.5	−	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 4 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-16 MSTIIC = MSTTRD = MSTTRC = 1	−	1	−	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR27 = 1, VCA20 = 0	−	90	390	μA
		Low-speed clock mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz No division FMR27 = 1, VCA20 = 0	−	80	400	μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz No division Program operation on RAM Flash memory off, FMSTP = 1, VCA20 = 0	−	40	−	μA
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	−	15	90	μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	−	4	80	μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (peripheral clock off) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	−	3.5	−	μA
		Stop mode	XIN clock off, T$_{opr}$ = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	−	2.0	5.0	μA
			XIN clock off, T$_{opr}$ = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	−	5.0	−	μA

Package Dimensions

Diagrams showing the latest package dimensions and mounting information are available in the "Packages" section of the Renesas Electronics website.

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LSSOP20-4.4x6.5-0.65	PLSP0020JB-A	20P2F-A	0.1g

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Detail F

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.4	6.5	6.6
E	4.3	4.4	4.5
A_2	—	1.15	—
A	—	—	1.45
A_1	0	0.1	0.2
b_p	0.17	0.22	0.32
c	0.13	0.15	0.2
θ	0°	—	10°
H_E	6.2	6.4	6.6
e	0.53	0.65	0.77
y	—	—	0.10
L	0.3	0.5	0.7

RENESAS

Renesas Electronics Corporation

http://www.renesas.com

SALES OFFICES

Refer to "http://www.renesas.com/" for the latest and detailed information.

Renesas Electronics America Inc.
2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-65030, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China
Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 / -7898

Renesas Electronics Hong Kong Limited
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2886-9318, Fax: +852 2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
1 harbourFront Avenue, #06-10, keppel Bay Tower, Singapore 098632
Tel: +65-6213-0200, Fax: +65-6278-8001

Renesas Electronics Malaysia Sdn.Bhd.
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics Korea Co., Ltd.
11F., Samik Lavied' or Bldg., 720-2 Yeoksam-Dong, Kangnam-Ku, Seoul 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141