



Welcome to **E-XFL.COM** 

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded - Microcontrollers</u>"

Details	
Product Status	Active
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I <sup>2</sup> C, LINbus, SIO, SSU, UART/USART
Peripherals	POR, PWM, Voltage Detect, WDT
Number of I/O	15
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	1.5K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-LSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-LSSOP
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f21324mdsp-u0

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

R8C/32M Group 1. Overview

Specifications for R8C/32M Group (2) Table 1.2

Item	Function	Specification			
Serial	UART0	Clock synchronous serial I/O/UART			
Interface	UART2	Clock synchronous serial I/O/UART, I <sup>2</sup> C mode (I <sup>2</sup> C-bus), multiprocessor communication function			
Synchronous S	Serial	1 (shared with I <sup>2</sup> C-bus)			
Communication	n Unit (SSU)				
I <sup>2</sup> C bus		1 (shared with SSU)			
LIN Module		Hardware LIN: 1 (timer RA, UART0)			
A/D Converter		10-bit resolution × 4 channels, includes sample and hold function, with sweep mode			
Comparator A		2 circuits (shared with voltage monitor 1 and voltage monitor 2)			
		External reference voltage input available			
Comparator B		2 circuits			
Flash Memory		• Programming and erasure voltage: VCC = 2.7 to 5.5 V			
		Programming and erasure endurance: 10,000 times (data flash)			
		1,000 times (program ROM)			
		Program security: ROM code protect, ID code check			
		Debug functions: On-chip debug, on-board flash rewrite function			
		Background operation (BGO) function			
Operating Fred Voltage	luency/Supply	f(XIN) = 20 MHz (VCC = 2.7 to 5.5 V) f(XIN) = 5 MHz (VCC = 1.8 to 5.5 V)			
Current consumption		Typ. 6.5 mA (VCC = 5.0 V, f(XIN) = 20 MHz) Typ. 3.5 mA (VCC = 3.0 V, f(XIN) = 10 MHz) Typ. 3.5 μA (VCC = 3.0 V, wait mode (f(XCIN) = 32 kHz)) Typ. 2.0 μA (VCC = 3.0 V, stop mode)			
Operating Amb	ient Temperature	-20 to 85°C (N version) -40 to 85°C (D version) (1)			
Package		20-pin LSSOP			
		Package code: PLSP0020JB-A (previous code: 20P2F-A)			

Note:
 1. Specify the D version if D version functions are to be used.

R8C/32M Group 1. Overview

Table 1.4 Pin Name Information by Pin Number

				I/O Pin Functions for Peripheral Modules				
Pin Number	Control Pin	Port	Interrupt	Timer	Serial Interface	SSU	I <sup>2</sup> C bus	A/D Converter, Comparator A, Comparator B
1		P4_2						VREF
2	MODE							
3	RESET							
4	XOUT(/XCOUT)	P4_7						
5	VSS/AVSS							
6	XIN(/XCIN)	P4_6						
7	VCC/AVCC							
8		P3_7		TRAO	(RXD2/SCL2/ TXD2/SDA2)	SSO	SDA	
9		P3_5		(TRCIOD)	(CLK2)	SSCK	SCL	
10		P3_4		(TRCIOC)	(RXD2/SCL2/ TXD2/SDA2)	SSI		IVREF3
11		P3_3	ĪNT3	(TRCCLK)	(CTS2/RTS2)	SCS		IVCMP3
12		P4_5	ĪNT0		(RXD2/SCL2)			ADTRG
13		P1_7	ĪNT1	(TRAIO)				IVCMP1
14		P1_6			(CLK0)			LVCOUT2/IVREF1
15		P1_5	(INT1)	(TRAIO)	(RXD0)			
16		P1_4		(TRCCLK)	(TXD0)			
17		P1_3	KI3	TRBO (/TRCIOC)				AN11/LVCOUT1
18		P1_2	KI2	(TRCIOB)				AN10/LVREF
19		P1_1	KI1	(TRCIOA/ TRCTRG)				AN9/LVCMP2
20		P1_0	KI0	(TRCIOD)				AN8/LVCMP1

# Note:

1. Can be assigned to the pin in parentheses by a program.

R8C/32M Group 1. Overview

Table 1.6 Pin Functions (2)

Item	Pin Name	I/O Type	Description
Reference voltage input	VREF	I	Reference voltage input pin to A/D converter
A/D converter	AN8 to AN11	I	Analog input pins to A/D converter
	ADTRG	I	A/D external trigger input pin
Comparator A	LVCMP1, LVCMP2	I	Comparator A analog voltage input pins
	LVREF	- 1	Comparator A reference voltage input pin
	LVCOUT1, LVCOUT2	0	Comparator A output pins
Comparator B	IVCMP1, IVCMP3	- 1	Comparator B analog voltage input pins
	IVREF1, IVREF3	1	Comparator B reference voltage input pins
I/O port	P1_0 to P1_7, P3_3 to P3_5, P3_7, P4_5 to P4_7	I/O	CMOS I/O ports. Each port has an I/O select direction register, allowing each pin in the port to be directed for input or output individually.  Any port set to input can be set to use a pull-up resistor or not by a program.  All ports can be used as LED drive ports.
Input port	P4_2	I	Input-only port

I: Input

O: Output

I/O: Input and output

R8C/32M Group 3. Memory

# 3. Memory

# 3.1 R8C/32M Group

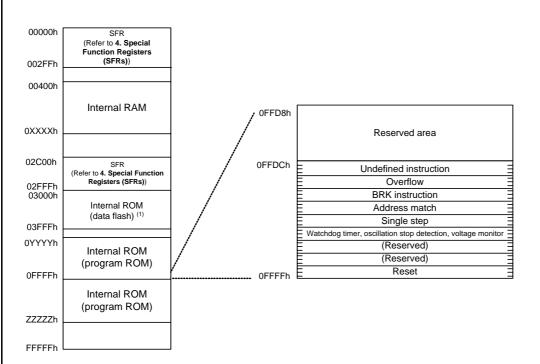
Figure 3.1 is a Memory Map of R8C/32M Group. The R8C/32M Group has a 1-Mbyte address space from addresses 00000h to FFFFFh. For example, a 16-Kbyte internal ROM area is allocated addresses 0C000h to 0FFFFh.

The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. The starting address of each interrupt routine is stored here.

The internal ROM (data flash) is allocated addresses 03000h to 03FFFh.

The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 1.5-Kbyte internal RAM area is allocated addresses 00400h to 009FFh. The internal RAM is used not only for data storage but also as a stack area when a subroutine is called or when an interrupt request is acknowledged.

Special function registers (SFRs) are allocated addresses 00000h to 002FFh and 02C00h to 02FFFh. Peripheral function control registers are allocated here. All unallocated spaces within the SFRs are reserved and cannot be accessed by users.



- 1. Data flash indicates block A (1 Kbyte), block B (1 Kbyte), block C (1 Kbyte), and block D (1 Kbyte).
- 2. The blank areas are reserved and cannot be accessed by users.

Dord November		Internal ROM	Internal RAM		
Part Number	Size	Address 0YYYYh	Address ZZZZZh	Size	Address 0XXXXh
R5F21321MNFP, R5F21321MDFP	4 Kbytes	0F000h	_	512 bytes	005FFh
R5F21322MNFP, R5F21322MDFP	8 Kbytes	0E000h	_	1 Kbyte	007FFh
R5F21324MNFP, R5F21324MDFP	16 Kbytes	0C000h	_	1.5 Kbytes	009FFh

Figure 3.1 Memory Map of R8C/32M Group

SFR Information (2) (1) Table 4.2

Address	Register	Symbol	After Reset
003Ah	Voltage Monitor 2 Circuit Control Register	VW2C	10000010b
003Bh			
003Ch			
003Dh			
003Eh			
003Eh			
003111 0040h			
	Floor Mamony Doody Interview Control Dogistor	EMPDYIC	VVVVV000h
0041h	Flash Memory Ready Interrupt Control Register	FMRDYIC	XXXXX000b
0042h			
0043h			
0044h			
0045h			
0046h			
0047h	Timer RC Interrupt Control Register	TRCIC	XXXXX000b
0048h			
0049h			
004Ah	Timer RE Interrupt Control Register	TREIC	XXXXX000b
004Bh	UART2 Transmit Interrupt Control Register	S2TIC	XXXXX000b
004Dh	UART2 Receive Interrupt Control Register	S2RIC	XXXXX000b XXXXXX000b
004CH	Key Input Interrupt Control Register	KUPIC	XXXXX000b XXXXXX000b
	Rey input interrupt Control Register		
004Eh	A/D Conversion Interrupt Control Register	ADIC	XXXXX000b
004Fh	SSU Interrupt Control Register / IIC bus Interrupt Control Register (2)	SSUIC / IICIC	XXXXX000b
0050h			
0051h	UART0 Transmit Interrupt Control Register	SOTIC	XXXXX000b
0052h	UARTO Receive Interrupt Control Register	SORIC	XXXXX000b
0053h	·		
0054h			
0055h			
0056h	Timer RA Interrupt Control Register	TRAIC	XXXXX000b
	Timer KA mierrupi Comitor Kegister	TRAIC	^^^^0000
0057h	T PRI C C C C C C C C C C C C C C C C C C C	T0010	200000000
0058h	Timer RB Interrupt Control Register	TRBIC	XXXXX000b
0059h	INT1 Interrupt Control Register	INT1IC	XX00X000b
005Ah	INT3 Interrupt Control Register	INT3IC	XX00X000b
005Bh			
005Ch			
005Dh	INT0 Interrupt Control Register	INT0IC	XX00X000b
005Eh	UART2 Bus Collision Detection Interrupt Control Register	U2BCNIC	XXXXX000b
005Fh	O THE TEN DE COMMON DE COMMON TRAPE CONTROL TO GROCE	02200	7.0.0.0.0.0002
0060h			
0061h			
0062h			
0063h			
0064h			
0065h			
0066h			
0067h			
0068h			
0069h			
006Ah			
006An			
006Ch			
006Dh			
006Eh			
006Fh			
0070h			
0071h			
0072h	Voltage Monitor 1 / Comparator A1 Interrupt Control Register	VCMP1IC	XXXXX000b
0073h	Voltage Monitor 2 / Comparator A2 Interrupt Control Register	VCMP2IC	XXXXX000b
0074h			
0074H			
0076h			
0077h			
0078h			
0079h			
007Ah			
007Bh			
007Ch			
007Ch			
007Eh 007Fh			
	1	1	i

Notes: 1. 2.

- The blank areas are reserved and cannot be accessed by users. Selectable by the IICSEL bit in the SSUIICSR register.

SFR Information (3) (1) Table 4.3

Address	Register	Symbol	After Reset
0080h	DTC Activation Control Register	DTCTL	00h
0081h	DTC Activation Control Register	DIGIE	0011
0081h			
0083h			
0084h			
0085h			
0086h			
0087h			
0088h	DTC Activation Enable Register 0	DTCEN0	00h
0089h	DTC Activation Enable Register 1	DTCEN1	00h
008Ah	DTC Activation Enable Register 2	DTCEN2	00h
008Bh	DTC Activation Enable Register 3	DTCEN3	00h
008Ch	2 TO THOMPSHIP THOUSE THOUSENESS	2.02.10	
008Dh	DTC Activation Enable Register 5	DTCEN5	00h
008Eh	DTC Activation Enable Register 6	DTCEN6	00h
	DTC Activation Enable Register 6	DICENO	0011
008Fh			
0090h			
0091h			
0092h			
0093h			
0094h			
0095h			
0096h			
0097h			
0098h			
0099h			
009Ah			
009Bh			
009Ch			
009Dh			
009Eh			
009Fh			
00A0h	UART0 Transmit / Receive Mode Register	U0MR	00h
00A1h	UART0 Bit Rate Register	U0BRG	XXh
00A2h	UART0 Transmit Buffer Register	U0TB	XXh
00A3h	1		XXh
00A4h	UART0 Transmit / Receive Control Register 0	U0C0	00001000b
00A5h	UART0 Transmit / Receive Control Register 1	U0C1	00000010b
00A6h	UART0 Receive Buffer Register	UORB	XXh
00A0H	OAKTO Receive Bullet Register	OOKB	XXh
	HARTOT SIAR SALE	LIONAD	
00A8h	UART2 Transmit / Receive Mode Register	U2MR	00h
00A9h	UART2 Bit Rate Register	U2BRG	XXh
00AAh	UART2 Transmit Buffer Register	U2TB	XXh
00ABh			XXh
00ACh	UART2 Transmit / Receive Control Register 0	U2C0	00001000b
00ADh	UART2 Transmit / Receive Control Register 1	U2C1	00000010b
00AEh	UART2 Receive Buffer Register	U2RB	XXh
00AFh	<sup>-</sup>		XXh
00B0h	UART2 Digital Filter Function Select Register	URXDF	00h
00B1h	<u> </u>		
00B2h			
00B2h			+
00B3h			+
00B4h			
00B6h			
00B7h			
00B8h			
00B9h			
00BAh			
00BBh	UART2 Special Mode Register 5	U2SMR5	00h
00BCh	UART2 Special Mode Register 4	U2SMR4	00h
00BDh	UART2 Special Mode Register 3	U2SMR3	000X0X0Xb
00BEh	I UART2 Special Mode Register 2	LU2SMR2	LX0000000b
00BEh 00BFh	UART2 Special Mode Register 2 UART2 Special Mode Register	U2SMR2 U2SMR	X0000000b X0000000b

X: Undefined
Note:

1. The blank areas are reserved and cannot be accessed by users.

SFR Information (4) (1) Table 4.4

Add   Add   Add   Register   ADD   Oxford   ADD   Oxford   Oxfor				16. 5
000000000000000000000000000000000000	Address	Register	Symbol	After Reset
000C2h         AD Register 1         0000000XXb           000C4h         AD Register 2         AD2         XXh           000C6h         AD Register 3         AD3         XXh           000C7h         AD Register 4         AD4         XXh           000C8h         AD Register 5         AD5         XXh           000C8h         AD Register 5         AD6         XXh           000C6h         AD Register 6         AD6         XXh           000C7h         AD7         XXh         000000Xb           000C6h         AD Register 7         AD7         XXh           000C7h         AD Register 7         AD7         XXh           000C7h         AD7         XXh         000000Xb           000C7h         AD7         XXh         00000Xb           0		A/D Register 0	AD0	
000000000000000000000000000000000000				000000XXb
000000000000000000000000000000000000	00C2h	A/D Register 1	AD1	XXh
000C4h         AD Register 2         AD2         XXM           000C8h         AOR Register 3         AD3         XXM           00C8h         ADR Register 4         AD4         XXM           00C8h         ADR Register 5         AD5         XXM           00CAL         ADR Register 6         AD6         XXM           00CDh         AD7         XXM         XXM           00CDh         AD7         AD7         XXM           00CDh         AD7         XXM         XXM		1 13 11		
000000Xb   00000Xb		A/D Register 2	AD2	
Mathematics		A/D Register 2	ADZ	
000Ch         AD Register 4         AD4         XXh           00C3h         AD Register 5         AD5         XXh           00C6h         AD Register 6         AD6         XXh           00CDh         AD Register 6         AD6         XXh           00CDh         AD Register 7         AD7         XXh           00CDh         AD Register 7         AD7         XXh           00C0h         AD7         XXh         0000000Xxb           00D1h         00D2h         00D0h         00D0h         00D0h           00D2h         AD Mode Register         ADMOD         00h         00D0h           00D3h         AD Input Select Register         ADMOD         00h         00D0h           00D3h         AD Input Select Register         ADMOD         00h         00D0h	00C5n			
000Cbh         A/D Register 4         AD4         XXh           00CAh         A/D Register 5         AD5         XXh           00Cbh         A/D Register 6         AD6         XXh           00CCh         A/D Register 7         AD7         XXh           00CFh         A/D Register 7         AD7         XXh           00CDh         00Ch         00Ch         0000000Xb           00Dbh         00Dh         00Ch         000000Xb           00Dbh         AD Mode Register         ADMOD         00h           00Dbh         AD Control Register 0         ADCON0         00h           00Dbh         AD Control Register 0         ADCON0         00h           00Dbh         AD Control Register 0         ADCON0         00h           00Dbh         ADCON1         00h         00b	00C6h	A/D Register 3	AD3	
000Cbh         A/D Register 4         AD4         XXh           00CAh         A/D Register 5         AD5         XXh           00Cbh         A/D Register 6         AD6         XXh           00CCh         A/D Register 7         AD7         XXh           00CFh         A/D Register 7         AD7         XXh           00CDh         00Ch         00Ch         0000000Xb           00Dbh         00Dh         00Ch         000000Xb           00Dbh         AD Mode Register         ADMOD         00h           00Dbh         AD Control Register 0         ADCON0         00h           00Dbh         AD Control Register 0         ADCON0         00h           00Dbh         AD Control Register 0         ADCON0         00h           00Dbh         ADCON1         00h         00b	00C7h			000000XXb
000000000000000000000000000000000000		A/D Register 4	AD4	
OOCAh   AID Register 5   ADS   OXX000000Xxb		7 v 2 · rogiotor ·	7.5.	
OOCCH		A/D De sister 5	ADE	
OOCCh		A/D Register 5	AD5	
00CEh         AD Register 7         AD7         XXh           00CFh         00D0h         000000Xb         000000Xb           00D0h         00D1h         00D0h         00D0h           00D2h         00D3h         00D0h         00D0h           00D5h         AD Mode Register         ADIMSEL         11000000b           00D5h         AD Control Register 0         ADCOMO         00h           00D7h         AD Control Register 1         ADCOMI         00h           00D8h         00D4h         00D0h         00D0h           00DAh         00D0h         00D0h         00D0h           00DCh         00D0h         00D0h         00D0h           00DEh         00D0h         00D0h         00D0h           00E0h         00E0h         00E0h         00E0h           00E3h         Port PI Register         P1         XXh           00E3h         Port PI Register         P1         O0           00E3h         Port PI Register         P2         XXh           00E6h         P0rt PA Register         P3         XXh           00E8h         P0rt PA Register         P3         XXh           00E8h         P0rt PA Register				
00CEh         AD Register 7         AD7         XXh           00CPh         00D0h         000000000000000000000000000000000000		A/D Register 6	AD6	XXh
00CEh         AD Register 7         AD7         XXh           00CPh         00D0h         000000000000000000000000000000000000	00CDh			000000XXb
000000000000000000000000000000000000		A/D Register 7	AD7	
00DDh         00Dth           00Dzh         00Dsh           00D3h         00Ddh           00D5h         AD Mode Register           00D5h         AD Input Select Register           00D5h         AD Control Register 0           00D6h         ADCON0           00D7h         ADCON1           00D8h         00D8h           00D4h         00D4h           00D4h         00D4h           00D4h         00D4h           00D5h         00D6h           00D6h         00D6h           00D6h         00D6h           00D6h         00D6h           00D6h         00D6h           00E7h         00E7h           00E8h         00E7h           00E8h         00E7h           00E8h         00E7h           00E8h         00E8h           00E8h         00				
00D1h         00D2h           00D2h         00D3h           00D4h         AD Mode Register           00D5h         AD Input Select Register           00D6h         AD Control Register 0           00D7h         AD Control Register 1           00D8h         AD Control Register 1           00D8h         ADCON1           00D8h         00D8h           00Eh         00D8h           00Eh         00Eh           00Eh				000000XXD
00D2h         0DD4h         AD Mode Register         ADMOD         00h           00D5h         AD Input Select Register         ADINSEL         11000000b           00D6h         AD Control Register 0         ADCON0         00h           00D7h         AD Control Register 1         ADCON1         00h           00D8h         00D8h         00h         00h           00D8h         00DAh         00DAh         00DAh           00D6h         00DCh         00DCh         00DCh           00D6h         00DCh         00DCh         00DCh           00E7h         00E9h         00E9h         00DCh           00E2h         00E3h         00Ch         00DCh           00E3h         00E3h         00Ch         00Ch           00E3h         00E3h         00Ch         00Ch           00E5h         00E6h         00Ch         00Ch           00E6h         00E7h         00FA         00Ch           00E7h         00E7h         00FA         00Ch           00E7h         00E7h         00Ch         00Ch           00E8h         00FA         00Ch         00Ch           00E8h         00Ch         00Ch         00				
00D3h         AD Mode Register         ADMOD         00h           00D5h         AD Input Select Register         ADINSEL         11000000b           00D6h         AD Control Register 0         ADCON0         00h           00D7h         A/D Control Register 1         ADCON1         00h           00D8h              00E9h              00E2h				
00D3h         AD Mode Register         ADMOD         00h           00D5h         AD Input Select Register         ADINSEL         11000000b           00D6h         AD Control Register 0         ADCON0         00h           00D7h         A/D Control Register 1         ADCON1         00h           00D8h              00E9h              00E2h				
00D4h         AD Imput Select Register         ADINSEL         11000000b           00D6h         AD Imput Select Register 0         ADCON0         00h           00D7h         AD Control Register 1         ADCON1         00h           00D8h         00D8h         00           00DAh         00DAh         00DAh           00DAh         00DCh         00DCh           00DFh         00DCh         00DCh           00DFh         00DFh         00DCh           00E1h         Port P1 Register         P1         XXh           00E2h         00E3h         00         00           00E3h         Port P2 Intection Register         PD1         00h           00E3h         Port P3 Register         P3         XXh           00E3h         Port P3 Direction Register         PD3         00h           00E8h         Port P4 Register         P4         XXh           00E8h         Port P4 Register         PA         XXh           00E8h         Port P4 Direction Register         PD4         00h           00E8h         Port P4 Direction Register         PD4         00h           00E6h         Port P5 Direction Register         PD4         00h				
ADD   ADD   Labelect Register   ADD   AD		A/D Mode Register	ADMOD	00h
ODD6h   AD Control Register 0   ADCON1   ODh				
00D7h (ODBh (		A/D Input Select Register		
00D8h         0           00DAh         0           00DBh         0           00DCh         0           00DDh         0           00DFh         0           00E0h         0           00E1h         0           00E1h         0           00E1h         0           00E1h         0           00E1h         0           00E3h         Port P1 Register           00E3h         Port P2 Direction Register           00E3h         Port P3 Register           00E6h         P0           00E7h         Port P3 Direction Register           00E8h         P01 P4 Register           00E9h         P01 P4 Register           00E9h         P01 P4 Register           00E9h         P02           00E8h         P04           00E9h         P07 P4 Register           00E9h         P08           00E9h         P09 P04           00E9h         P09 P04           00E9h         P00 P04           00E9h         P00 P04           00E9h         P00 P04           00E9h         P00 P04           00F9h				
00D9h         00DBh           00DBh         00DCh           00DDh         00DDh           00DFh         00DFh           00E1h         00E1h           00E1h         Port P1 Register           00E2h         POT P1 Direction Register           00E3h         Port P3 Register           00E6h         POT P3 Register           00E7h         Port P3 Direction Register           00E8h         Port P4 Register           00E9h         Pot P4 Register           00E9h         POT P4 Direction Register           00E8h         POT P4 Direction Register           00EBh         PD4           00Eh         O0H           00EBh         O0H           00EPh         O0H           00EPh         O0H           00EPh         O0F9h           00F3h         O0F9h           00F9h         O0F9h           00F0h         O0F9h           00FBh		A/D Control Register 1	ADCON1	00h
00D9h         00DBh           00DBh         00DCh           00DDh         00DDh           00DFh         00DFh           00E1h         00E1h           00E1h         Port P1 Register           00E2h         POT P1 Direction Register           00E3h         Port P3 Register           00E6h         POT P3 Register           00E7h         Port P3 Direction Register           00E8h         Port P4 Register           00E9h         Pot P4 Register           00E9h         POT P4 Direction Register           00E8h         POT P4 Direction Register           00EBh         PD4           00Eh         O0H           00EBh         O0H           00EPh         O0H           00EPh         O0H           00EPh         O0F9h           00F3h         O0F9h           00F9h         O0F9h           00F0h         O0F9h           00FBh	00D8h			
00DAh         00DCh           00DBh         00DCh           00DEh         00DEh           00Eh         00Eh           00E1h         Port P1 Register           00E1h         Port P1 Direction Register           00E3h         Port P1 Direction Register           00E3h         Port P3 Register           00E6h         Port P3 Direction Register           00E7h         Port P4 Direction Register           00E8h         Port P4 Register           00E8h         Port P4 Direction Register           00EAh         Port P4 Direction Register	00D9h			
00DBh         00DCh           00DDh         00DEh           00DFh         00Eh           00E1h         Port P1 Register           00E2h         Port P1 Direction Register           00E3h         Port P1 Direction Register           00E3h         Port P3 Register           00E6h         Port P3 Direction Register           00E7h         Port P4 Register           00E8h         Port P4 Register           00E8h         Port P4 Direction Register           00EAh         Port P4 Direction Register           00EDh         00EDh           00ECh         00EDh           00EBh         00F0h           00ECh         00EDh           00ECh         00EN           00F3h         00F3h           00F4h         00F6h           00F6h         00F6h           00F8h         00F8h			+	1
00DCh         00DDh           00DFh         00Eh           00E0h         00E0h           00E1h         Port P1 Register           00E2h         Port P1 Direction Register           00E3h         Port P1 Direction Register           00E5h         Port P3 Register           00E6h         Port P3 Direction Register           00E7h         Port P4 Register           00E8h         Port P4 Direction Register           00E8h         Port P4 Direction Register           00EAh         Pott P4 Direction Register           00EAh         Pott P5 Direction Register           00EAh         Pott P6 Direction Register           00EAh         Pott P7 Direction Register           00EAH         Pott P6 Direction Register           00EAH         Pott P7 Direction Register           00EAH         Pott P7 Direction Register           00EAH         Pott P7 Direction Register           00EAH         Pott P8 Direction Register           00EAH         Pott P9 Direction Register <td></td> <td></td> <td></td> <td></td>				
00DDh         00DEh           00DFh         00E0h           00E1h         Port P1 Register           00E3h         Port P1 Direction Register           00E3h         Port P2 Register           00E4h         Port P3 Register           00E6h         Port P4 Register           00E7h         Port P4 Register           00E9h         Port P4 Direction Register           00E8h         Port P4 Direction Register           00E8h         Port P5 Direction Register           00EBh         Port P6 Direction Register           00ECh         Port P7 Direction Register           00ECh         Port P8 Direction Register           00EDh         Port P9 D4           00EDh         Port P9 D4           00ECh         Port P9 D4           00ERh         Port P9 D9           0				
00DEh         00DFh           00E0h         00E1h           00E1h         Port P1 Register           00E3h         Port P1 Direction Register           00E3h         Port P3 Register           00E5h         Port P3 Register           00E7h         Port P3 Direction Register           00E8h         Port P4 Register           00E8h         Port P4 Register           00E9h         00h           00E8h         00h           00EBh         00h           00EDh         00h           00EDh         00EDh           00EDh         00EDh           00EH         00EDh           00EH         00EDh           00F1h         00F3h           00F3h         00F3h <tr< td=""><td></td><td></td><td></td><td></td></tr<>				
00DEh         00DFh           00E0h         00E1h           00E1h         Port P1 Register           00E3h         Port P1 Direction Register           00E3h         Port P3 Register           00E5h         Port P3 Register           00E7h         Port P3 Direction Register           00E8h         Port P4 Register           00E8h         Port P4 Register           00E9h         00h           00E8h         00h           00EBh         00h           00EDh         00h           00EDh         00EDh           00EDh         00EDh           00EH         00EDh           00EH         00EDh           00F1h         00F3h           00F3h         00F3h <tr< td=""><td>00DDh</td><td></td><td></td><td></td></tr<>	00DDh			
00Fh         00E0h           00E1h         Port P1 Register         P1         XXh           00E3h         Port P1 Direction Register         PD1         00h           00E3h         Port P3 Register         P3         XXh           00E6h         Port P3 Direction Register         PD3         00h           00E8h         Port P4 Register         P4         XXh           00E8h         Port P4 Direction Register         PD4         00h           00E8h         P0t P4 Direction Register         PD4         00h           00EBh         P0t P4 Direction Register         PD4         00h           00ECh         P0ECh         PD4         00h           00EDh         P0ECh         PD4         00h           00EDh         P0ECh         PD4         00h           00ECh         P0F9h         PD4         00h           00F3h         P0F9h         PD4         00h           00F6h         P0F9h         PD4         00h           00F8h         P0F9h         PD4         00h           00F8h         P0F9h         PD4         PD4         PD4           00F8h         P0F9h         PD4         PD4         PD4 </td <td>00DEh</td> <td></td> <td></td> <td></td>	00DEh			
00E0h         Port P1 Register         P1         XXh           00E2h         00E3h         Port P1 Direction Register         PD1         00h           00E4h         00E6h         0         0           00E5h         Port P3 Register         P3         XXh           00E7h         00E7h         00h         0           00E8h         Port P4 Register         P4         XXh           00E9h         00E0h         00h         0           00E8h         Port P4 Direction Register         PD4         00h           00E8h         00E0h         00h         0           00EBh         00E0h         00h         0           00EBh         00E0h         00h         0           00E9h         00E0h         00E0h         0           00E9h         00F0h         0         0           00E9h         00F0h         0         0           00F3h         00F3h         0         0           00F6h         0         0         0           00F8h         0         0         0           00F8h         0         0         0           00F8h         0         0				
00E1h         Port P1 Register         P1         XXh           00E2h         00E3h         Port P1 Direction Register         PD1         00h           00E3h         Port P3 Register         P3         XXh           00E6h         Port P3 Direction Register         PD3         00h           00E7h         Port P4 Register         P4         XXh           00E8h         Port P4 Lirection Register         PD4         00h           00EAh         Port P4 Direction Register         PD4         00h           00EDh         00E0h         00E0h         00E0h           00EDh         00F0h         00F0h         00F0h           00F3h         00F3h         00F3h         00F3h           00F6h         00F8h         00F3h         00F3h           00F3h         00F3h         00F3h         00F3h         00F3h           00F6				
00E2h         Port P1 Direction Register         PD1         00h           00E3h         Port P3 Register         P3         XXh           00E6h         00E7h         00h         00h           00E8h         Port P3 Direction Register         PD3         00h           00E8h         Port P4 Register         P4         XXh           00E8h         Port P4 Direction Register         PD4         00h           00EBh         00E0h         00h         00h           00EDh         00EDh         00EDh         00EDh           00EFh         00EPh         00FOh         00EDh           00F2h         00F3h         00F3h         00F3h           00F3h         00F6h         00F6h         00F8h           00F8h         00F8h         00F8h         00F8h           00FCh         00FDh         00FCh         00FDh           00FCh         00FDh         00FCh         00FDh			<u> </u>	100
00E3h         Port P1 Direction Register         PD1         00h           00E4h         00E6h         00E7h         Port P3 Register         P3         XXh           00E6h         00E7h         Port P3 Direction Register         PD3         00h           00E8h         Port P4 Register         P4         XXh           00E9h         00EAh         Port P4 Direction Register         PD4         00h           00ECh         00EBh         00ECh         00ECh         00ECh           00EFh         00EFh         00ECh         00ECh         00ECh           00F1h         00F3h         00F3h         00F3h         00F3h           00F3h         00F6h         00F9h         00F8h         00F8h           00F8h         00F8h         00F8h         00F8h           00FCh         00FBh         00FCh         00FBh           00FCh         00FCh         00FBh         00FEH		Port P1 Register	P1	XXh
00E3h         Port P1 Direction Register         PD1         00h           00E4h         00E6h         00E7h         Port P3 Register         P3         XXh           00E6h         00E7h         Port P3 Direction Register         PD3         00h           00E8h         Port P4 Register         P4         XXh           00E9h         00EAh         Port P4 Direction Register         PD4         00h           00ECh         00EBh         00ECh         00ECh         00ECh           00EFh         00EFh         00ECh         00ECh         00ECh           00F1h         00F3h         00F3h         00F3h         00F3h           00F3h         00F6h         00F9h         00F8h         00F8h           00F8h         00F8h         00F8h         00F8h           00FCh         00FBh         00FCh         00FBh           00FCh         00FCh         00FBh         00FEH				
00E4h         00E5h         Port P3 Register         P3         XXh           00E7h         Port P3 Direction Register         PD3         00h           00E8h         Port P4 Register         P4         XXh           00E9h         00EAh         PD4         00h           00EBh         00ED         00ED         00ED           00ECh         00EDh         00ED         00ED           00EFh         00Fh         00Fh         00Fh           00F3h         00F3h         00F3h         00F3h           00F6h         00F6h         00F8h         00F9h           00F8h         00F9h         00F8h         00F9h           00FBh         00FCh         00FBh         00FCh           00FCh         00FDh         00FCh         00FDh           00FEh         00FEh         00FEh         00FEh		Port P1 Direction Register	PD1	00h
00E5h         Port P3 Register         P3         XXh           00E7h         Port P3 Direction Register         PD3         00h           00E8h         Port P4 Register         P4         XXh           00E9h         PD4         00h           00EAh         POT P4 Direction Register         PD4         00h           00ECh         P00ECh				1
00E6h         00E7h         Port P3 Direction Register         PD3         00h           00E8h         Port P4 Register         P4         XXh           00EAh         Port P4 Direction Register         PD4         00h           00EBh         00EDh         00EDh         00EDh           00EPh         00EPh         00EDh         00EDh           00F1h         00F3h         00F3h         00F3h           00F3h         00F4h         00F6h         00F6h           00F7h         00F8h         00F9h         00F9h           00F8h         00F9h         00F8h         00F8h           00FBh         00FCh         00FDh         00FBh           00FCh         00FDh         00FBh         00FBh           00FEh         00FEh         00FEh         00FEh	000-111	Dort D2 Degister	D2	VVh
00E7h         Port P3 Direction Register         PD3         00h           00E8h         Port P4 Register         P4         XXh           00E9h         00EAh         Port P4 Direction Register         PD4         00h           00EBh         00ECh         00EDh	00501	FULL FO INEGISTER		۸۸۱۱
00E8h         Port P4 Register         P4         XXh           00E9h         00EAh         Port P4 Direction Register         PD4         00h           00EBh         00ECh         00EDh         00EDh </td <td></td> <td></td> <td></td> <td></td>				
00E8h         Port P4 Register         P4         XXh           00E9h         00EAh         Port P4 Direction Register         PD4         00h           00EBh         00ECh         00EDh         00EDh </td <td></td> <td>Port P3 Direction Register</td> <td></td> <td></td>		Port P3 Direction Register		
00E9h         00EAh         Port P4 Direction Register         PD4         00h           00EBh         00ECh         00EDh         00EBh         00FBh         00FBh <td>00E8h</td> <td>Port P4 Register</td> <td>P4</td> <td>XXh</td>	00E8h	Port P4 Register	P4	XXh
00EAh         Port P4 Direction Register         PD4         00h           00EBh         00ECh         00EDh         00EDh <td></td> <td><u> </u></td> <td></td> <td></td>		<u> </u>		
00EBh         00ECh           00EDh         00EBh           00EEh         00Fh           00FN         00Fh           00F1h         00Fh           00F3h         00Fh           00F4h         00Fsh           00F6h         00Fh           00F8h         00Fh           00F9h         00FAh           00FBh         00FCh           00FDh         00FDh           00FEh         00FDh	005011	Port P4 Direction Posistor	וחח	00b
00ECh         00EDh           00EEh         00Eh           00EFh         00F0h           00F0h         00F1h           00F2h         00F3h           00F3h         00F4h           00F5h         00F6h           00F7h         00F8h           00F9h         00F9h           00FAh         00FBh           00FCh         00FDh           00FDh         00FDh		FOIL F4 DIRECTION REGISTER	PD4	UUII
00EDh           00EFh           00Fh           00F0h           00F1h           00F2h           00F3h           00F4h           00F5h           00F6h           00F7h           00F8h           00F9h           00FAh           00FCh           00FCh           00FDh				
00EEh         00EFh           00F0h         00Fh           00F1h         00F2h           00F3h         00F4h           00F5h         00F6h           00F7h         00F8h           00F9h         00FAh           00FAh         00FCh           00FCh         00FDh           00FEh         00FDh				
00EEh         00EFh           00F0h         00Fh           00F1h         00F2h           00F3h         00F4h           00F5h         00F6h           00F7h         00F8h           00F9h         00FAh           00FAh         00FCh           00FCh         00FDh           00FEh         00FDh	00EDh			
00EFh         00F0h         00F1h         00F2h         00F3h         00F4h         00F5h         00F6h         00F7h         00F8h         00F9h         00FBh         00FCh         00FDh         00FDh				
00F0h         00F1h         00F2h         00F3h         00F4h         00F5h         00F6h         00F7h         00F8h         00F9h         00FAh         00FBh         00FCh         00FDh         00FEh				<u> </u>
00F1h       00F2h         00F3h       00F4h         00F5h       00F6h         00F7h       00F8h         00F9h       00FAh         00FBh       00FCh         00FDh       00FDh				
00F2h         00F3h         00F4h         00F5h         00F6h         00F7h         00F8h         00F9h         00FAh         00FBh         00FCh         00FDh         00FEh				
00F3h       00F4h         00F5h       00F6h         00F7h       00F8h         00F9h       00FAh         00FAh       00FBh         00FCh       00FCh         00FEh       00FBh				
00F3h       00F4h         00F5h       00F6h         00F7h       00F8h         00F9h       00FAh         00FAh       00FBh         00FCh       00FCh         00FEh       00FBh	00F2h			
00F4h         00F5h         00F6h         00F7h         00F8h         00F9h         00FBh         00FBh         00FCh         00FDh         00FEh				
00F5h         00F6h         00F7h         00F8h         00F9h         00FAh         00FBh         00FCh         00FDh         00FDh				<u> </u>
00F6h         00F7h         00F8h         00F9h         00FAh         00FBh         00FCh         00FDh         00FEh			<del></del>	
00F7h 00F8h 00F9h 00FAh 00FBh 00FCh 00FDh 00FEh				
00F8h 00F9h 00FAh 00FBh 00FCh 00FDh				
00F9h 00FAh 00FBh 00FCh 00FDh	00F7h			
00F9h 00FAh 00FBh 00FCh 00FDh				
00FAh       00FBh       00FCh       00FDh       00FEh				<u> </u>
00FBh         00FCh           00FDh         00FEh				
00FCh 00FDh 00FEh				
00FDh 00FEh				
00FDh 00FEh	00FCh			
00FEh				
				1
VVFFII				
/. Lia da fina a d				

X: Undefined
Note:

1. The blank areas are reserved and cannot be accessed by users.

SFR Information (12) (1) **Table 4.12** 

Address	Register	Symbol	After Reset
2CF0h	DTC Control Data 22	DTCD22	XXh
2CF1h			XXh
2CF2h			XXh
2CF3h			XXh
2CF4h			XXh
2CF5h			XXh
2CF6h			XXh
2CF7h			XXh
2CF8h	DTC Control Data 23	DTCD23	XXh
2CF9h			XXh
2CFAh			XXh
2CFBh			XXh
2CFCh			XXh
2CFDh			XXh
2CFEh			XXh
2CFFh			XXh
2D00h			
:		•	
2FFFh			
V. I II - £I		T.	J

X: Undefined

### **Table 4.13 ID Code Areas and Option Function Select Area**

Address	Area Name	Symbol	After Reset
:			-
FFDBh	Option Function Select Register 2	OFS2	(Note 1)
:			
FFDFh	ID1		(Note 2)
:			
FFE3h	ID2		(Note 2)
:			
FFEBh	ID3		(Note 2)
:			
FFEFh	ID4		(Note 2)
:			
FFF3h	ID5		(Note 2)
FFF7h	ID6		(Note 2)
:			1/11 / 0
FFFBh	ID7		(Note 2)
:		Long	101
FFFFh	Option Function Select Register	OFS	(Note 1)

- The option function select area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program. Do not write additions to the option function select area. If the block including the option function select area is erased, the option function select area is set to FFh.
  - When blank products are shipped, the option function select area is set to FFh. It is set to the written value after written by the user. When factory-programming products are shipped, the value of the option function select area is the value programmed by the user.
- The ID code areas are allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program. Do not write additions to the ID code areas. If the block including the ID code areas is erased, the ID code areas are set to FFh. When blank products are shipped, the ID code areas are set to FFh. They are set to the written value after written by the user. When factory-programming products are shipped, the value of the ID code areas is the value programmed by the user.

Note:

1. The blank areas are reserved and cannot be accessed by users.

R8C/32M Group 5. Electrical Characteristics

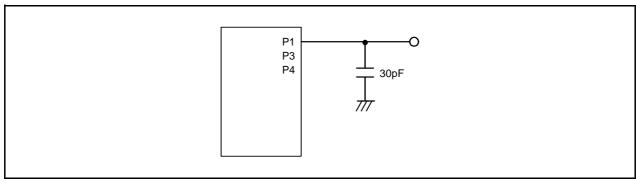


Figure 5.1 Ports P1, P3, P4 Timing Measurement Circuit

Table 5.7	Flash Memory	Data flash Block A to Block D	D) Electrical Characteristics
iubic o.i	i lasti metilory	Data Hash Blook A to Blook L	Licotrioai Oriaracteristics

Symbol	Parameter	Conditions		Unit		
Symbol	Farameter	Conditions	Min.	Тур.	Max.	Offic
_	Program/erase endurance (2)		10,000 (3)	-	-	times
_	Byte program time (program/erase endurance ≤ 1,000 times)		_	160	1,500	μS
_	Byte program time (program/erase endurance > 1,000 times)		-	300	1,500	μS
_	Block erase time (program/erase endurance ≤ 1,000 times)		-	0.2	1	S
_	Block erase time (program/erase endurance > 1,000 times)		-	0.3	1	S
td(SR-SUS)	Time delay from suspend request until suspend		_	-	5 + CPU clock × 3 cycles	ms
_	Interval from erase start/restart until following suspend request		0	=	_	μS
_	Time from suspend until erase restart		-	-	30+CPU clock × 1 cycle	μS
td(CMDRST- READY)	Time from when command is forcibly terminated until reading is enabled		-	-	30+CPU clock × 1 cycle	μS
-	Program, erase voltage		2.7	_	5.5	V
-	Read voltage		1.8	-	5.5	V
=	Program, erase temperature		-20 <sup>(7)</sup>	-	85	°C
=	Data hold time (8)	Ambient temperature = 55 °C	20	-	_	year

# Notes:

- 1. Vcc = 2.7 to 5.5 V and Topr = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
- 2. Definition of programming/erasure endurance
  - The programming and erasure endurance is defined on a per-block basis.

If the programming and erasure endurance is n (n = 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.

However, the same address must not be programmed more than once per erase operation (overwriting prohibited).

- 3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
- 4. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. In addition, averaging the erasure endurance between blocks A to D can further reduce the actual erasure endurance. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
- 5. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
- 6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
- 7. -40°C for D version.
- 8. The data hold time includes time that the power supply is off or the clock is not supplied.

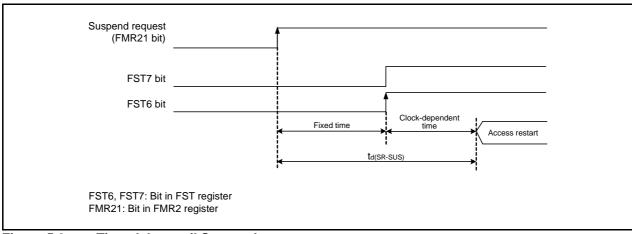


Figure 5.2 Time delay until Suspend

R8C/32M Group 5. Electrical Characteristics

Table 5.10 Voltage Detection 2 Circuit Electrical Characteristics

Cumbal	Parameter	Condition		Unit		
Symbol	Parameter	Condition	Min.	Тур.	Max.	Offic
Vdet2	Voltage detection level Vdet2_0 (2)	At the falling of Vcc	3.70	4.00	4.30	V
Voltage detection level Vdet2_EXT (2)		At the falling of LVCMP2	1.20	1.34	1.48	V
_	Hysteresis width at the rising of Vcc in voltage detection 2 circuit		-	0.10	-	V
_	Voltage detection 2 circuit response time (3)	At the falling of Vcc from 5 V to (Vdet2_0 - 0.1) V	-	20	150	μS
_	Voltage detection circuit self power consumption	VCA27 = 1, Vcc = 5.0 V	_	1.7	_	μΑ
td(E-A)	Waiting time until voltage detection circuit operation starts <sup>(4)</sup>		-		100	μS

### Notes:

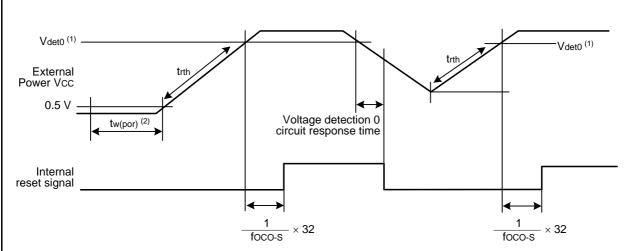
- 1. The measurement condition is Vcc = 1.8 V to 5.5 V and  $T_{opr} = -20$  to  $85^{\circ}C$  (N version) / -40 to  $85^{\circ}C$  (D version).
- 2. The voltage detection level varies with detection targets. Select the level with the VCA24 bit in the VCA2 register.
- 3. Time until the voltage monitor 2 interrupt request is generated after the voltage passes Vdet2.
- 4. Necessary time until the voltage detection circuit operates after setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.

Table 5.11 Power-on Reset Circuit (2)

Symbol	Parameter	Condition		Unit		
	Faiametei	Condition	Min.	Тур.	Max.	Offic
trth	External power Vcc rise gradient	(1)	0	_	50,000	mV/ms

### Notes:

- 1. The measurement condition is Topr = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
- 2. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS register to 0.



- 1. Vdeto indicates the voltage detection level of the voltage detection 0 circuit. Refer to **6. Voltage Detection Circuit** of User's Manual: Hardware for details.
- 2. tw(por) indicates the duration the external power Vcc must be held below the valid voltage (0.5 V) to enable a power-on reset. When turning on the power after it falls with voltage monitor 0 reset disabled, maintain tw(por) for 1 ms or more.

Figure 5.3 Power-on Reset Circuit Electrical Characteristics

R8C/32M Group 5. Electrical Characteristics

**Table 5.12 High-speed On-Chip Oscillator Circuit Electrical Characteristics** 

C: male al	Devenuetos	Condition		Standard		Unit
Symbol	Parameter	Condition	Min.	Тур.	Max.	Unit
=	High-speed on-chip oscillator frequency after reset	Vcc = 1.8 V to 5.5 V -20°C ≤ Topr ≤ 85°C	39.4	40	40.6	MHz
		Vcc = 1.8 V to 5.5 V -40°C ≤ Topr ≤ 85°C	39.4	40	40.6	MHz
		Vcc = 1.8 V to 5.5 V Topr = 25°C	39.6	40	40.4	MHz
	High-speed on-chip oscillator frequency when the FRA4 register correction value is written into	Vcc = 1.8 V to 5.5 V -20°C ≤ Topr ≤ 85°C	36.311	36.864	37.417	MHz
		Vcc = 1.8 V to 5.5 V -40°C ≤ Topr ≤ 85°C	36.311	36.864	37.417	MHz
		Vcc = 1.8 V to 5.5 V Topr = 25°C	36.495	36.864	37.233	MHz
	High-speed on-chip oscillator frequency when the FRA6 register correction value is written into	Vcc = 1.8 V to 5.5 V -20°C ≤ Topr ≤ 85°C	31.52	32	32.48	MHz
	correction value into the FRA3 register	Vcc = 1.8 V to 5.5 V -40°C ≤ Topr ≤ 85°C	31.52	32	32.48	MHz
		Vcc = 1.8 V to 5.5 V Topr = 25°C	31.68	32	32.32	MHz
_	Oscillation stability time	Vcc = 5.0 V, Topr = 25°C	_	100	450	μS
=	Self power consumption at oscillation	Vcc = 5.0 V, Topr = 25°C	-	500	_	μΑ

### Notes:

- 1. Vcc = 1.8 to 5.5 V, Topr = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
- 2. This enables the setting errors of bit rates such as 9600 bps and 38400 bps to be 0% when the serial interface is used in

**Table 5.13** Low-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition		Unit		
Symbol	Farameter	Condition	Min.	Тур.	Max.	Offic
fOCO-S	Low-speed on-chip oscillator frequency		60	125	250	kHz
_	Oscillation stability time	Vcc = 5.0 V, Topr = 25°C	_	30	100	μS
_	Self power consumption at oscillation	Vcc = 5.0 V, Topr = 25°C	_	2	-	μА
fOCO-WDT	Low-speed on-chip oscillator frequency for the watchdog timer		60	125	250	kHz
_	Oscillation stability time	Vcc = 5.0 V, Topr = 25°C	_	30	100	μS
_	Self power consumption at oscillation	Vcc = 5.0 V, Topr = 25°C	-	2	-	μА

1. Vcc = 1.8 to 5.5 V,  $T_{opr} = -20$  to  $85^{\circ}C$  (N version) / -40 to  $85^{\circ}C$  (D version), unless otherwise specified.

**Table 5.14 Power Supply Circuit Timing Characteristics** 

Symbol	Parameter	Condition	Standard			Unit
Syllibol	Falametei	Condition	Min.	Тур.	Max.	Offic
td(P-R)	Time for internal power supply stabilization during power-on <sup>(2)</sup>		I	=	2,000	μS

- The measurement condition is Vcc = 1.8 to 5.5 V and T<sub>opr</sub> = 25°C.
   Waiting time until the internal power supply generation circuit stabilizes during power-on.

R8C/32M Group 5. Electrical Characteristics

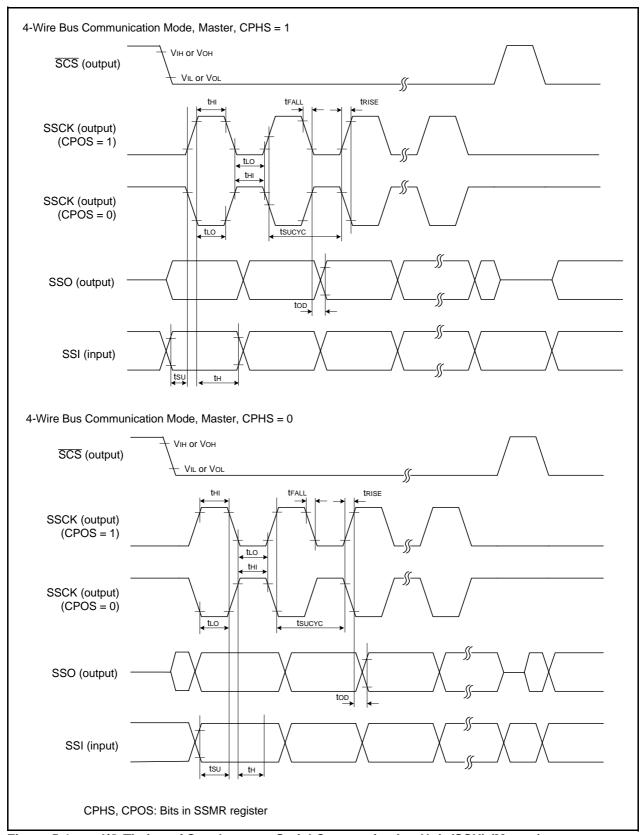


Figure 5.4 I/O Timing of Synchronous Serial Communication Unit (SSU) (Master)

Table 5.18 Electrical Characteristics (2) [3.3 V  $\leq$  Vcc  $\leq$  5.5 V] (Topr = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)

0	5 .	Condition		Standard			116-24
Symbol	Parameter		Condition	Min.	Typ.	Max.	Unit
Icc	Power supply current (Vcc = 3.3 to 5.5 V)	High-speed clock mode	XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	-	6.5	15	mA
	Single-chip mode, output pins are open, other pins		XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	_	5.3	12.5	mA
	are Vss		XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	_	3.6	-	mA
			XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	_	3.0	_	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	_	2.2	_	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	_	1.5	_	mA
	High-speed on-chip oscillator mode  Low-speed on-chip oscillator mode  Low-speed clock mode	on-chip	XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz No division	_	7.0	15	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	_	3.0	_	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 4 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-16 MSTIRC = MSTTRD = MSTTRC = 1	-	1	_	mA
		on-chip	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR27 = 1, VCA20 = 0	-	90	400	μА
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz No division FMR27 = 1, VCA20 = 0	-	85	400	μА
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz No division Program operation on RAM Flash memory off, FMSTP = 1, VCA20 = 0	-	47	-	μА
	Wait mode	Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	-	15	100	μА
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	_	4	90	μА
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (peripheral clock off) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	-	3.5	-	μА
		Stop mode	XIN clock off, Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	-	2.0	5.0	μА
			XIN clock off, Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	_	5.0	_	μА

Table 5.23 Electrical Characteristics (3) [2.7 V  $\leq$  Vcc < 4.2 V]

Symbol	Do	ameter	Conditi	0.0	Standard			Unit
Symbol	Par	ameter	Conditi	On	Min.	Тур.	Max.	Unit
Vон	Output "H" voltage	Other than XOUT	Drive capacity High	Iон = −5 mA	Vcc - 0.5	=	Vcc	V
			Drive capacity Low	Iон = −1 mA	Vcc - 0.5	-	Vcc	V
		XOUT		Ioн = -200 μA	1.0	-	Vcc	V
Vol	Output "L" voltage	Other than XOUT	Drive capacity High	IoL = 5 mA	=	-	0.5	V
			Drive capacity Low	IoL = 1 mA	=	-	0.5	V
		XOUT		IoL = 200 μA	=	-	0.5	V
VT+-VT-	Hysteresis	INTO, INT1, INT3, KIO, KI1, KI2, KI3, TRAIO, TRCIOA, TRCIOB, TRCIOC, TRCIOD, TRCTRG, TRCCLK, ADTRG, RXD0, RXD2, CLK0, CLK2, SSI, SCL, SDA, SSO	Vcc = 3.0 V		0.1	0.4	-	V
		RESET	Vcc = 3.0 V		0.1	0.5	_	V
lін	Input "H" current		VI = 3 V, Vcc = 3.0 \	/	=	-	4.0	μΑ
lıL	Input "L" current		VI = 0 V, Vcc = 3.0 \	/	=	-	-4.0	μΑ
RPULLUP	Pull-up resistance		VI = 0 V, Vcc = 3.0 \	/	42	84	168	kΩ
RfXIN	Feedback resistance	XIN			-	0.3	_	МΩ
RfXCIN	Feedback resistance	XCIN			_	8	_	МΩ
VRAM	RAM hold voltage		During stop mode		1.8	-	_	V

<sup>1.</sup>  $2.7 \text{ V} \le \text{Vcc} < 4.2 \text{ V}$  and  $\text{Topr} = -20 \text{ to } 85^{\circ}\text{C}$  (N version) /  $-40 \text{ to } 85^{\circ}\text{C}$  (D version), f(XIN) = 10 MHz, unless otherwise specified.

Table 5.29 Electrical Characteristics (5) [1.8 V  $\leq$  Vcc < 2.7 V]

Symbol	Dor	ameter	Conditi	on	Standard			Unit
Symbol	Fai	ametei	Conditi	OH	Min.	Тур.	Max.	Offic
Vон	Output "H" voltage	Other than XOUT	Drive capacity High	Iон = −2 mA	Vcc - 0.5	=	Vcc	V
			Drive capacity Low	Iон = −1 mA	Vcc - 0.5	-	Vcc	V
		XOUT		$IOH = -200 \mu A$	1.0	-	Vcc	V
Vol	Output "L" voltage	Other than XOUT	Drive capacity High	IoL = 2 mA	=	-	0.5	V
			Drive capacity Low	IoL = 1 mA	=	=	0.5	V
		XOUT		IoL = 200 μA	=	=	0.5	V
VT+-VT-	Hysteresis	INTO, INT1, INT3, KIO, KI1, KI2, KI3, TRAIO, TRCIOA, TRCIOB, TRCIOC, TRCIOD, TRCTRG, TRCCLK, ADTRG, RXD0, RXD2, CLK0, CLK2, SSI, SCL, SDA, SSO	Vcc = 2.2 V		0.05	0.2	_	V
		RESET	Vcc = 2.2 V		0.05	0.20	_	V
Iн	Input "H" current		VI = 2.2  V,  VCC = 2.2  V	2 V	ı	_	4.0	μΑ
lıL	Input "L" current		VI = 0 V, Vcc = 2.2 \	/	1	I	-4.0	μΑ
RPULLUP	Pull-up resistance		VI = 0 V, Vcc = 2.2 \	/	70	140	300	kΩ
RfXIN	Feedback resistance	XIN			-	0.3	-	ΜΩ
RfXCIN	Feedback resistance	XCIN			=	8	-	ΜΩ
VRAM	RAM hold voltage		During stop mode		1.8	-	-	V

<sup>1.</sup>  $1.8 \text{ V} \le \text{Vcc} < 2.7 \text{ V}$  at Topr = -20 to 85°C (N version) / -40 to 85°C (D version), f(XIN) = 5 MHz, unless otherwise specified.

Table 5.30 Electrical Characteristics (6) [1.8 V  $\leq$  Vcc < 2.7 V] (Topr = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
Symbol	Parameter		Condition	Min.	Тур.	Max.	Unit
Icc	Power supply current (Vcc = 1.8 to 2.7 V) Single-chip mode, output pins are open,	High-speed clock mode	XIN = 5 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	-	2.2	=	mA
	other pins are Vss		XIN = 5 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	_	0.8	_	mA
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO-F = 5 MHz Low-speed on-chip oscillator on = 125 kHz No division	-	2.5	10	mA
	mode	XIN clock off High-speed on-chip oscillator on fOCO-F = 5 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	-	1.7	_	mA	
			XIN clock off High-speed on-chip oscillator on fOCO-F = 4 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-16 MSTIIC = MSTTRD = MSTTRC = 1	-	1	_	mA
		Low-speed on- chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR27 = 1, VCA20 = 0	_	90	300	μА
		Low-speed clock mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz No division FMR27 = 1, VCA20 = 0	-	80	350	μА
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz No division Program operation on RAM Flash memory off, FMSTP = 1, VCA20 = 0	_	40	-	μА
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	_	15	90	μА
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	_	4	80	μА
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (peripheral clock off) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	-	3.5	-	μА
		Stop mode	XIN clock off, Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	-	2.0	5	μА
			XIN clock off, Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	=	5.0	-	μА

Table 5.33 Seria	Interface
------------------	-----------

Symbol		Parameter	Stan	ıdard	Unit
Symbol		Falanetei	Min.	Max.	Onit
tc(CK)	CLKi input cycle time	When external clock is selected	800	-	ns
tW(CKH)	CLKi input "H" width		400	-	ns
tW(CKL)	CLKi input "L" width		400	-	ns
td(C-Q)	TXDi output delay time		-	200	ns
th(C-Q)	TXDi hold time		0	-	ns
tsu(D-C)	RXDi input setup time		150	-	ns
th(C-D)	RXDi input hold time		90	-	ns
td(C-Q)	TXDi output delay time	When internal clock is selected	-	200	ns
tsu(D-C)	RXDi input setup time		150	-	ns
th(C-D)	RXDi input hold time		90	-	ns

i = 0, 2 Note:

1. Vcc = 2.2 V and  $Topr = -20 \text{ to } 85 \,^{\circ}\text{C}$  (N version)/ $-40 \text{ to } 85 \,^{\circ}\text{C}$  (D version), unless otherwise specified.

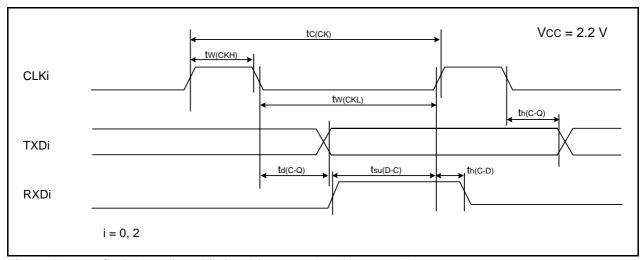


Figure 5.18 Serial Interface Timing Diagram when Vcc = 2.2 V

Table 5.34 External Interrupt  $\overline{\text{INTi}}$  (i = 0, 1, 3) Input, Key Input Interrupt  $\overline{\text{Kli}}$  (i = 0 to 3)

Symbol	Parameter		Standard		
	Falanielei	Min.	Max.	Unit	
tw(INH)	ĪNTi input "H" width, Kli input "H" width	1000 (1)	-	ns	
tw(INL)	INTi input "L" width, Kli input "L" width	1000 (2)	1	ns	

- 1. When selecting the digital filter by the  $\overline{\text{INTi}}$  input filter select bit, use an  $\overline{\text{INTi}}$  input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
- 2. When selecting the digital filter by the  $\overline{\text{INTi}}$  input filter select bit, use an  $\overline{\text{INTi}}$  input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

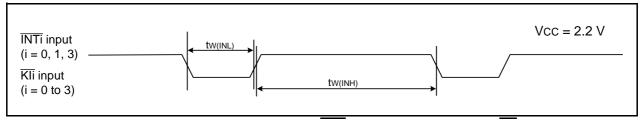
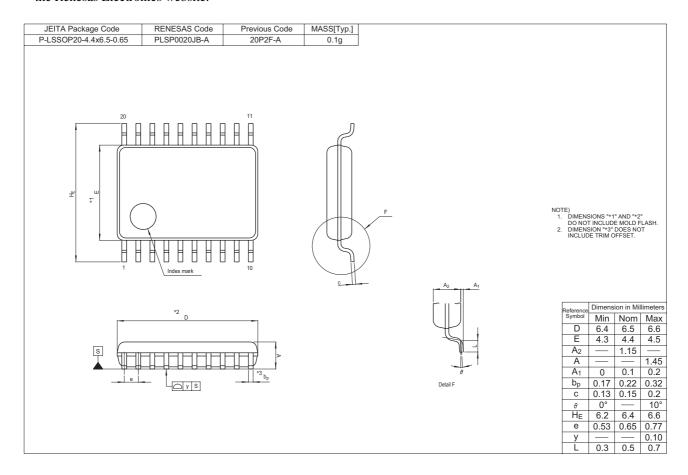


Figure 5.19 Input Timing for External Interrupt INTi and Key Input Interrupt Kli when Vcc = 2.2 V

R8C/32M Group Package Dimensions

# **Package Dimensions**

Diagrams showing the latest package dimensions and mounting information are available in the "Packages" section of the Renesas Electronics website.



# General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

### 1. Handling of Unused Pins

Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

# 2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

# 3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

 The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

# 4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

— When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

# 5. Differences between Products

Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

— The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.