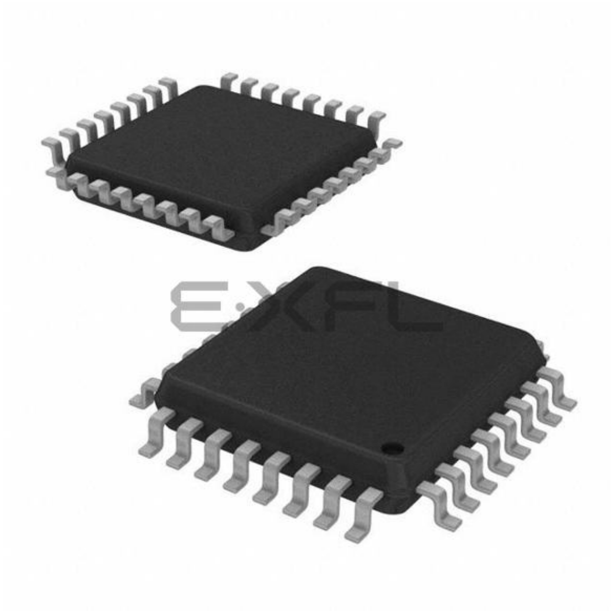
Microchip Technology - AT89C51CC02CA-RATUM Datasheet



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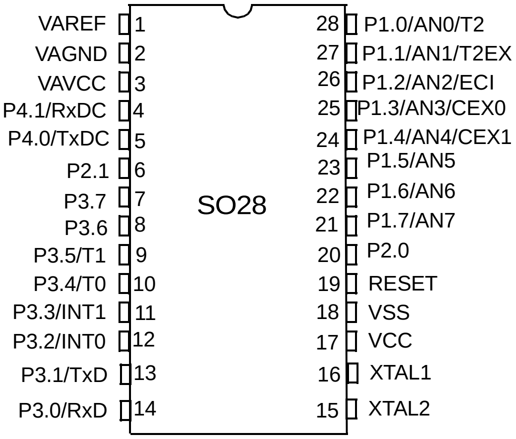
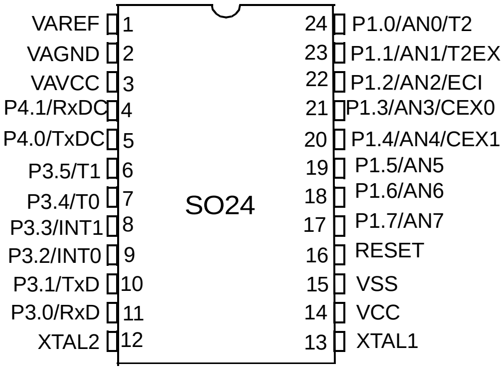
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	80C51
Core Size	8-Bit
Speed	40MHz
Connectivity	CANbus, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	20
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-VQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at89c51cc02ca-ratum

Pin Configurations





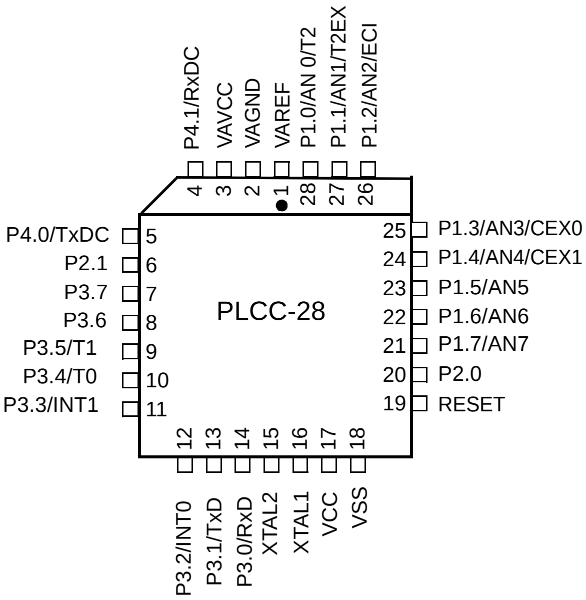
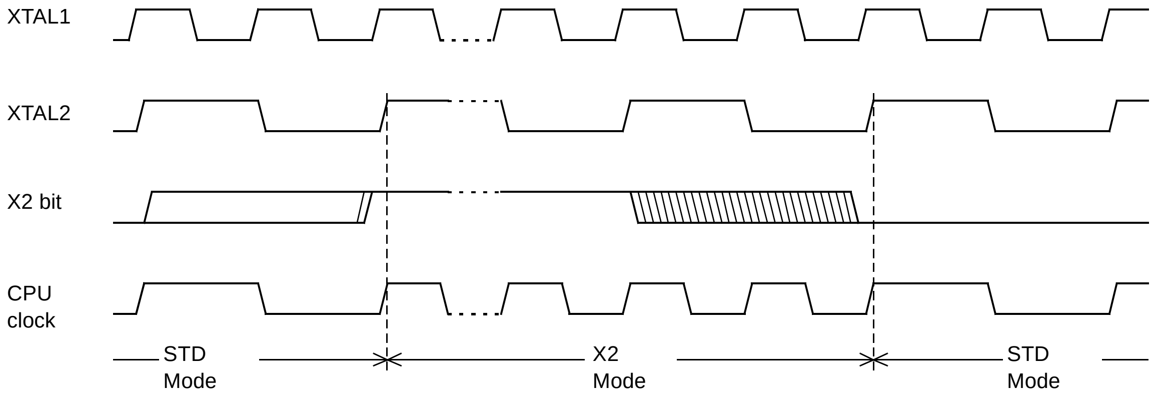


Table 9. CAN SFRs (Continued)

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
CANEN	CFh	CAN Enable Channel byte					ENCH3	ENCH2	ENCH1	ENCH0
CANGIE	C1h	CAN General Interrupt Enable			ENRX	ENTX	ENERCH	ENBUF	ENERG	
CANIE	C3h	CAN Interrupt Enable Channel byte					IECH3	IECH2	IECH1	IECH0
CANSIT	BBh	CAN Status Interrupt Channel byte					SIT3	SIT2	SIT1	SIT0
CANTCON	A1h	CAN Timer Control	TPRESC 7	TPRESC 6	TPRESC 5	TPRESC 4	TPRESC 3	TPRESC 2	TPRESC 1	TPRESC 0
CANTIMH	ADh	CAN Timer high	CANTIM 15	CANTIM 14	CANTIM 13	CANTIM 12	CANTIM 11	CANTIM 10	CANTIM 9	CANTIM 8
CANTIML	ACh	CAN Timer low	CANTIM 7	CANTIM 6	CANTIM 5	CANTIM 4	CANTIM 3	CANTIM 2	CANTIM 1	CANTIM 0
CANSTMPH	AFh	CAN Timer Stamp high	TIMSTMP 15	TIMSTMP 14	TIMSTMP 13	TIMSTMP 12	TIMSTMP 11	TIMSTMP 10	TIMSTMP 9	TIMSTMP 8
CANSTMPL	AEh	CAN Timer Stamp low	TIMSTMP7	TIMSTMP 6	TIMSTMP 5	TIMSTMP 4	TIMSTMP 3	TIMSTMP 2	TIMSTMP 1	TIMSTMP 0
CANTTCH	A5h	CAN Timer TTC high	TIMTTC 15	TIMTTC 14	TIMTTC 13	TIMTTC 12	TIMTTC 11	TIMTTC 10	TIMTTC 9	TIMTTC 8
CANTTCL	A4h	CAN Timer TTC low	TIMTTC 7	TIMTTC 6	TIMTTC 5	TIMTTC 4	TIMTTC 3	TIMTTC 2	TIMTTC 1	TIMTTC 0
CANTEC	9Ch	CAN Transmit Error Counter	TEC7	TEC6	TEC5	TEC4	TEC3	TEC2	TEC1	TEC0
CANREC	9Dh	CAN Receive Error Counter	REC7	REC6	REC5	REC4	REC3	REC2	REC1	REC0
CANPAGE	B1h	CAN Page	-	-	CHNB1	CHNB0	AINC	INDX2	INDX1	INDX0
CANSTCH	B2h	CAN Status Channel	DLCW	TXOK	RXOK	BERR	SERR	CERR	FERR	AERR
CANCONCH	B3h	CAN Control Channel	CONCH1	CONCH0	RPLV	IDE	DLC3	DLC2	DLC1	DLC0
CANMSG	A3h	CAN Message Data	MSG7	MSG6	MSG5	MSG4	MSG3	MSG2	MSG1	MSG0
CANIDT1	BCh	CAN Identifier Tag byte 1(Part A) CAN Identifier Tag byte 1(PartB)	IDT10 IDT28	IDT9 IDT27	IDT8 IDT26	IDT7 IDT25	IDT6 IDT24	IDT5 IDT23	IDT4 IDT22	IDT3 IDT21
CANIDT2	BDh	CAN Identifier Tag byte 2 (PartA) CAN Identifier Tag byte 2 (PartB)	IDT2 IDT20	IDT1 IDT19	IDT0 IDT18	- IDT17	- IDT16	- IDT15	- IDT14	- IDT13
CANIDT3	BEh	CAN Identifier Tag byte 3(PartA) CAN Identifier Tag byte 3(PartB)	- IDT12	- IDT11	- IDT10	- IDT9	- IDT8	- IDT7	- IDT6	- IDT5
CANIDT4	BFh	CAN Identifier Tag byte 4(PartA) CAN Identifier Tag byte 4(PartB)	- IDT4	- IDT3	- IDT2	- IDT1	- IDT0	RTRTAG	- RB1TAG	RB0TAG
CANIDM1	C4h	CAN Identifier Mask byte 1(PartA) CAN Identifier Mask byte 1(PartB)	IDMSK10 IDMSK28	IDMSK9 IDMSK27	IDMSK8 IDMSK26	IDMSK7 IDMSK25	IDMSK6 IDMSK24	IDMSK5 IDMSK23	IDMSK4 IDMSK22	IDMSK3 IDMSK21

Figure 4. Mode Switching Waveforms[(1)]

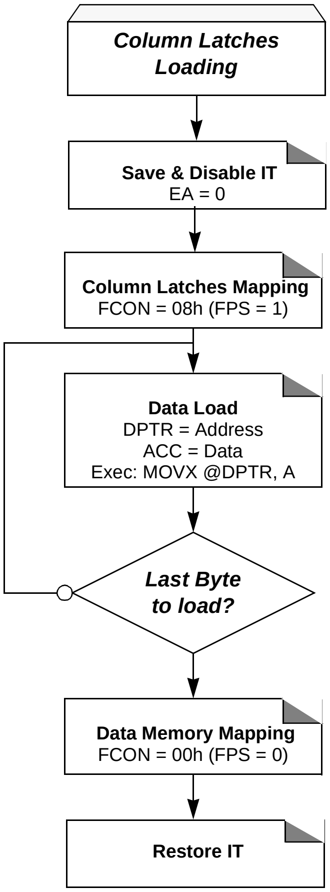


Note: 1. In order to prevent any incorrect operation while operating in the X2 Mode, users must be aware that all peripherals using the clock frequency as a time reference (UART, timers...) will have their time reference divided by 2. For example, a free running timer generating an interrupt every 20 ms will then generate an interrupt every 10 ms. A UART with a 4800 baud rate will have a 9600 baud rate.

Table 15. Pin Conditions in Special Operating Modes

Mode	Port 1	Port 2	Port 3	Port 4
Reset	High	High	High	High
Idle (internal code)	Data	Data	Data	Data
Idle (external code)	Data	Data	Data	Data
Power-Down(internal code)	Data	Data	Data	Data
Power-Down (external code)	Data	Data	Data	Data

Figure 14. Column Latches Loading Procedure[1]



Note: 1. The last page address used when loading the column latch is the one used to select the page programming address.

Programming the Flash Spaces

User

The following procedure is used to program the User space and is summarized in Figure 15:

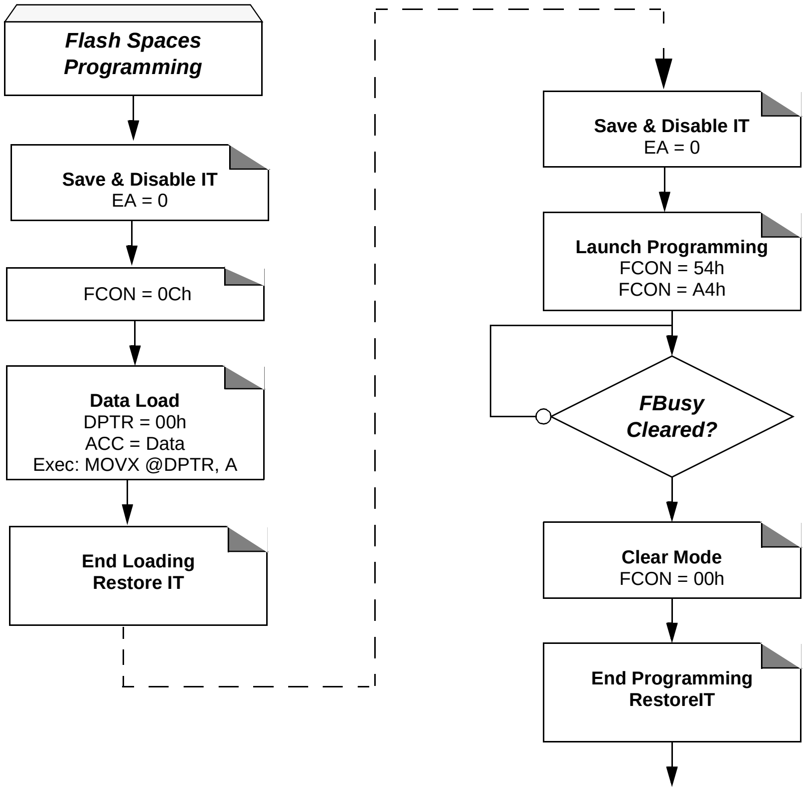
- Load up to one page of data in the column latches from address 0000h to 3FFFh.
- Save then disable the interrupts.
- Launch the programming by writing the data sequence 50h followed by A0h in FCON register.This step must be executed from FM1.
  The end of the programming indicated by the FBUSY flag cleared.
- Restore the interrupts.

Extra Row

The following procedure is used to program the Extra Row space and is summarized in Figure 15:

- Load data in the column latches from address FF80h to FFFFh.
- Save then disable the interrupts.
- Launch the programming by writing the data sequence 52h followed by A2h in FCON register. This step of the procedure must be executed from FM1.
  The end of the programming indicated by the FBUSY flag cleared.
- Restore the interrupts.

Figure 16. Hardware Programming Procedure



Reading the Flash Spaces

User

The following procedure is used to read the User space:

- Read one byte in Accumulator by executing MOVC A,@A+DPTR with A+DPTR is the address of the code byte to read.

Note: FCON must be cleared (00h) when not used.

Extra Row

The following procedure is used to read the Extra Row space and is summarized in Figure 17:

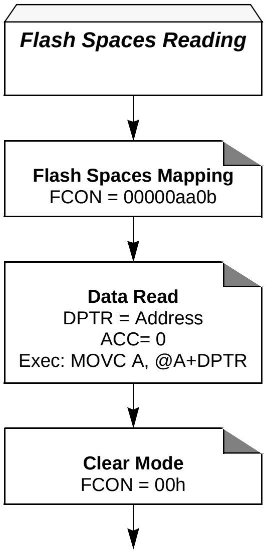
- Map the Extra Row space by writing 02h in FCON register.
- Read one byte in Accumulator by executing MOVC A,@A+DPTR with A= 0 & DPTR= FF80h to FFFFh.
- Clear FCON to unmap the Extra Row.

Hardware Security Byte

The following procedure is used to read the Hardware Security Byte and is summarized in Figure 17:

- Map the Hardware Security space by writing 04h in FCON register.
- Read the byte in Accumulator by executing MOVC A,@A+DPTR with A= 0 & DPTR= 0000h.
- Clear FCON to unmap the Hardware Security Byte.

Figure 17. Reading Procedure



Note: aa = 10 for the Hardware Security Byte.

Flash Protection from Parallel Programming

The three lock bits in Hardware Security Byte (See 'In-System Programming' section) are programmed according to Table 24 provide different level of protection for the on-chip code and data located in FM0 and FM1.

The only way to write this bits are the parallel mode. They are set by default to level 3.

Table 24. Program Lock bit

Program Lock bits				
Security Level	LB0	LB1	LB2	**Protection Description**
1	U	U	U	No program lock features enabled.
2	P	U	U	Parallel programming of the Flash is disabled.
3	U	P	U	Same as 2, also verify through parallel programming interface is disabled. This is the factory defaul programming.
4	U	U	P	Same as 3

Note: 1. Program Lock bits
U: unprogrammed
P: programmed

WARNING: Security level 2, 3 and 4 should only be programmed after Flash and Core verification.

Preventing Flash Corruption

See Section “Power Management”.

Programmable Clock-Output

In clock-out mode, Timer 2 operates as a 50%-duty-cycle, programmable clock generator (Figure 30). The input clock increments TL2 at frequency $f_{OSC}/2$. The timer repeatedly counts to overflow from a loaded value. At overflow, the contents of RCAP2H and RCAP2L registers are loaded into TH2 and TL2. In this mode, Timer 2 overflows do not generate interrupts. The formula gives the clock-out frequency depending on the system oscillator frequency and the value in the RCAP2H and RCAP2L registers:

$$Clock-OutFrequency = \frac{FT2clock}{4 \times (65536 - RCAP2H/RCAP2L)}$$

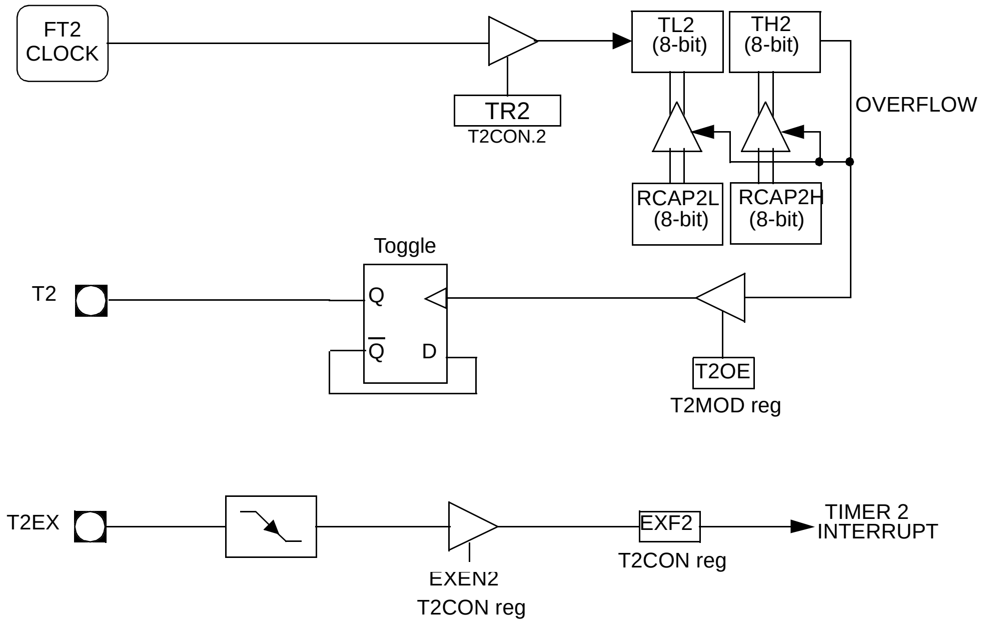
For a 16 MHz system clock in x1 mode, Timer 2 has a programmable frequency range of 61 Hz ($f_{OSC}/2^{16)}$ to 4 MHz ($f_{OSC}/4$). The generated clock signal is brought out to T2 pin (P1.0).

Timer 2 is programmed for the clock-out mode as follows:

- Set T2OE bit in T2MOD register.
- Clear $C/\overline{T2}$ bit in T2CON register.
- Determine the 16-bit reload value from the formula and enter it in RCAP2H/RCAP2L registers.
- Enter a 16-bit initial value in timer registers TH2/TL2. It can be the same as the reload value or different depending on the application.
- To start the timer, set TR2 run control bit in T2CON register.

It is possible to use Timer 2 as a baud rate generator and a clock generator simultaneously. For this configuration, the baud rates and clock frequencies are not independent since both functions use the values in the RCAP2H and RCAP2L registers.

Figure 30. Clock-Out Mode



Registers

Table 44. T2CON Register
T2CON (S:C8h)
Timer 2 Control Register

7	6	5	4	3	2	1	0
TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2#	CP/RL2#

Bit Number	Bit Mnemonic	Description
7	TF2	**Timer 2 Overflow Flag** TF2 is not set if RCLK=1 or TCLK = 1. Must be cleared by software. Set by hardware on Timer 2 overflow.
6	EXF2	**Timer 2 External Flag** Set when a capture or a reload is caused by a negative transition on T2EX pin if EXEN2=1. Set to cause the CPU to vector to Timer 2 interrupt routine when Timer 2 interrupt is enabled. Must be cleared by software.
5	RCLK	**Receive Clock bit** Clear to use timer 1 overflow as receive clock for serial port in mode 1 or 3. Set to use Timer 2 overflow as receive clock for serial port in mode 1 or 3.
4	TCLK	**Transmit Clock bit** Clear to use timer 1 overflow as transmit clock for serial port in mode 1 or 3. Set to use Timer 2 overflow as transmit clock for serial port in mode 1 or 3.
3	EXEN2	**Timer 2 External Enable bit** Clear to ignore events on T2EX pin for Timer 2 operation. Set to cause a capture or reload when a negative transition on T2EX pin is detected, if Timer 2 is not used to clock the serial port.
2	TR2	**Timer 2 Run Control bit** Clear to turn off Timer 2. Set to turn on Timer 2.
1	C/T2#	**Timer/Counter 2 Select bit** Clear for timer operation (input from internal clock system: f_{OSC}). Set for counter operation (input from T2 input pin).
0	CP/RL2#	**Timer 2 Capture/Reload bit** If RCLK=1 or TCLK=1, CP/RL2# is ignored and timer is forced to auto-reload on Timer 2 overflow. Clear to auto-reload on Timer 2 overflows or negative transitions on T2EX pin if EXEN2=1. Set to capture on negative transitions on T2EX pin if EXEN2=1.

Reset Value = 0000 0000b
bit addressable

Table 47. TL2 Register
TL2 (S:CCh)
Timer 2 Low Byte Register

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-

Bit Number	Bit Mnemonic	Description
7 - 0		Low Byte of Timer 2

Reset Value = 0000 0000b
Not bit addressable

Table 48. RCAP2H Register
RCAP2H (S:CBh)
Timer 2 Reload/Capture High Byte Register

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-

Bit Number	Bit Mnemonic	Description
7 - 0		High Byte of Timer 2 Reload/Capture.

Reset Value = 0000 0000b
Not bit addressable

Table 49. RCAP2L Register
RCAP2L (S:CAh) Timer 2 Reload/Capture Low Byte Register

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-

Bit Number	Bit Mnemonic	Description
7 - 0		Low Byte of Timer 2 Reload/Capture.

Reset Value = 0000 0000b
Not bit addressable

Watchdog Timer During Power-down Mode and Idle

In Power-down mode the oscillator stops, which means the WDT also stops. While in Power-down mode, the user does not need to service the WDT. There are 2 methods of exiting Power-down mode: by a hardware reset or via a level activated external interrupt which is enabled prior to entering Power-down mode. When Power-down is exited with hardware reset, the watchdog is disabled. Exiting Power-down with an interrupt is significantly different. The interrupt shall be held low long enough for the oscillator to stabilize. When the interrupt is brought high, the interrupt is serviced. To prevent the WDT from resetting the device while the interrupt pin is held low, the WDT is not started until the interrupt is pulled high. It is suggested that the WDT be reset during the interrupt service for the interrupt used to exit Power-down.

To ensure that the WDT does not overflow within a few states of exiting powerdown, it is best to reset the WDT just before entering powerdown.

In the Idle mode, the oscillator continues to run. To prevent the WDT from resetting T89C51CC02 while in Idle mode, the user should always set up a timer that will periodically exit Idle, service the WDT, and re-enter Idle mode.

Register

Table 52. WDTPRG Register
WDTPRG (S:A7h) – Watchdog Timer Duration Programming register

7	6	5	4	3	2	1	0
-	-	-	-	-	S2	S1	S0

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
6	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
3	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
2	S2	**Watchdog Timer Duration selection bit 2** Work in conjunction with bit 1 and bit 0.
1	S1	**Watchdog Timer Duration selection bit 1** Work in conjunction with bit 2 and bit 0.
0	S0	**Watchdog Timer Duration selection bit 0** Work in conjunction with bit 1 and bit 2.

Reset Value = XXXX X000b

Figure 37. CAN Controller Memory Organization

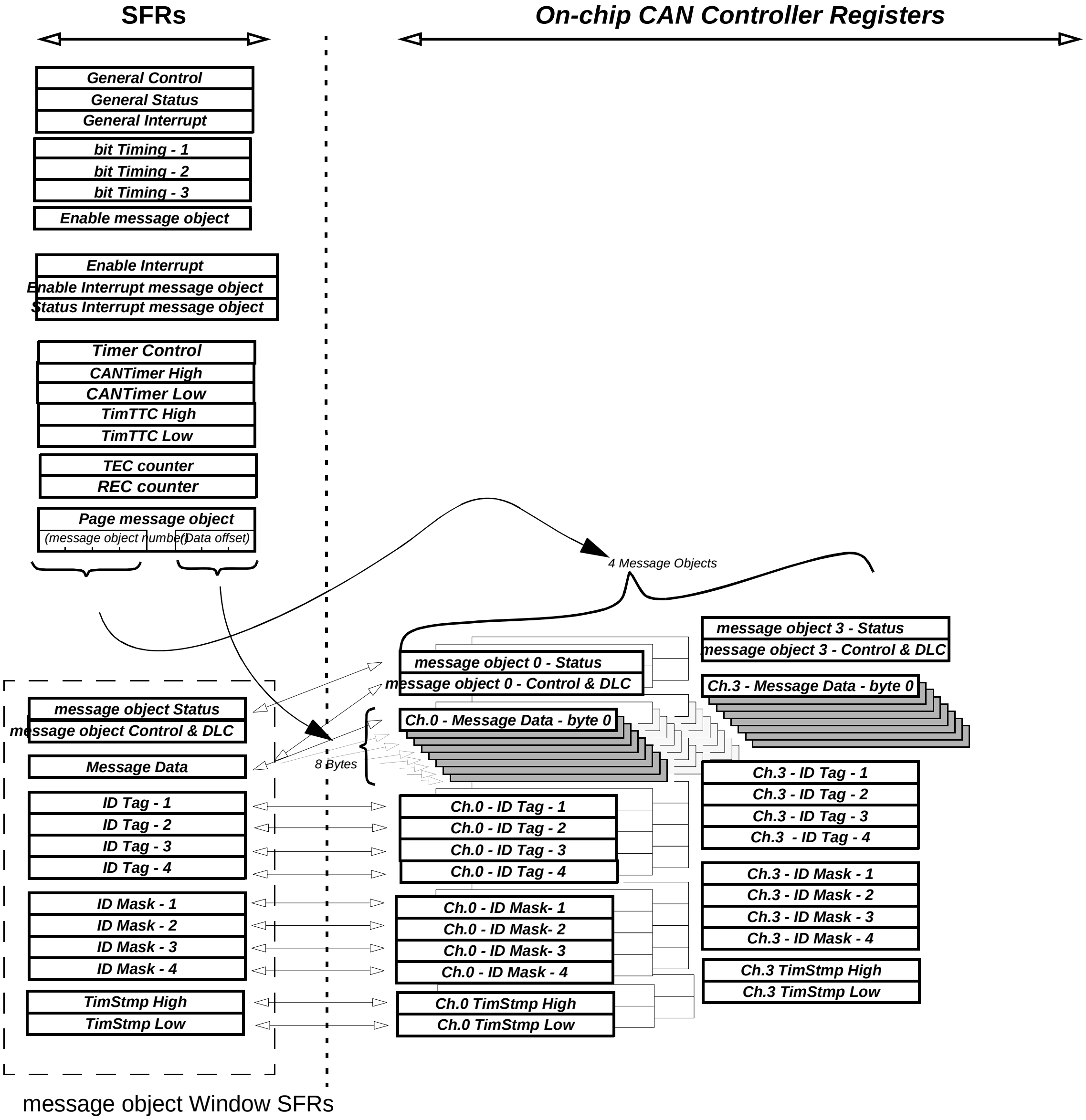
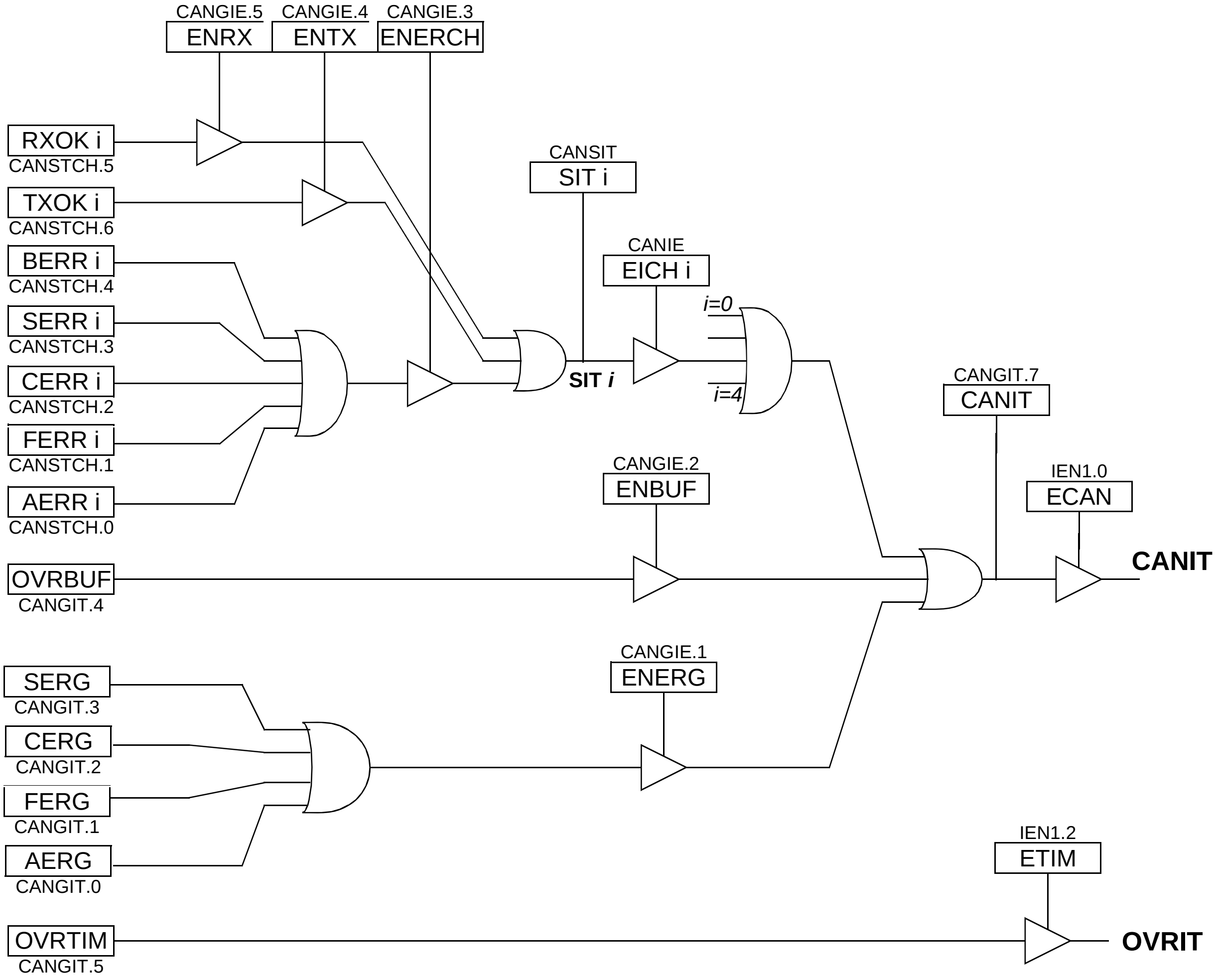


Figure 39. CAN Controller Interrupt Structure



To enable a transmission interrupt:

- Enable General CAN IT in the interrupt system register
- Enable interrupt by message object, EICHi
- Enable transmission interrupt, ENTX

To enable a reception interrupt:

- Enable General CAN IT in the interrupt system register
- Enable interrupt by message object, EICHi
- Enable reception interrupt, ENRX

To enable an interrupt on message object error:

- Enable General CAN IT in the interrupt system register
- Enable interrupt by message object, EICHi
- Enable interrupt on error, ENERCH

To enable an interrupt on general error:

- Enable General CAN IT in the interrupt system register
- Enable interrupt on error, ENERG

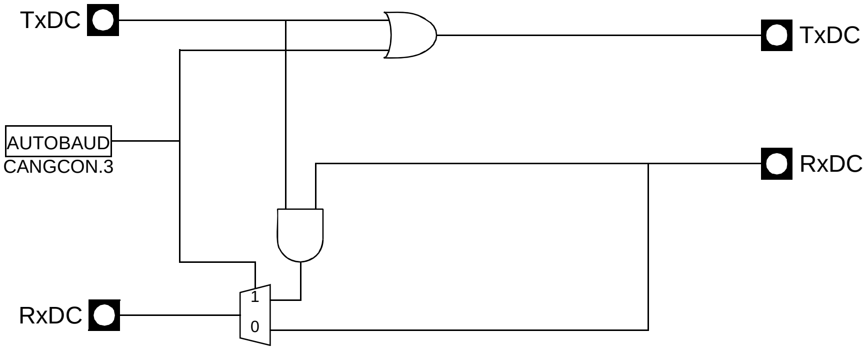
CAN Autobaud and Listening Mode

To activate the Autobaud feature, the AUTOBAUD bit in the CANGCON register must be set. In this mode, the CAN controller is only listening to the line without acknowledging the received messages. It cannot send any message. The error flags are updated. The bit timing can be adjusted until no error occurs (good configuration find).

In this mode, the error counters are frozen.

To go back to the standard mode, the AUTOBAUD bit must be cleared.

Figure 45. Autobaud Mode



Routine Examples

```
1. Init of CAN macro
// Reset the CAN macro
 CANGCON = 01h;
// Disable CAN interrupts
 ECAN   = 0;
 ETIM   = 0;
// Init the Mailbox
 for num_page =0; num_page <4; num_page++
    {
    CANPAGE = num_channel << 4;
    CANCONCH = 00h
    CANSTCH = 00h;
    CANIDT1 = 00h;
    CANIDT2 = 00h;
    CANIDT3 = 00h;
    CANIDT4 = 00h;
    CANIDM1 = 00h;
    CANIDM2 = 00h;
    CANIDM3 = 00h;
    CANIDM4 = 00h;
    for num_data =0; num_data <8; num_data++)
      {
      CANMSG = 00h;
}
}
// Configure the bit timing
 CANBT1 = xxh
 CANBT2 = xxh
 CANBT3 = xxh
```

Table 59. CANTEC Register
CANTEC (S:9Ch Read Only) – CAN Transmit Error Counter

7	6	5	4	3	2	1	0
TEC7	TEC6	TEC5	TEC4	TEC3	TEC2	TEC1	TEC0

Bit Number	Bit Mnemonic	Description
7 - 0	TEC7:0	**Transmit Error Counte**r See Figure 42

Reset Value = 00h

Table 60. CANREC Register
CANREC (S:9Dh Read Only) – CAN Reception Error Counter

7	6	5	4	3	2	1	0
REC7	REC6	REC5	REC4	REC3	REC2	REC1	REC0

Bit Number	Bit Mnemonic	Description
7 - 0	REC7:0	**Reception Error Counter** See Figure 42

Reset Value = 00h

Table 70. CANSTCH Register
CANSTCH (S:B2h) – CAN Message Object Status Register

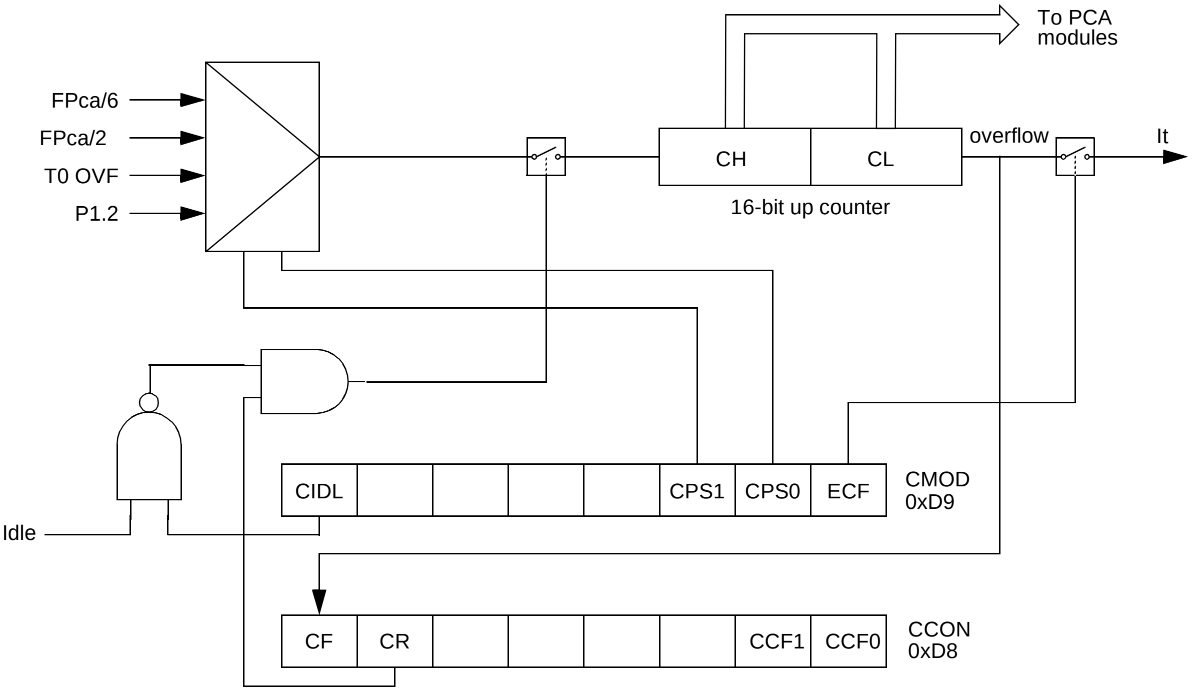
7	6	5	4	3	2	1	0
DLCW	TXOK	RXOK	BERR	SERR	CERR	FERR	AERR

Bit Number	Bit Mnemonic	Description
7	DLCW	**Data Length Code Warning** The incoming message does not have the DLC expected. Whatever the frame type, the DLC field of the CANCONCH register is updated by the received DLC.
6	TXOK	**Transmit OK** The communication enabled by transmission is completed. When the controller is ready to send a frame, if two or more message objects are enabled as producers, the lower index message object (0 to 13) is supplied first. Must be cleared by software. This flag can generate an interrupt.
5	RXOK	**Receive OK** The communication enabled by reception is completed. In the case of two or more message object reception hits, the lower index message object (0 to 13) is updated first. Must be cleared by software. This flag can generate an interrupt.
4	BERR	**bit Error (only in transmission)** The bit value monitored is different from the bit value sent. Exceptions: the monitored recessive bit sent as a dominant bit during the arbitration field and the acknowledge slot detecting a dominant bit during the sending of an error frame. Must be cleared by software. This flag can generate an interrupt.
3	SERR	**Stuff Error** Detection of more than five consecutive bits with the same polarity. Must be cleared by software. This flag can generate an interrupt.
2	CERR	**CRC Error** The receiver performs a CRC check on each destuffed received message from the start of frame up to the data field. If this checking does not match with the destuffed CRC field, a CRC error is set. Must be cleared by software. This flag can generate an interrupt.
1	FERR	**Form Error** The form error results from one or more violations of the fixed form in the following bit fields: CRC delimiter acknowledgment delimiter end_of_frame Must be cleared by software. This flag can generate an interrupt.
0	AERR	**Acknowledgment Error** No detection of the dominant bit in the acknowledge slot. Must be cleared by software. This flag can generate an interrupt.

Note: See Figure 39.

No default value after reset.

Figure 46. PCA Timer/Counter



The CMOD register includes three additional bits associated with the PCA.

- The CIDL bit which allows the PCA to stop during idle mode.
- The ECF bit which when set causes an interrupt and the PCA overflow flag CF in CCON register to be set when the PCA timer overflows.

The CCON register contains the run control bit for the PCA and the flags for the PCA timer and each module.

- The CR bit must be set to run the PCA. The PCA is shut off by clearing this bit.
- The CF bit is set when the PCA counter overflows and an interrupt will be generated if the ECF bit in CMOD register is set. The CF bit can only be cleared by software.
- The CCF0:1 bits are the flags for the modules (CCF0 for module0...) and are set by hardware when either a match or a capture occurs. These flags also can be cleared by software.

The bits SCH0 to SCH2 in ADCON register are used for the analog input channel selection.

Table 102. Selected Analog input

SCH2	SCH1	SCH0	Selected Analog Input
0	0	0	AN0
0	0	1	AN1
0	1	0	AN2
0	1	1	AN3
1	0	0	AN4
1	0	1	AN5
1	1	0	AN6
1	1	1	AN7

Voltage Conversion

When the ADCIN is equals to VAREF the ADC converts the signal to 3FFh (full scale). If the input voltage equals VAGND, the ADC converts it to 000h. Input voltage between VAREF and VAGND are a straight-line linear conversion. All other voltages will result in 3FFh if greater than VAREF and 000h if less than VAGND.

Note that ADCIN should not exceed VAREF absolute maximum range (See section “AC-DC”).

Clock Selection

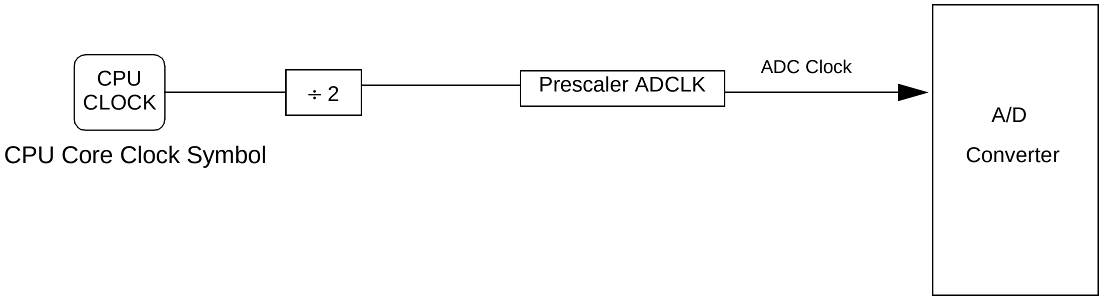
The ADC clock is the same as CPU.

The maximum clock frequency is defined in the DC parmeter for A/D converter. A prescaler is featured (ADCCLK) to generate the ADC clock from the oscillator frequency.

if PRS = 0 then F_{ADC} = F_{periph} / 64

if PRS > 0 then F_{ADC} = F_{periph} / 2 x PRS

Figure 54. A/D Converter Clock



ADC Standby Mode

When the ADC is not used, it is possible to set it in standby mode by clearing bit ADEN in ADCON register. In this mode the power dissipation is reduced.

Table 110. IPL0 Register
IPL0 (S:B8h)
Interrupt Enable Register

7	6	5	4	3	2	1	0
-	PPC	PT2	PS	PT1	PX1	PT0	PX0

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
6	PPC	**PCA Interrupt Priority bit** Refer to PPCH for priority level
5	PT2	**Timer 2 Overflow Interrupt Priority bit** Refer to PT2H for priority level.
4	PS	**Serial Port Priority bit** Refer to PSH for priority level.
3	PT1	**Timer 1 Overflow Interrupt Priority bit** Refer to PT1H for priority level.
2	PX1	**External Interrupt 1 Priority bit** Refer to PX1H for priority level.
1	PT0	**Timer 0 Overflow Interrupt Priority bit** Refer to PT0H for priority level.
0	PX0	**External Interrupt 0 Priority bit** Refer to PX0H for priority level.

Reset Value = X000 0000b
bit addressable

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