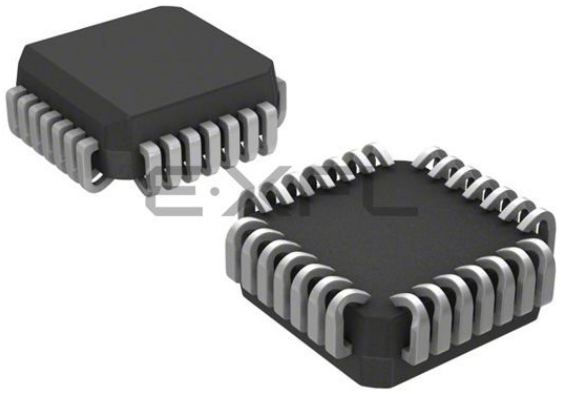

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	80C51
Core Size	8-Bit
Speed	40MHz
Connectivity	CANbus, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	20
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-LCC (J-Lead)
Supplier Device Package	28-PLCC (11.51x11.51)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at89c51cc02ua-sisum

Table 11. SFR Mapping

	0/8[1]	1/9	2/A	3/B	4/C	5/D	6/E	7/F	
F8h	**IPL1** **xxxx x000**	CH 0000 0000	CCAP0H 0000 0000	CCAP1H 0000 0000					FFh
F0h	**B** **0000 0000**		ADCLK xxx0 0000	ADCON x000 0000	ADDL 0000 0000	ADDH 0000 0000	ADCF 0000 0000	IPH1 xxxx x000	F7h
E8h	**IEN1** **xxxx x000**	CL 0000 0000	CCAP0L 0000 0000	CCAP1L 0000 0000					EFh
E0h	**ACC** **0000 0000**								E7h
D8h	**CCON** **0000 0000**	CMOD 0xxx x000	CCAPM0 x000 0000	CCAPM1 x000 0000					DFh
D0h	**PSW** **0000 0000**	FCON 0000 0000	EECON xxxx xx00						D7h
C8h	**T2CON** 0000 0000	T2MOD xxxx xx00	RCAP2L 0000 0000	RCAP2H 0000 0000	TL2 0000 0000	TH2 0000 0000		CANEN xxxx 0000	CFh
C0h	**P4** **xxxx xx11**	CANGIE 1100 0000		CANIE 1111 0000	CANIDM1 xxxx xxxx	CANIDM2 xxxx xxxx	CANIDM3 xxxx xxxx	CANIDM4 xxxx xxxx	C7h
B8h	**IPL0** **x000 0000**	SADEN 0000 0000		CANSIT xxxx 0000	CANIDT1 xxxx xxxx	CANIDT2 xxxx xxxx	CANIDT3 xxxx xxxx	CANIDT4 xxxx xxxx	BFh
B0h	**P3** **1111 1111**	CANPAGE 1100 0000	CANSTCH xxxx xxxx	CANCONCH xxxx xxxx	CANBT1 xxxx xxxx	CANBT2 xxxx xxxx	CANBT3 xxxx xxxx	IPH0 x000 0000	B7h
A8h	**IEN0** **0000 0000**	SADDR 0000 0000	CANGSTA 1010 0000	CANGCON 0000 0000	CANTIML 0000 0000	CANTIMH 0000 0000	CANSTMPL xxxx xxxx	CANSTMPH xxxx xxxx	AFh
A0h	**P2** **xxxx xx11**	CANTCON 0000 0000	AUXR1[2] xxxx 00x0	CANMSG xxxx xxxx	CANTTCL 0000 0000	CANTTCH 0000 0000	WDTRST 1111 1111	WDTPRG xxxx x000	A7h
98h	**SCON** **0000 0000**	SBUF 0000 0000		CANGIT 0x00 0000	CANTEC 0000 0000	CANREC 0000 0000			9Fh
90h	**P1** **1111 1111**								97h
88h	**TCON** **0000 0000**	TMOD 0000 0000	TL0 0000 0000	TL1 0000 0000	TH0 0000 0000	TH1 0000 0000		CKCON 0000 0000	8Fh
80h		SP 0000 0111	DPL 0000 0000	DPH 0000 0000				PCON 00x1 0000	87h
	0/8[1]	1/9	2/A	3/B	4/C	5/D	6/E	7/F	

Reserved

Notes: 1. These registers are bit-addressable.
Sixteen addresses in the SFR space are both byte-addressable and bit-addressable. The bit-addressable SFRs are those whose address ends in 0 and 8. The bit addresses, in this area, are 0x80 through to 0xFF.
2. AUXR1 bit ENBOOT is initialized with the content of the BLJB bit inverted.

Clock

The T89C51CC02 core needs only 6 clock periods per machine cycle. This feature, called “X2”, provides the following advantages:

- Divides frequency crystals by 2 (cheaper crystals) while keeping the same CPU power.
- Saves power consumption while keeping the same CPU power (oscillator power saving).
- Saves power consumption by dividing dynamic operating frequency by 2 in operating and idle modes.
- Increases CPU power by 2 while keeping the same crystal frequency.

In order to keep the original C51 compatibility, a divider-by-2 is inserted between the XTAL1 signal and the main clock input of the core (phase generator). This divider may be disabled by the software.

An extra feature is available to start after Reset in the X2 Mode. This feature can be enabled by a bit X2B in the Hardware Security Byte. This bit is described in the section ’In-System Programming’.

Description

The X2 bit in the CKCON register (See Table 12) allows switching from 12 clock cycles per instruction to 6 clock cycles and vice versa. At reset, the standard speed is activated (STD mode).

Setting this bit activates the X2 feature (X2 Mode) for the CPU Clock only (See Figure 3).

The Timers 0, 1 and 2, Uart, PCA, watchdog or CAN switch in X2 Mode only if the corresponding bit is cleared in the CKCON register.

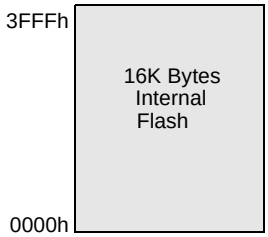
The clock for the whole circuit and peripheral is first divided by two before being used by the CPU core and peripherals. This allows any cyclic ratio to be accepted on the XTAL1 input. In X2 Mode, as this divider is bypassed, the signals on XTAL1 must have a cyclic ratio between 40 to 60%. Figure 3. shows the clock generation block diagram. The X2 bit is validated on the XTAL1 ÷ 2 rising edge to avoid glitches when switching from the X2 to the STD mode. Figure 4 shows the mode switching waveforms.

Program/Code Memory

The T89C51CC02 implement 16K Bytes of on-chip program/code memory.

The Flash memory increases EPROM and ROM functionality by in-circuit electrical erasure and programming. Thanks to the internal charge pump, the high voltage needed for programming or erasing Flash cells is generated on-chip using the standard V_{DD} voltage. Thus, the Flash memory can be programmed using only one voltage and allows In-System Programming (ISP). Hardware programming mode is also available using specific programming tool.

Figure 12. Program/Code Memory Organization



Flash Memory Architecture

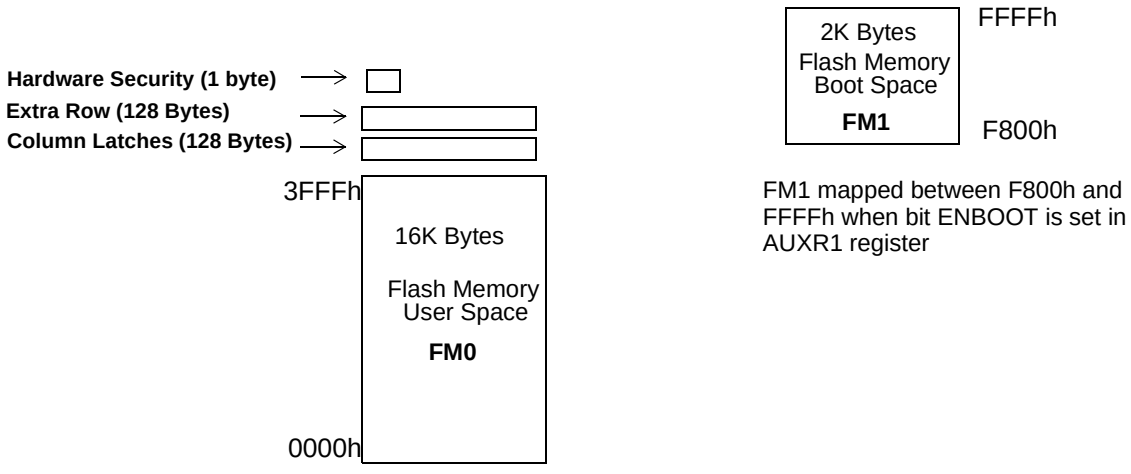
T89C51CC02 features two on-chip Flash memories:

- Flash memory FM0:
  containing 16K Bytes of program memory (user space) organized into 128 bytes pages,
- Flash memory FM1:
  2K Bytes for boot loader and Application Programming Interfaces (API).

The FM0 can be program by both parallel programming and Serial ISP whereas FM1 supports only parallel programming by programmers. The ISP mode is detailed in the 'In-System Programming' section.

All Read/Write access operations on Flash memory by user application are managed by a set of API described in the 'In-System Programming' section.

Figure 13. Flash Memory Architecture



FM0 Memory Architecture

The Flash memory is made up of 4 blocks (See Figure 13):

1. The memory array (user space) 16K Bytes
2. The Extra Row
3. The Hardware security bits
4. The column latch registers

User Space

This space is composed of a 16K Bytes Flash memory organized in 128 pages of 128 Bytes. It contains the user's application code.

Extra Row (XRow)

This row is a part of FM0 and has a size of 128 Bytes. The extra row may contain information for boot loader usage.

Hardware Security Byte

The Hardware security Byte space is a part of FM0 and has a size of 1 byte.
The 4 MSB can be read/written by software, the 4 LSB can only be read by software and written by hardware in parallel mode.

Column Latches

The column latches, also part of FM0, have a size of full page (128 Bytes).
The column latches are the entrance buffers of the three previous memory locations (user array, XROW and Hardware security byte).

Cross Flash Memory Access Description

The FM0 memory can be programmed as describe on Table 21. Programming FM0 from FM0 is impossible.

The FM1 memory can be program only by parallel programming.

Table 21 show all software Flash access allowed.

Table 21. Cross Flash Memory Access

Code executing from		Action	FM0 (user Flash)	FM1 (boot Flash)
	FM0 (user Flash)	Read	ok	-
		Load column latch	ok	-
		Write	-	-
	FM1 (boot Flash)	Read	ok	ok
		Load column latch	ok	-
		Write	ok	-

Registers

Table 25. FCON Register
FCON Register FCON (S:D1h)
Flash Control Register

7	6	5	4	3	2	1	0
FPL3	**FPL2**	**FPL1**	**FPL0**	**FPS**	**FMOD1**	**FMOD0**	**FBUSY**

Bit Number	Bit Mnemonic	Description
7 - 4	FPL3:0	**Programming Launch Command bits** Write 5Xh followed by AXh to launch the programming according to FMOD1:0. (See Table 23.)
3	FPS	**Flash Map Program Space** Set to map the column latch space in the data memory space. Clear to re-map the data memory space.
2 - 1	FMOD1:0	**Flash Mode** See Table 22 or Table 23.
0	FBUSY	**Flash Busy** Set by hardware when programming is in progress. Clear by hardware when programming is done. Can not be changed by software.

Reset Value = 0000 0000b

Figure 22. UART Timing in Mode 1

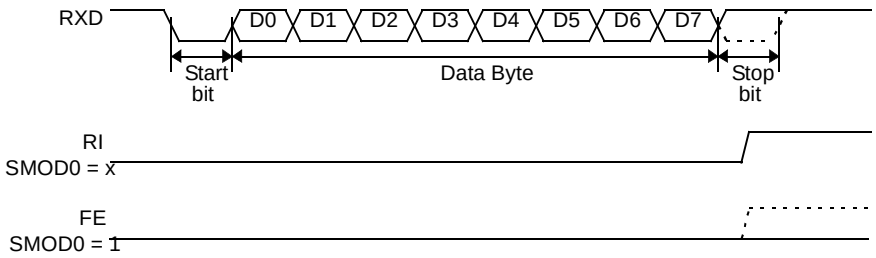
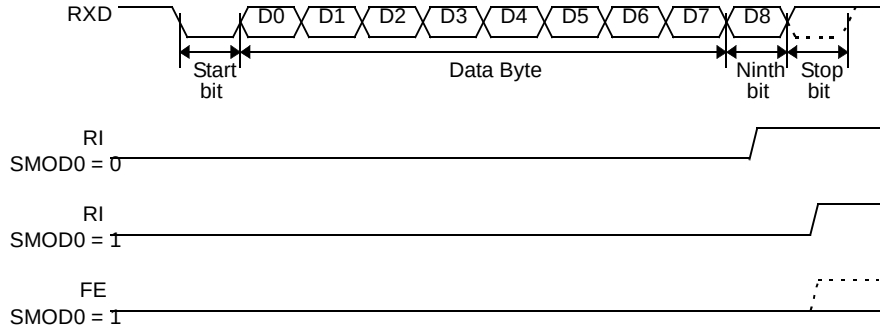


Figure 23. UART Timing in Modes 2 and 3



Automatic Address Recognition

The automatic address recognition feature is enabled when the multiprocessor communication feature is enabled (SM2 bit in SCON register is set).

Implemented in the hardware, automatic address recognition enhances the multiprocessor communication feature by allowing the serial port to examine the address of each incoming command frame. Only when the serial port recognizes its own address will the receiver set the RI bit in the SCON register to generate an interrupt. This ensures that the CPU is not interrupted by command frames addressed to other devices.
If necessary, the user can enable the automatic address recognition feature in mode 1. In this configuration, the stop bit takes the place of the ninth data bit. bit RI is set only when the received command frame address matches the device's address and is terminated by a valid stop bit.

To support automatic address recognition, a device is identified by a given address and a broadcast address.

Note: The multiprocessor communication and automatic address recognition features cannot be enabled in mode 0 (i.e. setting SM2 bit in SCON register in mode 0 has no effect).

Given Address

Each device has an individual address that is specified in the SADDR register; the SADEN register is a mask byte that contains don't-care bits (defined by zeros) to form the device's given address. The don't-care bits provide the flexibility to address one or more slaves at a time. The following example illustrates how a given address is formed. To address a device by its individual address, the SADEN mask byte must be `1111 1111b`.
For example:

```
SADDR0101 0110b
SADEN1111 1100b
Given0101 01XXb
```

Registers

Table 33. SCON Register

SCON (S:98h)
Serial Control Register

7	6	5	4	3	2	1	0
FE/SM0	**SM1**	**SM2**	**REN**	**TB8**	**RB8**	**TI**	**RI**

Bit Number	Bit Mnemonic	Description
7	FE	**Framing Error bit (SMOD0 = 1**) Clear to reset the error state, not cleared by a valid stop bit. Set by hardware when an invalid stop bit is detected.
	SM0	**Serial port Mode bit 0 (SMOD0 = 0)** Refer to SM1 for serial port mode selection.
6	SM1	**Serial port Mode bit 1** SM0 SM1 Mode Baud Rate 0 0 Shift Register F_{XTAL}/12 (or F_{XTAL}/6 in mode X2) 0 1 8-bit UART Variable 1 0 9bit UART F_{XTAL}/64 or F_{XTAL}/32 1 1 9bit UART Variable
5	SM2	**Serial port Mode 2 bit/Multiprocessor Communication Enable bit** Clear to disable multiprocessor communication feature. Set to enable multiprocessor communication feature in mode 2 and 3.
4	REN	**Reception Enable bit** Clear to disable serial reception. Set to enable serial reception.
3	TB8	**Transmitter bit 8/Ninth bit to Transmit in Modes 2 and 3** Clear to transmit a logic 0 in the 9th bit. Set to transmit a logic 1 in the 9th bit.
2	RB8	**Receiver bit 8/Ninth bit Received in Modes 2 and 3** Cleared by hardware if 9th bit received is a logic 0. Set by hardware if 9th bit received is a logic 1.
1	TI	**Transmit Interrupt Flag** Clear to acknowledge interrupt. Set by hardware at the end of the 8th bit time in mode 0 or at the beginning of the stop bit in the other modes.
0	RI	**Receive Interrupt Flag** Clear to acknowledge interrupt. Set by hardware at the end of the 8th bit time in mode 0, See Figure 22. and Figure 23. in the other modes.

Reset Value = 0000 0000b
bit addressable

Table 37. PCON Register
PCON (S:87h)
Power Control Register

7	6	5	4	3	2	1	0
SMOD1	**SMOD0**	**-**	**POF**	**GF1**	**GF0**	**PD**	**IDL**

Bit Number	Bit Mnemonic	Description
7	SMOD1	**Serial port Mode bit 1** Set to select double baud rate in mode 1, 2 or 3.
6	SMOD0	**Serial port Mode bit 0** Clear to select SM0 bit in SCON register. Set to select FE bit in SCON register.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	POF	**Power-off Flag** Clear to recognize next reset type. Set by hardware when V_{CC} rises from 0 to its nominal voltage. Can also be set by software.
3	GF1	**General purpose Flag** Cleared by user for general purpose usage. Set by user for general purpose usage.
2	GF0	**General purpose Flag** Cleared by user for general purpose usage. Set by user for general purpose usage.
1	PD	**Power-down Mode bit** Cleared by hardware when reset occurs. Set to enter power-down mode.
0	IDL	**Idle Mode bit** Clear by hardware when interrupt or reset occurs. Set to enter idle mode.

Reset Value = 00X1 0000b
Not bit addressable

Timer 2

The T89C51CC02 Timer 2 is compatible with Timer 2 in the 80C52.

It is a 16-bit timer/counter: the count is maintained by two eightbit timer registers, TH2 and TL2 that are cascade-connected. It is controlled by T2CON register (See Table 45) and T2MOD register (See Table 46). Timer 2 operation is similar to Timer 0 and Timer 1. C/$\overline{T2}$ selects $F_{T2\ clock}$/6 (timer operation) or external pin T2 (counter operation) as timer clock. Setting TR2 allows TL2 to be incremented by the selected input.

Timer 2 includes the following enhancements:

- Auto-reload mode (up or down counter)
- Programmable clock-output

Auto-Reload Mode

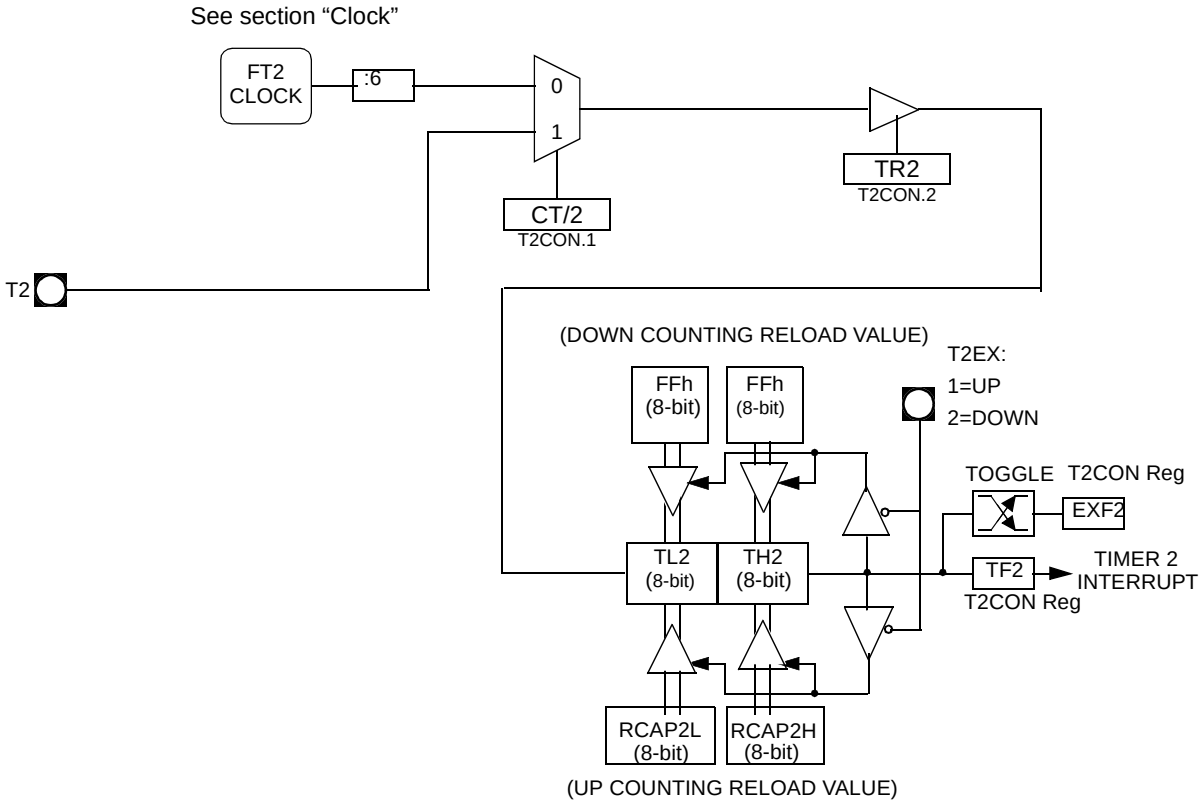
The auto-reload mode configures Timer 2 as a 16-bit timer or event counter with automatic reload. This feature is controlled by the DCEN bit in T2MOD register (See Table 45). Setting the DCEN bit enables Timer 2 to count up or down as shown in Figure 29. In this mode the T2EX pin controls the counting direction.

When T2EX is high, Timer 2 counts up. Timer overflow occurs at FFFFh which sets the TF2 flag and generates an interrupt request. The overflow also causes the 16-bit value in RCAP2H and RCAP2L registers to be loaded into the timer registers TH2 and TL2.

When T2EX is low, Timer 2 counts down. Timer underflow occurs when the count in the timer registers TH2 and TL2 equals the value stored in RCAP2H and RCAP2L registers. The underflow sets TF2 flag and reloads FFFFh into the timer registers.

The EXF2 bit toggles when Timer 2 overflow or underflow, depending on the direction of the count. EXF2 does not generate an interrupt. This bit can be used to provide 17-bit resolution.

Figure 29. Auto-Reload Mode Up/Down Counter



fields against the fixed format and the frame size. Errors detected by frame checks are designated "format errors".

- ACK Errors
  As already mentioned frames received are acknowledged by all receivers through positive acknowledgement. If no acknowledgement is received by the transmitter of the message an ACK error is indicated.

Error at Bit Level

- Monitoring
  The ability of the transmitter to detect errors is based on the monitoring of bus signals. Each node which transmits also observes the bus level and thus detects differences between the bit sent and the bit received. This permits reliable detection of global errors and errors local to the transmitter.
- Bit Stuffing
  The coding of the individual bits is tested at bit level. The bit representation used by CAN is "Non Return to Zero (NRZ)" coding, which guarantees maximum efficiency in bit coding. The synchronization edges are generated by means of bit stuffing.

Error Signalling

If one or more errors are discovered by at least one node using the above mechanisms, the current transmission is aborted by sending an "error flag". This prevents other nodes accepting the message and thus ensures the consistency of data throughout the network. After transmission of an erroneous message that has been aborted, the sender automatically re-attempts transmission.

CAN Controller Description

The CAN controller accesses are made through SFR.
Several operations are possible by SFR:

- arithmetic and logic operations, transfers and program control (SFR is accessible by direct addressing).
- 4 independent message objects are implemented, a pagination system manages their accesses.

Any message object can be programmed in a reception buffer block (even non-consecutive buffers). For the reception of defined messages one or several receiver message objects can be masked without participating in the buffer feature. An IT is generated when the buffer is full. The frames following the buffer-full interrupt will not be taken into account until at least one of the buffer message objects is re-enabled in reception. Higher priority of a message object for reception or transmission is given to the lower message object number.

The programmable 16-bit Timer (CANTIMER) is used to stamp each received and sent message in the CANSTMP register. This timer starts counting as soon as the CAN controller is enabled by the ENA bit in the CANGCON register.

The Time Trigger Communication (TTC) protocol is supported by the T89C51CC02.

To enable an interrupt on Buffer-full condition:

- Enable General CAN IT in the interrupt system register
- Enable interrupt on Buffer full, ENBUF

To enable an interrupt when Timer overruns:

- Enable Overrun IT in the interrupt system register

When an interrupt occurs, the corresponding message object bit is set in the SIT register.

To acknowledge an interrupt, the corresponding CANSTCH bits (RXOK, TXOK,...) or CANGIT bits (OVRTIM, OVRBUF,...), must be cleared by the software application.

When the CAN node is in transmission and detects a Form Error in its frame, a bit Error will also be raised. Consequently, two consecutive interrupts can occur, both due to the same error.

When a message object error occurs and is set in CANSTCH register, no general error are set in CANGIE register.

Fault Confinement

With respect to fault confinement, a unit may be in one of the three following status:

- Error active
- Error passive
- Bus off

An error active unit takes part in bus communication and can send an active error frame when the CAN macro detects an error.

An error passive unit cannot send an active error frame. It takes part in bus communication, but when an error is detected, a passive error frame is sent. Also, after a transmission, an error passive unit will wait before initiating further transmission.

A bus off unit is not allowed to have any influence on the bus.

For fault confinement, two error counters (TEC and REC) are implemented.

See CAN Specification for details on Fault confinement.

Figure 42. Line Error Mode

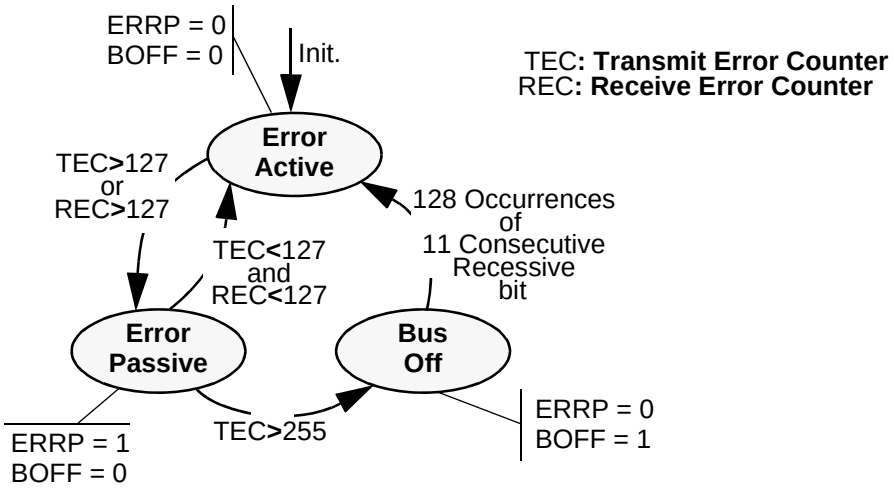


Table 74. CANIDT1 for V2.0 part A

CANIDT4 for V2.0 part A (S:BFh)
CAN Identifier Tag Registers 4

7	6	5	4	3	2	1	0
-	-	-	-	-	RTRTAG	-	RB0TAG

Bit Number	Bit Mnemonic	Description
7 - 3	-	**Reserved** The values read from these bits are indeterminate. Do not set these bits.
2	RTRTAG	Remote transmission request tag value.
1	-	**Reserved** The values read from this bit are indeterminate. Do not set these bit.
0	RB0TAG	Reserved bit 0 tag value.

No default value after reset.

Table 75. CANIDT2Register for V2.0 part A
CANIDT1 for V2.0 Part B (S:BCh)
CAN Identifier Tag Registers 1

7	6	5	4	3	2	1	0
IDT 28	IDT 27	IDT 26	IDT 25	IDT 24	IDT 23	IDT 22	IDT 21

Bit Number	Bit Mnemonic	Description
7 - 0	IDT28:21	**IDentifier Tag Value** See Figure 43.

No default value after reset.

Table 76. CANIDT2 Register for V2.0 Part B
CANIDT2 for V2.0 Part B (S:BDh)
CAN Identifier Tag Registers 2

7	6	5	4	3	2	1	0
IDT 20	IDT 19	IDT 18	IDT 17	IDT 16	IDT 15	IDT 14	IDT 13

Bit Number	Bit Mnemonic	Description
7 - 0	IDT20:13	**IDentifier Tag Value** See Figure 43.

No default value after reset.

Table 82. CANIDM4 Register for V2.0 part A
CANIDM4 for V2.0 part A (S:C7h)
CAN Identifier Mask Registers 4

7	6	5	4	3	2	1	0
-	-	-	-	-	RTRMSK	-	IDEMSK

Bit Number	Bit Mnemonic	Description
7 - 3	-	**Reserved** The values read from these bits are indeterminate. Do not set these bits.
2	RTRMSK	**Remote transmission request Mask Value** 0 - comparison true forced. 1 - bit comparison enabled.
1	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
0	IDEMSK	**IDentifier Extension Mask Value** 0 - comparison true forced. 1 - bit comparison enabled.

Note: The ID Mask is only used for reception.

No default value after reset.

Table 83. CANIDM1 Register for V2.0 Part B
CANIDM1 for V2.0 Part B (S:C4h)
CAN Identifier Mask Registers 1

7	6	5	4	3	2	1	0
IDMSK 28	IDMSK 27	IDMSK 26	IDMSK 25	IDMSK 24	IDMSK 23	IDMSK 22	IDMSK 21

Bit Number	Bit Mnemonic	Description
7 - 0	IDMSK28:21	**IDentifier Mask Value** 0 - comparison true forced. 1 - bit comparison enabled. See Figure 43.

Note: The ID Mask is only used for reception.

No default value after reset.

16-bit Software Timer Mode

The PCA modules can be used as software timers by setting both the ECOM and MAT bits in the modules CCAPMn register. The PCA timer will be compared to the module's capture registers and when a match occurs an interrupt will occur if the CCFn (CCON SFR) and the ECCFn (CCAPMn SFR) bits for the module are both set.

Figure 49. PCA 16-bit Software Timer and High Speed Output Mode

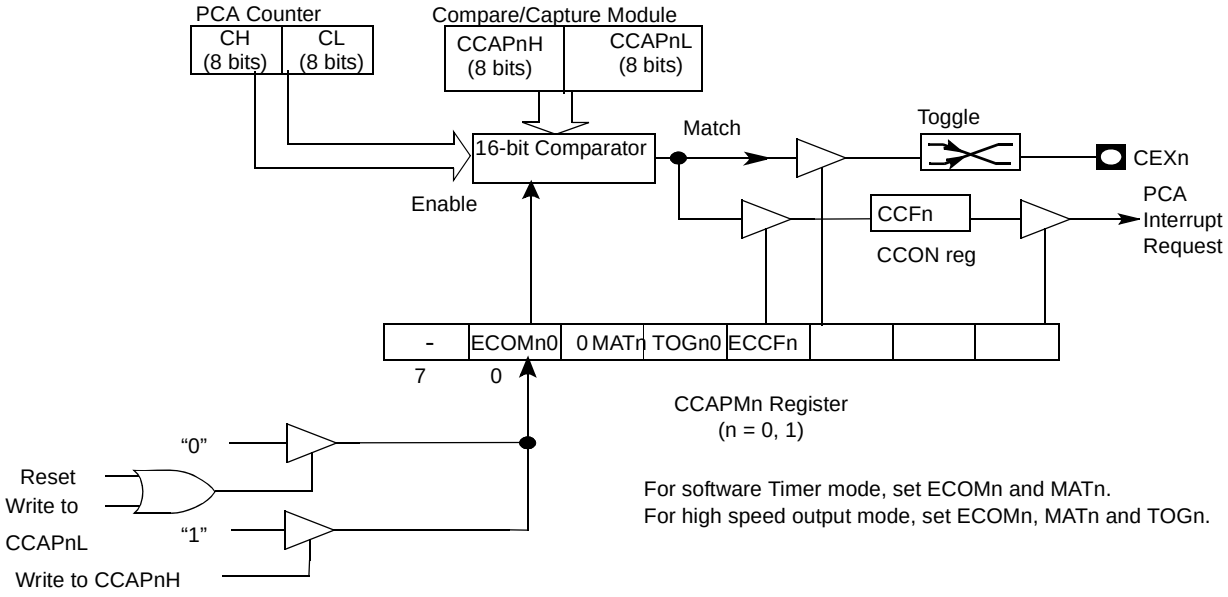


Figure 52. ADC Description

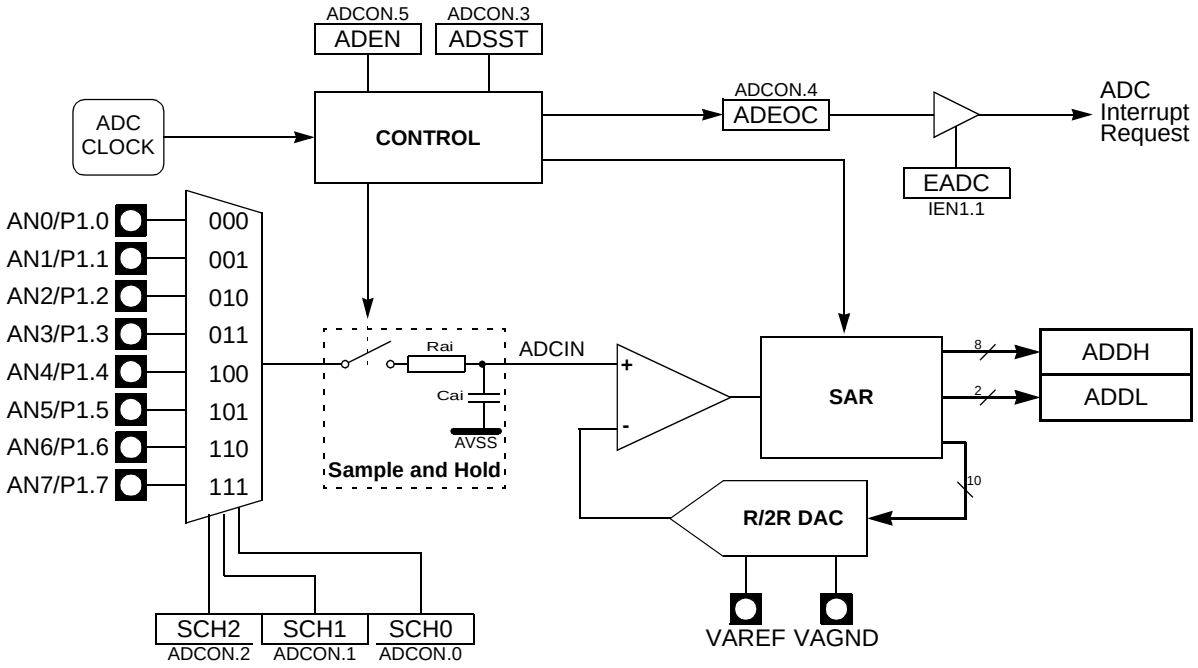
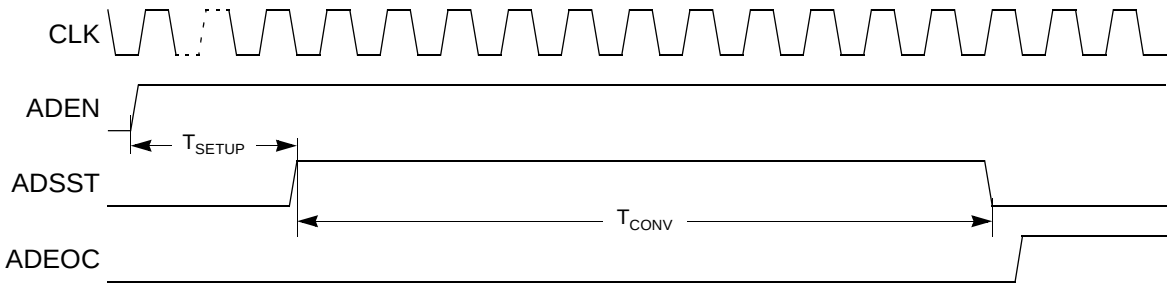


Figure 53 shows the timing diagram of a complete conversion. For simplicity, the figure depicts the waveforms in idealized form and do not provide precise timing information. For ADC characteristics and timing parameters refer to the section “AC Characteristics” of this datasheet.

Figure 53. Timing Diagram



Note: Tsetup min, see the AC Parameter for A/D conversion.
Tconv = 11 clock ADC = 1sample and hold + 10-bit conversion
The user must ensure that Tsetup time between setting ADEN and the start of the first conversion.

ADC Converter Operation

A start of single A/D conversion is triggered by setting bit ADSST (ADCON.3).

After completion of the A/D conversion, the ADSST bit is cleared by hardware.

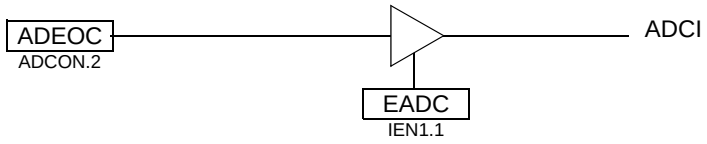
The end-of-conversion flag ADEOC (ADCON.4) is set when the value of conversion is available in ADDH and ADDL, it must be cleared by software. If the bit EADC (IEN1.1) is set, an interrupt occur when flag ADEOC is set (See Figure 55). Clear this flag for re-arming the interrupt.

Note: Always leave Tsetup time before starting a conversion unless ADEN is permanently high. In this case one should wait Tsetup only before the first conversion

IT ADC Management

An interrupt end-of-conversion will occurs when the bit ADEOC is activated and the bit EADC is set. For re-arming the interrupt the bit ADEOC must be cleared by software.

Figure 55. ADC interrupt structure



Routine Examples

```
1. Configure P1.2 and P1.3 in ADC channels
// configure channel P1.2 and P1.3 for ADC
 ADCF = 0Ch

// Enable the ADC
 ADCON = 20h
2. Start a standard conversion
// The variable 'channel' contains the channel to convert
// The variable 'value_converted' is an unsigned int
// Clear the field SCH[2:0]
 ADCON &= F8h
// Select channel
 ADCON |= channel
// Start conversion in standard mode
 ADCON |= 08h
// Wait flag End of conversion
 while((ADCON & 01h)!= 01h)
// Clear the End of conversion flag
 ADCON &= EFh
// read the value
 value_converted = (ADDH << 2)+(ADDL)

3. Start a precision conversion (need interrupt ADC)
// The variable 'channel' contains the channel to convert
// Enable ADC
 EADC = 1
// clear the field SCH[2:0]
 ADCON &= F8h
// Select the channel
 ADCON |= channel
// Start conversion in precision mode
 ADCON |= 48h
```

Note: To enable the ADC interrupt: EA = 1

Table 111. IPL1 Register
IPL1 (S:F8h)
Interrupt Priority Low Register 1

7	6	5	4	3	2	1	0
-	-	-	-		POVRL	PADCL	PCANL

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
6	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
3	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
2	POVRL	**Timer Overrun Interrupt Priority Level Less Significant bit** Refer to PI2CH for priority level.
1	PADCL	**ADC Interrupt Priority Level Less Significant bit** Refer to PSPIH for priority level.
0	PCANL	**CAN Interrupt Priority Level Less Significant bit** Refer to PKBH for priority level.

Reset Value = XXXX X000b
bit addressable

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