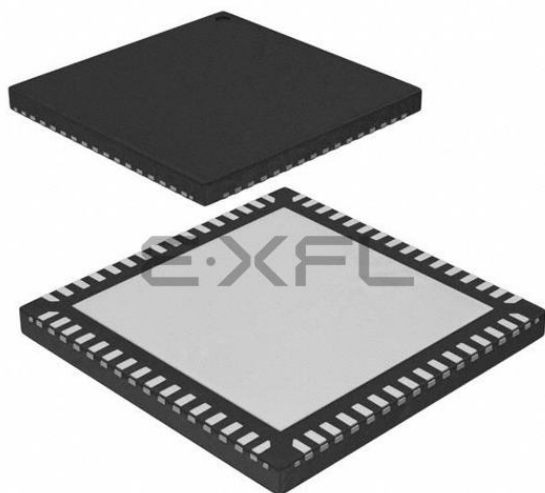




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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I ² C, IrDA, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, LCD, POR, PWM, WDT
Number of I/O	56
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.98V ~ 3.8V
Data Converters	A/D 8x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32wg840f256-qfn64t

process and close to automatic transfers. Automatic recognition of slave addresses is provided in all energy modes.

2.1.11 Universal Synchronous/Asynchronous Receiver/Transmitter (USART)

The Universal Synchronous Asynchronous serial Receiver and Transmitter (USART) is a very flexible serial I/O module. It supports full duplex asynchronous UART communication as well as RS-485, SPI, MicroWire and 3-wire. It can also interface with ISO7816 SmartCards, IrDA and I2S devices.

2.1.12 Pre-Programmed UART Bootloader

The bootloader presented in application note AN0003 is pre-programmed in the device at factory. Auto-baud and destructive write are supported. The autobaud feature, interface and commands are described further in the application note.

2.1.13 Low Energy Universal Asynchronous Receiver/Transmitter (LEUART)

The unique LEUART[™], the Low Energy UART, is a UART that allows two-way UART communication on a strict power budget. Only a 32.768 kHz clock is needed to allow UART communication up to 9600 baud/s. The LEUART includes all necessary hardware support to make asynchronous serial communication possible with minimum of software intervention and energy consumption.

2.1.14 Timer/Counter (TIMER)

The 16-bit general purpose Timer has 3 compare/capture channels for input capture and compare/Pulse-Width Modulation (PWM) output. TIMER0 also includes a Dead-Time Insertion module suitable for motor control applications.

2.1.15 Real Time Counter (RTC)

The Real Time Counter (RTC) contains a 24-bit counter and is clocked either by a 32.768 kHz crystal oscillator, or a 32.768 kHz RC oscillator. In addition to energy modes EM0 and EM1, the RTC is also available in EM2. This makes it ideal for keeping track of time since the RTC is enabled in EM2 where most of the device is powered down.

2.1.16 Backup Real Time Counter (BURTC)

The Backup Real Time Counter (BURTC) contains a 32-bit counter and is clocked either by a 32.768 kHz crystal oscillator, a 32.768 kHz RC oscillator or a 1 kHz ULFRCO. The BURTC is available in all Energy Modes and it can also run in backup mode, making it operational even if the main power should drain out.

2.1.17 Low Energy Timer (LETIMER)

The unique LETIMER[™], the Low Energy Timer, is a 16-bit timer that is available in energy mode EM2 in addition to EM1 and EM0. Because of this, it can be used for timing and output generation when most of the device is powered down, allowing simple tasks to be performed while the power consumption of the system is kept at an absolute minimum. The LETIMER can be used to output a variety of waveforms with minimal software intervention. It is also connected to the Real Time Counter (RTC), and can be configured to start counting on compare matches from the RTC.

2.1.18 Pulse Counter (PCNT)

The Pulse Counter (PCNT) can be used for counting pulses on a single input or to decode quadrature encoded inputs. It runs off either the internal LFACLK or the PCNTn_S0IN pin as external clock source. The module may operate in energy mode EM0 – EM3.

3.3.2 Environmental

Table 3.3. Environmental

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V _{ESDHBM}	ESD (Human Body Model HBM)	T _{AMB} =25°C			1000	V
V _{ESDCDM}	ESD (Charged Device Model, CDM)	T _{AMB} =25°C			500	V

Latch-up sensitivity passed: $\pm 100 \text{ mA}/1.5 \times V_{\text{SUPPLY}}(\text{max})$ according to JEDEC JESD 78 method Class II, 85°C.

3.4 Current Consumption

Table 3.4. Current Consumption

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I _{EM0}	EM0 current. No prescaling. Running prime number calculation code from Flash. (Production test condition = 14 MHz)	48 MHz HFXO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =25°C		225	236	μA/ MHz
		48 MHz HFXO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =85°C		225		μA/ MHz
		28 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =25°C		226	238	μA/ MHz
		28 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =85°C		227		μA/ MHz
		21 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =25°C		228	240	μA/ MHz
		21 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =85°C		229		μA/ MHz
		14 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =25°C		230	243	μA/ MHz
		14 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =85°C		231		μA/ MHz
		11 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =25°C		232	245	μA/ MHz
		11 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =85°C		233		μA/ MHz
		6.6 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =25°C		238	250	μA/ MHz
		6.6 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =85°C		238		μA/ MHz

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		1.2 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$, $T_{AMB}=25^{\circ}\text{C}$		271	286	$\mu\text{A}/\text{MHz}$
		1.2 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$, $T_{AMB}=85^{\circ}\text{C}$		275		$\mu\text{A}/\text{MHz}$
I_{EM1}	EM1 current (Production test condition = 14 MHz)	48 MHz HFXO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$, $T_{AMB}=25^{\circ}\text{C}$		63	75	$\mu\text{A}/\text{MHz}$
		48 MHz HFXO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$, $T_{AMB}=85^{\circ}\text{C}$		65	76	$\mu\text{A}/\text{MHz}$
		28 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$, $T_{AMB}=25^{\circ}\text{C}$		64	75	$\mu\text{A}/\text{MHz}$
		28 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$, $T_{AMB}=85^{\circ}\text{C}$		65	77	$\mu\text{A}/\text{MHz}$
		21 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$, $T_{AMB}=25^{\circ}\text{C}$		65	76	$\mu\text{A}/\text{MHz}$
		21 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$, $T_{AMB}=85^{\circ}\text{C}$		66	78	$\mu\text{A}/\text{MHz}$
		14 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$, $T_{AMB}=25^{\circ}\text{C}$		67	79	$\mu\text{A}/\text{MHz}$
		14 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$, $T_{AMB}=85^{\circ}\text{C}$		68	82	$\mu\text{A}/\text{MHz}$
		11 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$, $T_{AMB}=25^{\circ}\text{C}$		68	81	$\mu\text{A}/\text{MHz}$
		11 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$, $T_{AMB}=85^{\circ}\text{C}$		70	83	$\mu\text{A}/\text{MHz}$
		6.6 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$, $T_{AMB}=25^{\circ}\text{C}$		74	87	$\mu\text{A}/\text{MHz}$
		6.6 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$, $T_{AMB}=85^{\circ}\text{C}$		76	89	$\mu\text{A}/\text{MHz}$
		1.2 MHz HFRCO. all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$, $T_{AMB}=25^{\circ}\text{C}$		106	120	$\mu\text{A}/\text{MHz}$
		1.2 MHz HFRCO. all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$, $T_{AMB}=85^{\circ}\text{C}$		112	129	$\mu\text{A}/\text{MHz}$
I_{EM2}	EM2 current	EM2 current with RTC prescaled to 1 Hz, 32.768 kHz LFRCO, $V_{DD}=3.0\text{ V}$, $T_{AMB}=25^{\circ}\text{C}$		0.95 ¹	1.7 ¹	μA

Figure 3.3. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 21MHz

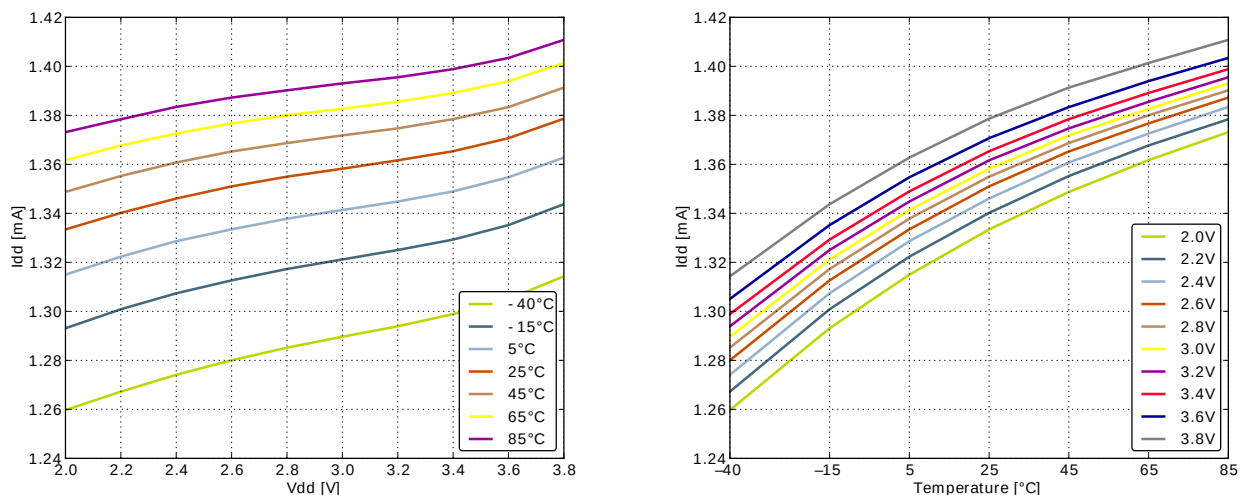
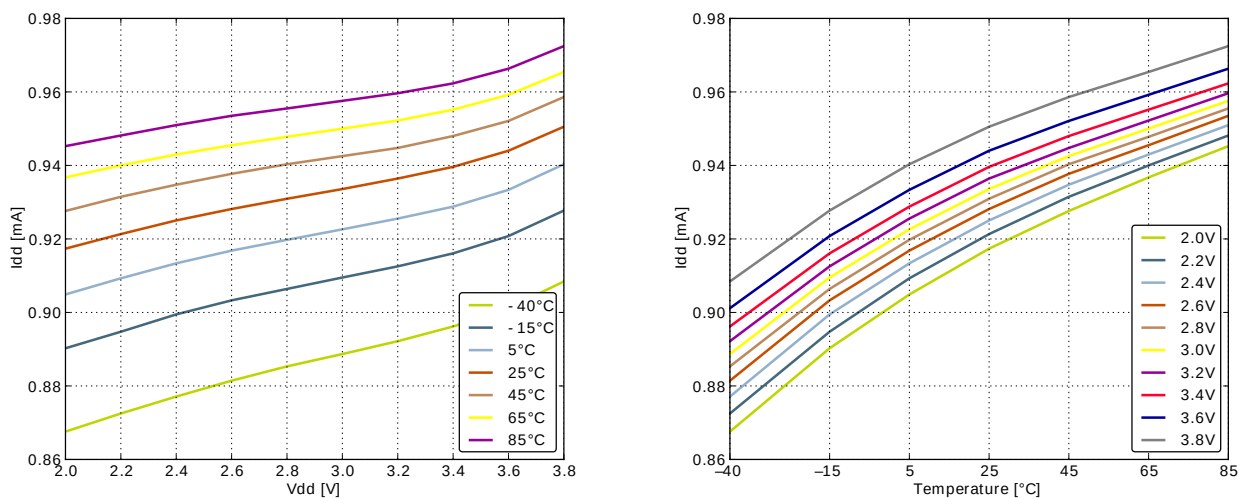


Figure 3.4. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 14MHz



3.6 Power Management

The EFM32WG requires the AVDD_x, VDD_DREG and IOVDD_x pins to be connected together (with optional filter) at the PCB level. For practical schematic recommendations, please see the application note, "AN0002 EFM32 Hardware Design Considerations".

Table 3.6. Power Management

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V _{BODextthr-}	BOD threshold on falling external supply voltage		1.74		1.96	V
V _{BODextthr+}	BOD threshold on rising external supply voltage			1.85	1.98	V
V _{PORthr+}	Power-on Reset (POR) threshold on rising external supply voltage				1.98	V
t _{RESET}	Delay from reset is released until program execution starts	Applies to Power-on Reset, Brown-out Reset and pin reset.		163		μs
C _{DECOUPLE}	Voltage regulator decoupling capacitor.	X5R capacitor recommended. Apply between DECOUPLE pin and GROUND		1		μF

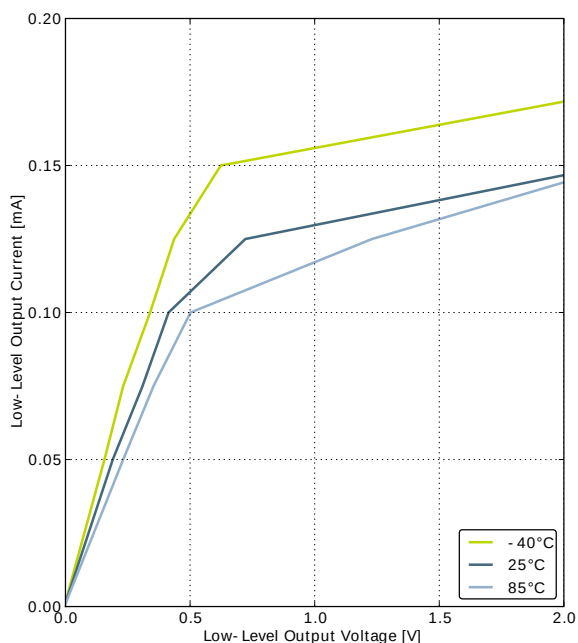
3.7 Flash

Table 3.7. Flash

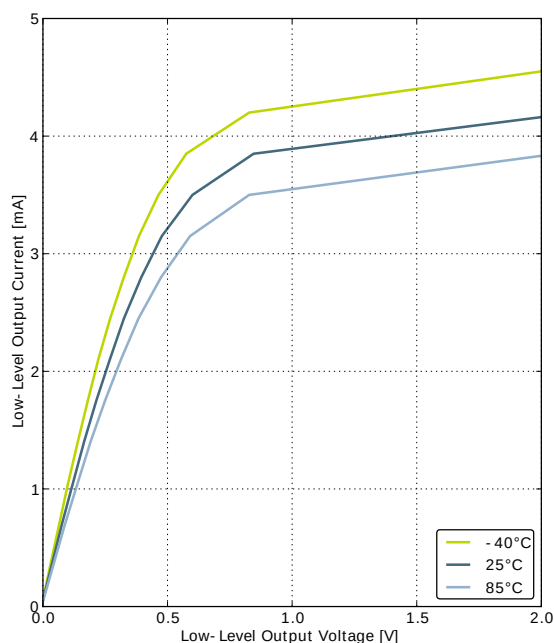
Symbol	Parameter	Condition	Min	Typ	Max	Unit
EC _{FLASH}	Flash erase cycles before failure		20000			cycles
RET _{FLASH}	Flash data retention	T _{AMB} <150°C	10000			h
		T _{AMB} <85°C	10			years
		T _{AMB} <70°C	20			years
t _{W_PROG}	Word (32-bit) programming time		20			μs
t _{PERASE}	Page erase time		20	20.4	20.8	ms
t _{DERASE}	Device erase time		40	40.8	41.6	ms
I _{ERASE}	Erase current				7 ¹	mA
I _{WRITE}	Write current				7 ¹	mA
V _{FLASH}	Supply voltage during flash erase and write		1.98		3.8	V

¹Measured at 25°C

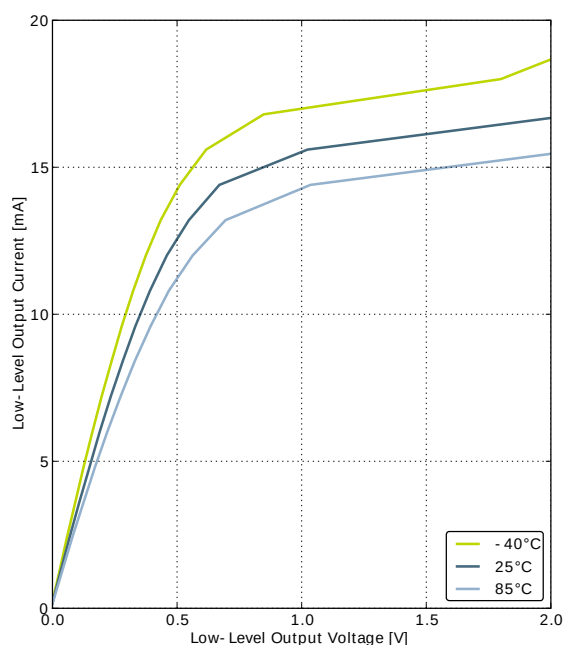
Figure 3.11. Typical Low-Level Output Current, 2V Supply Voltage



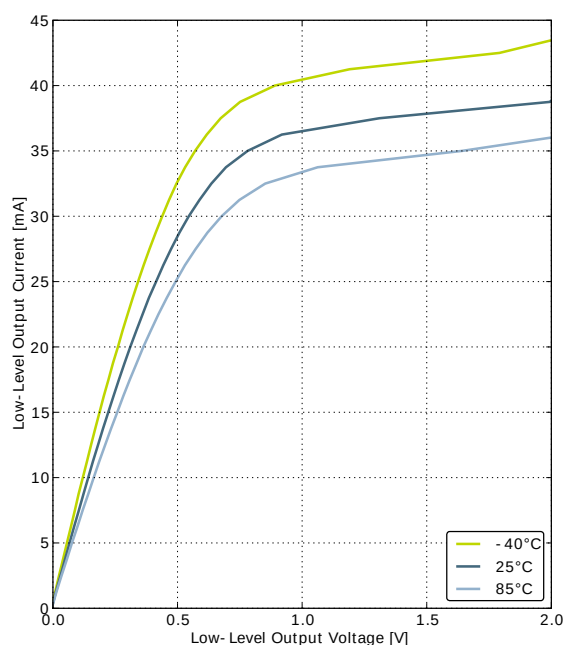
GPIO_Px_CTRL DRIVEMODE = LOWEST



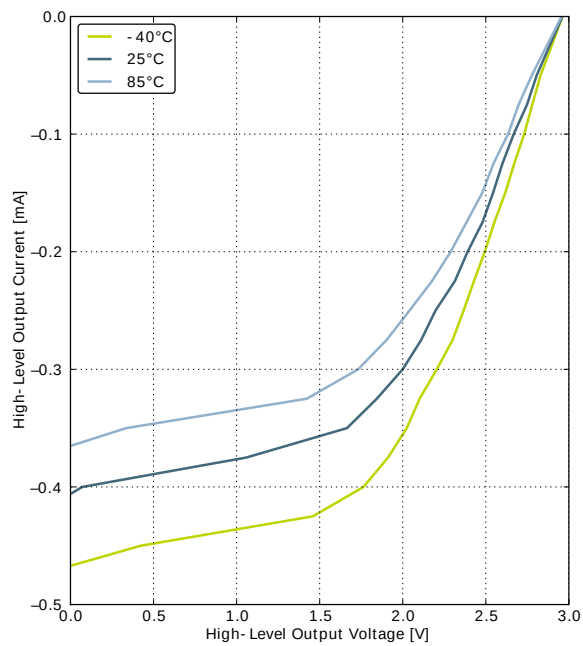
GPIO_Px_CTRL DRIVEMODE = LOW



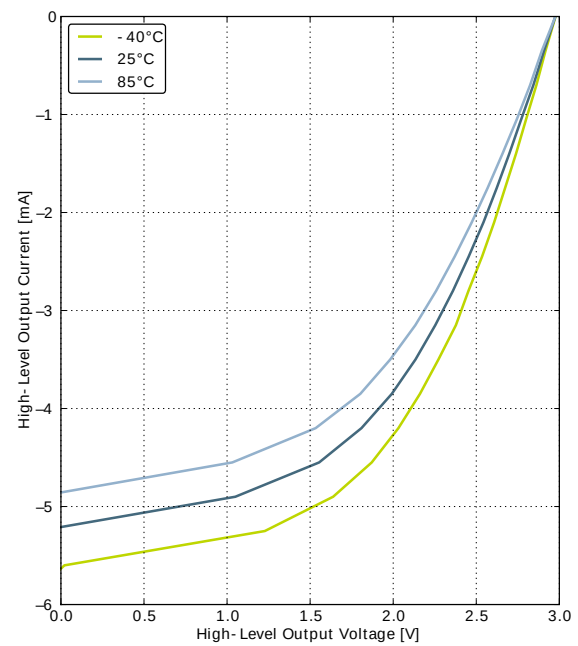
GPIO_Px_CTRL DRIVEMODE = STANDARD



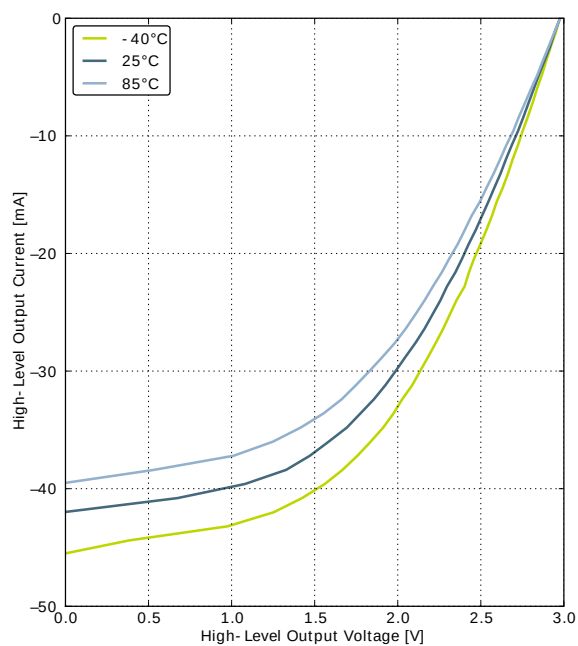
GPIO_Px_CTRL DRIVEMODE = HIGH

Figure 3.14. Typical High-Level Output Current, 3V Supply Voltage

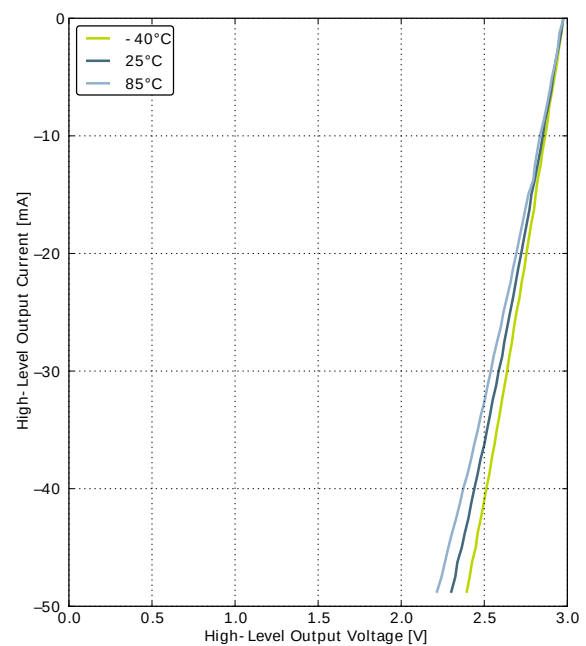
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW

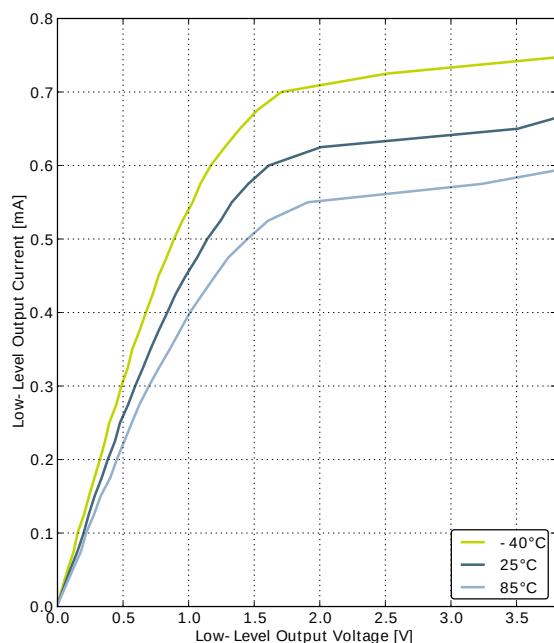


GPIO_Px_CTRL DRIVEMODE = STANDARD

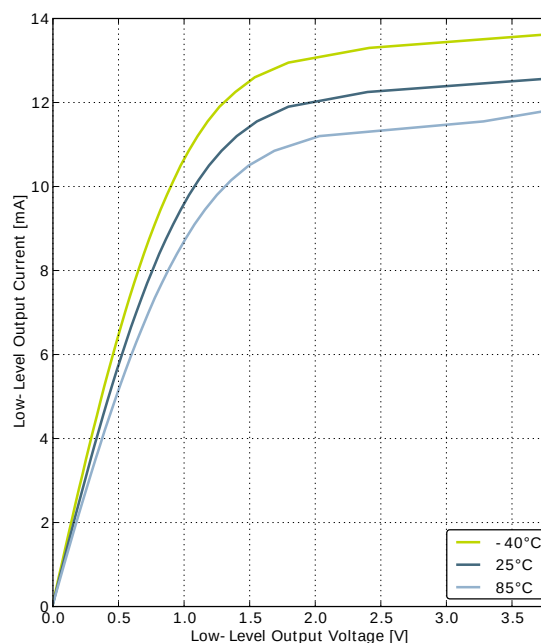


GPIO_Px_CTRL DRIVEMODE = HIGH

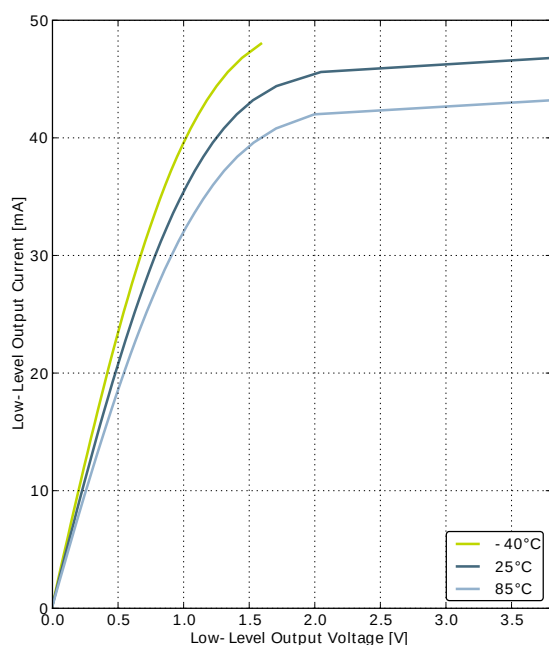
Figure 3.15. Typical Low-Level Output Current, 3.8V Supply Voltage



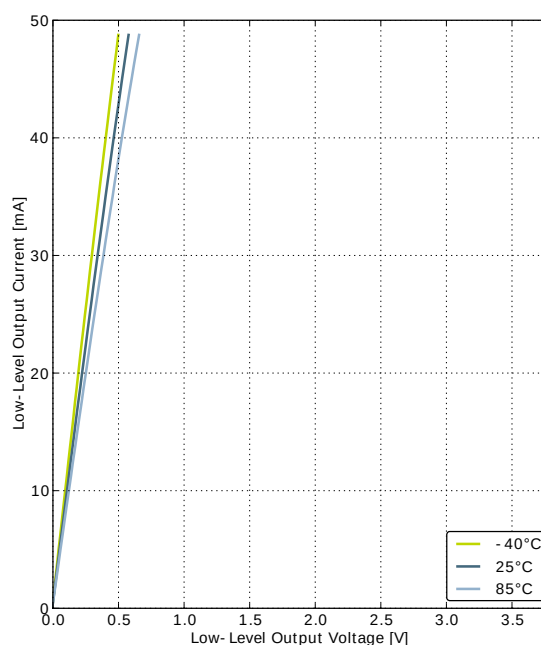
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW



GPIO_Px_CTRL DRIVEMODE = STANDARD



GPIO_Px_CTRL DRIVEMODE = HIGH

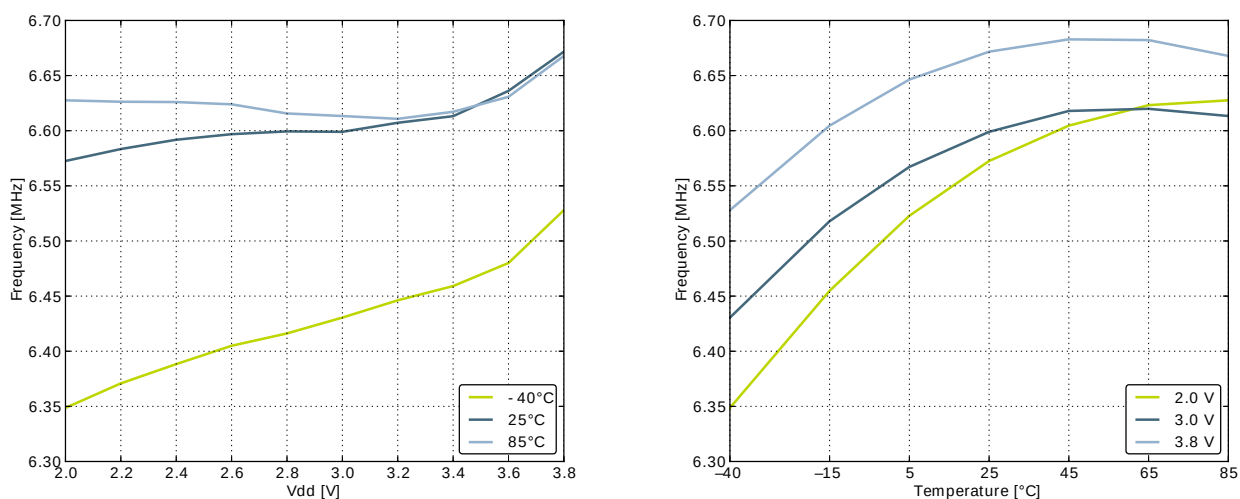
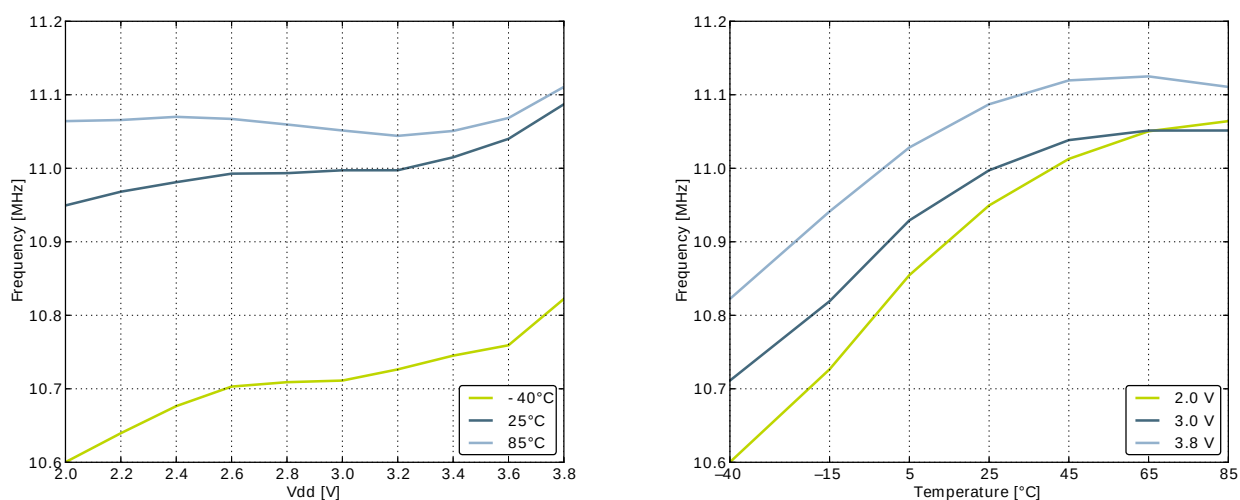
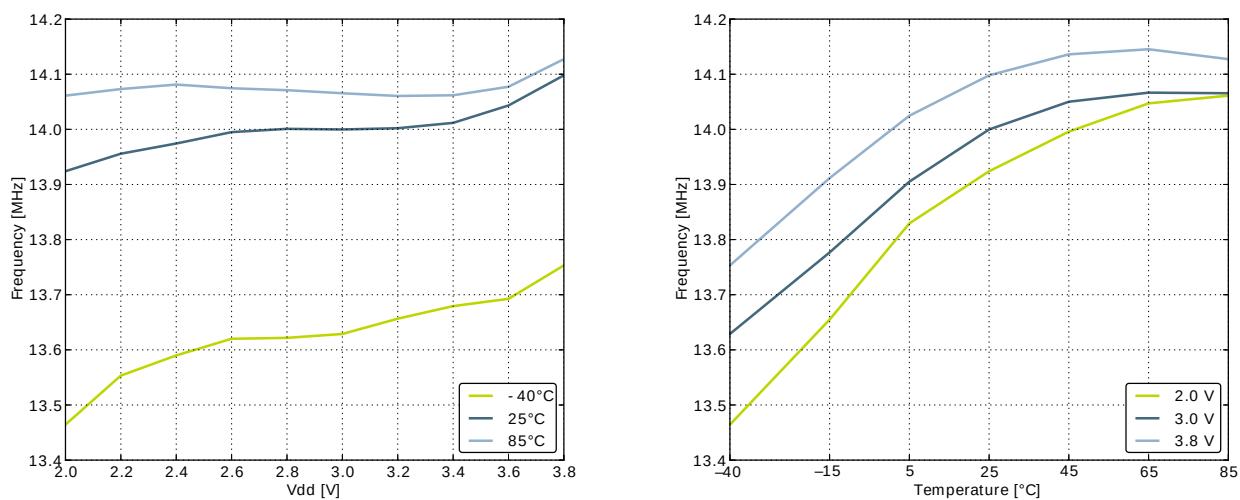
Figure 3.19. Calibrated HFRCO 7 MHz Band Frequency vs Supply Voltage and Temperature**Figure 3.20. Calibrated HFRCO 11 MHz Band Frequency vs Supply Voltage and Temperature****Figure 3.21. Calibrated HFRCO 14 MHz Band Frequency vs Supply Voltage and Temperature**

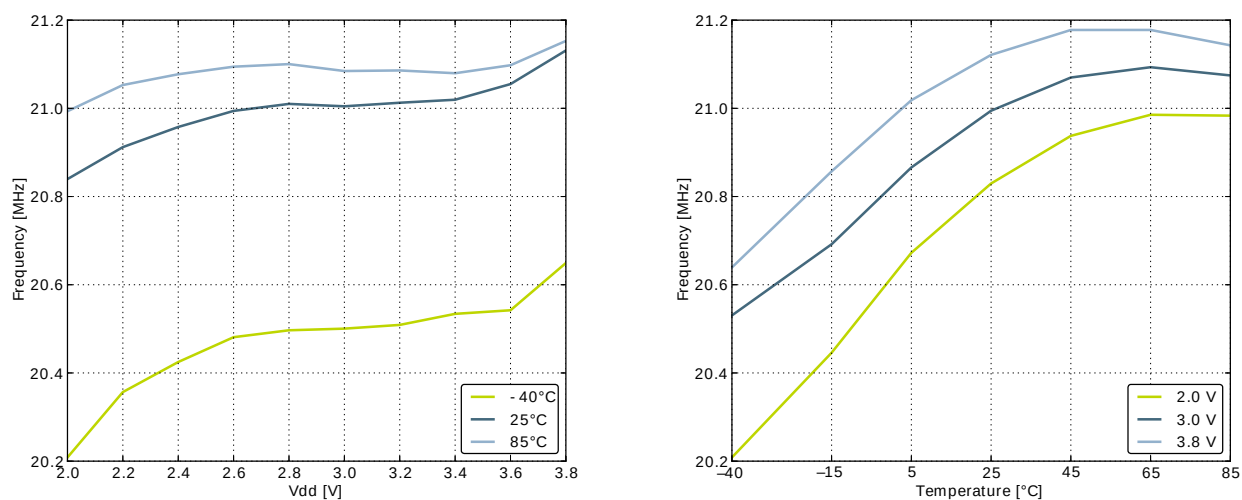
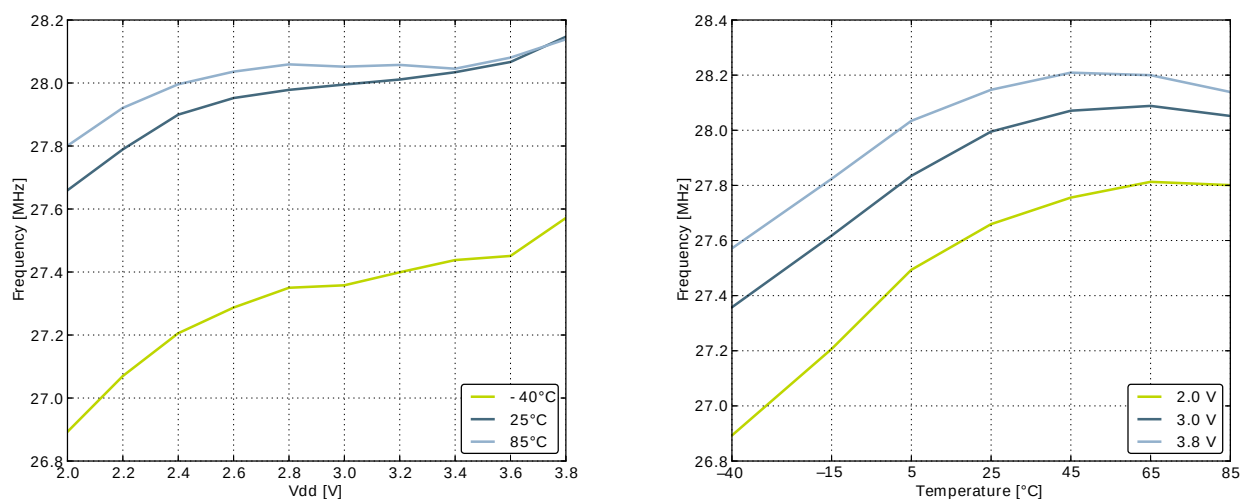
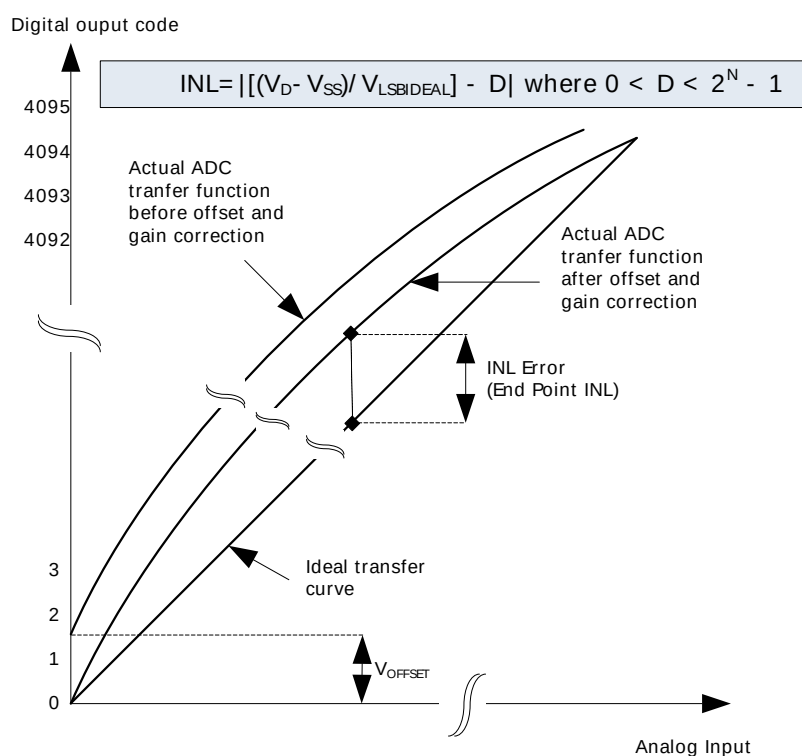
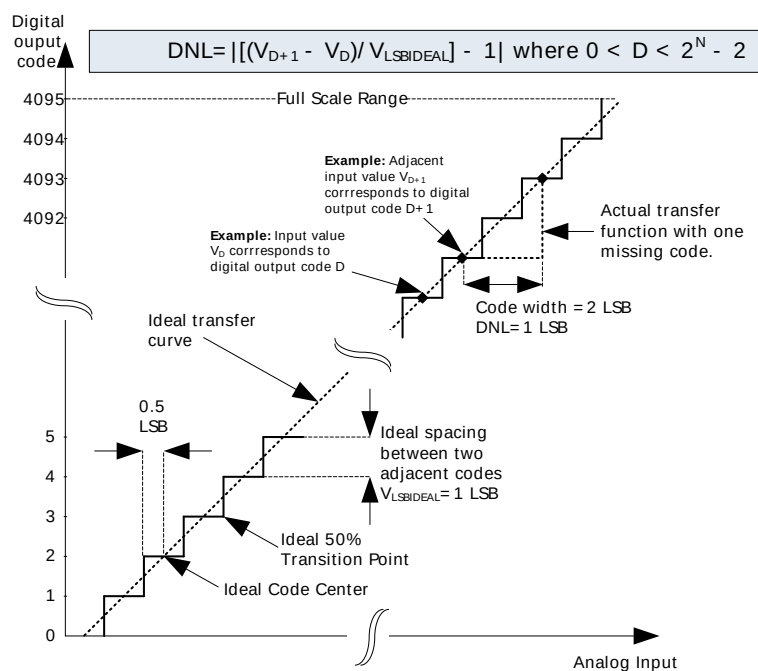
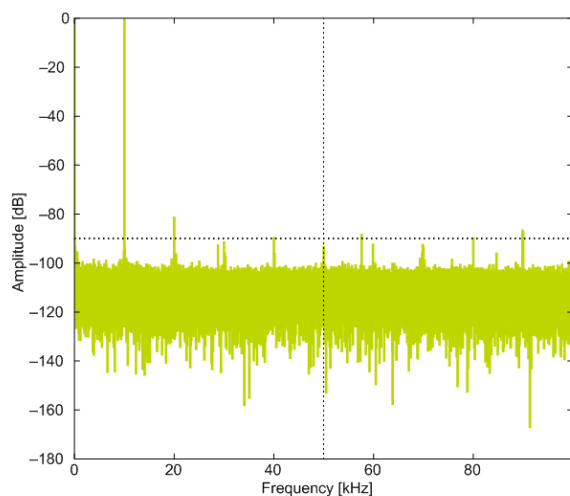
Figure 3.22. Calibrated HFRCO 21 MHz Band Frequency vs Supply Voltage and Temperature**Figure 3.23. Calibrated HFRCO 28 MHz Band Frequency vs Supply Voltage and Temperature**

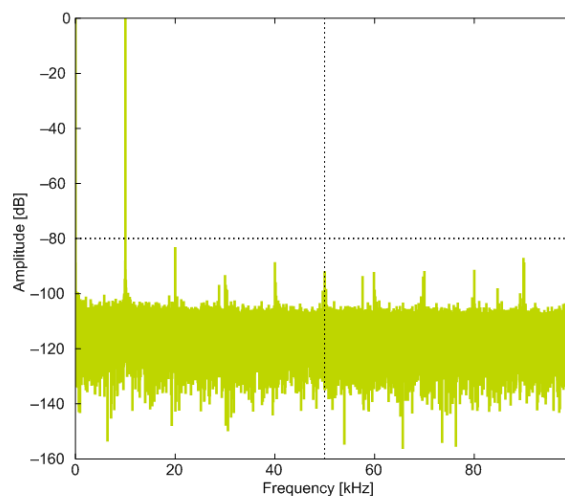
Figure 3.24. Integral Non-Linearity (INL)**Figure 3.25. Differential Non-Linearity (DNL)**

3.10.1 Typical performance

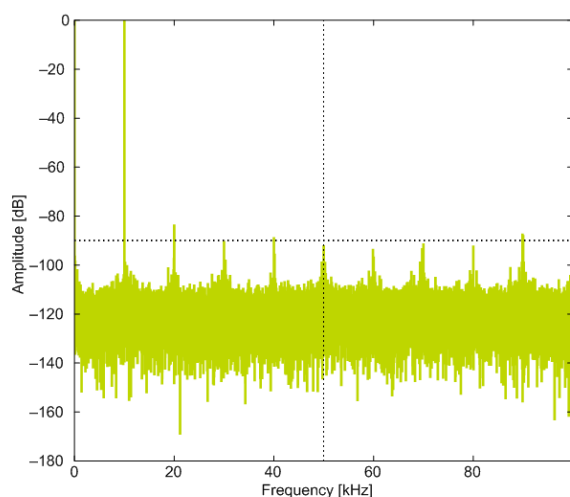
Figure 3.26. ADC Frequency Spectrum, $V_{dd} = 3V$, Temp = 25°C



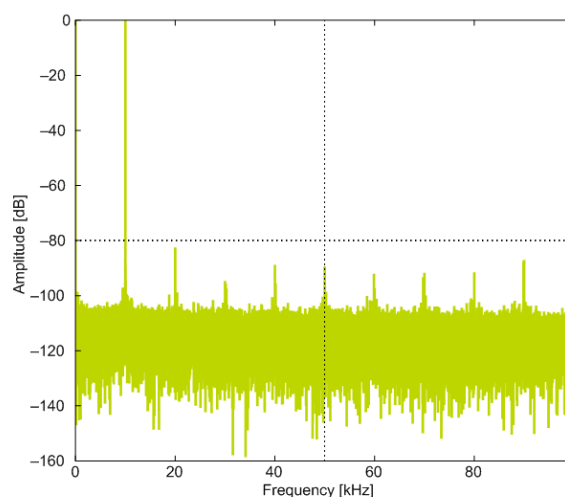
1.25V Reference



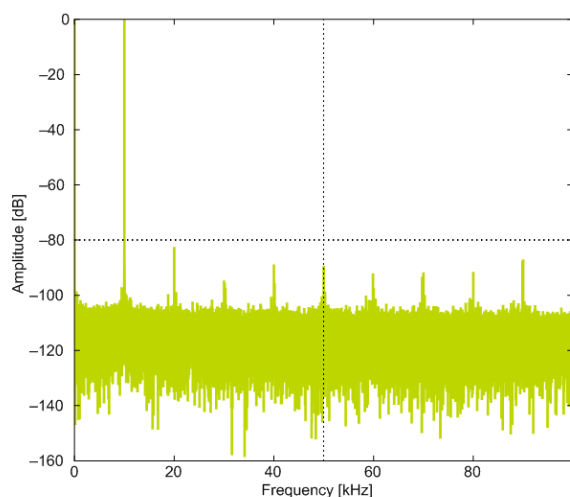
2.5V Reference



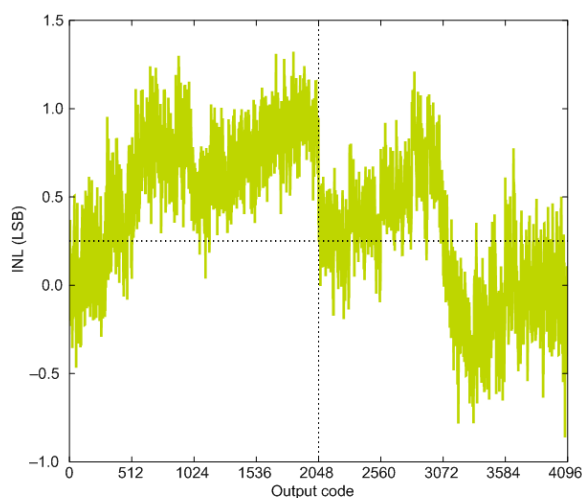
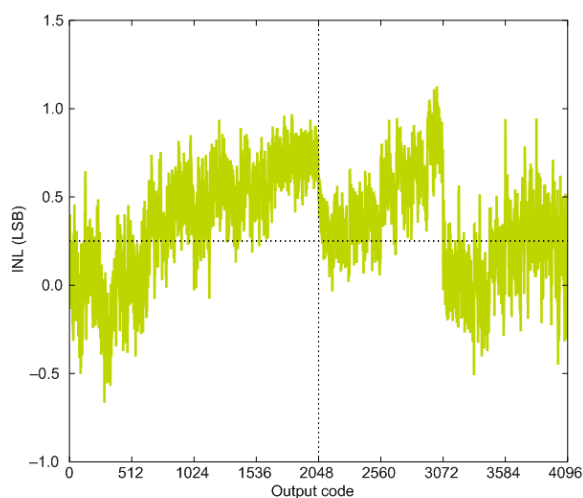
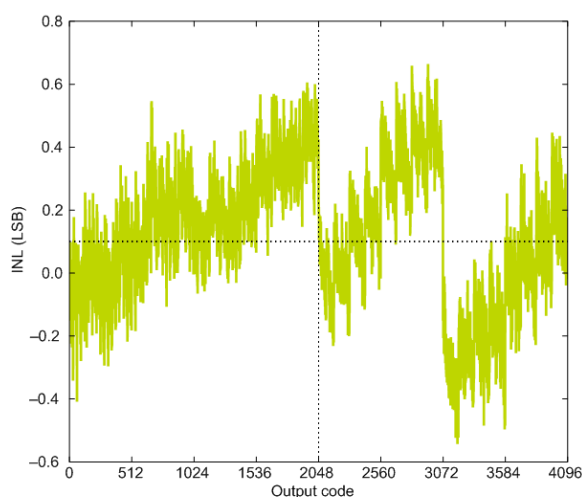
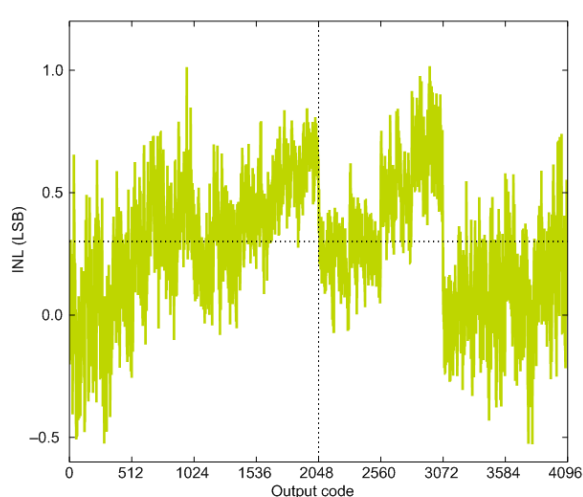
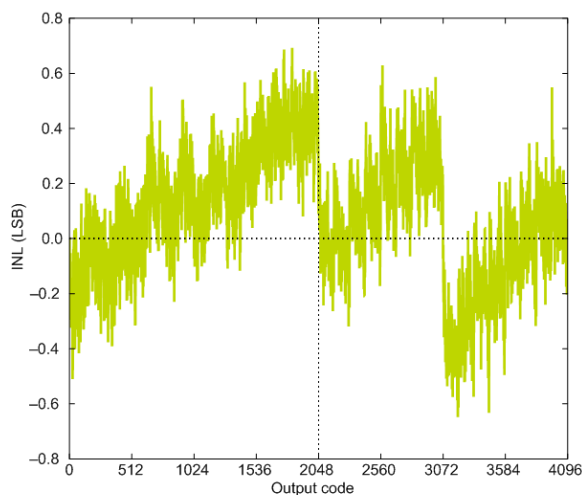
2XVDDVSS Reference



5VDIFF Reference



VDD Reference

Figure 3.27. ADC Integral Linearity Error vs Code, Vdd = 3V, Temp = 25°C**1.25V Reference****2.5V Reference****2XVDDVSS Reference****5VDIFF Reference****VDD Reference**

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		$V_{out}=1V$, RESSEL=0, 0.1 Hz< f <1 MHz, OPAXHCMDIS=0		196		μV_{RMS}
		$V_{out}=1V$, RESSEL=0, 0.1 Hz< f <1 MHz, OPAXHCMDIS=1		229		μV_{RMS}
		RESSEL=7, 0.1 Hz< f <10 kHz, OPAXHCMDIS=0		1230		μV_{RMS}
		RESSEL=7, 0.1 Hz< f <10 kHz, OPAXHCMDIS=1		2130		μV_{RMS}
		RESSEL=7, 0.1 Hz< f <1 MHz, OPAXHCMDIS=0		1630		μV_{RMS}
		RESSEL=7, 0.1 Hz< f <1 MHz, OPAXHCMDIS=1		2590		μV_{RMS}

Figure 3.32. OPAMP Common Mode Rejection Ratio

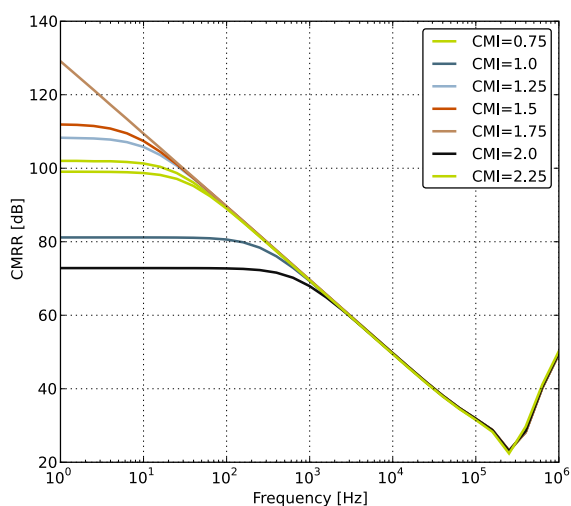
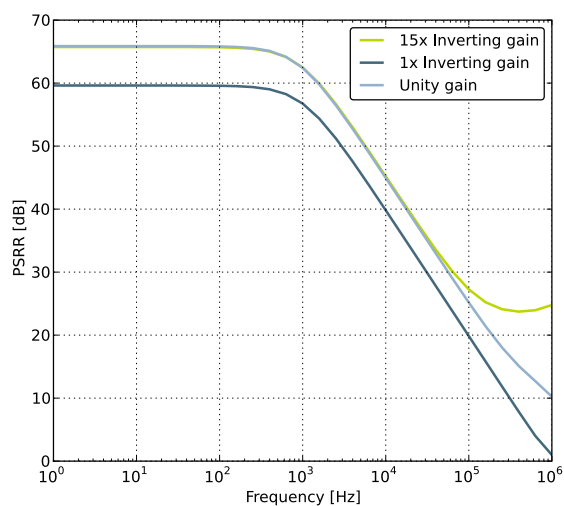


Figure 3.33. OPAMP Positive Power Supply Rejection Ratio



3.15 LCD

Table 3.20. LCD

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{LCDFR}	Frame rate		30		200	Hz
NUM_{SEG}	Number of segments supported			20×8		seg
V_{LCD}	LCD supply voltage range	Internal boost circuit enabled	2.0		3.8	V
I_{LCD}	Steady state current consumption.	Display disconnected, static mode, framerate 32 Hz, all segments on.		250		nA
		Display disconnected, quadruplex mode, framerate 32 Hz, all segments on, bias mode to ONETHIRD in LCD_DISPCTRL register.		550		nA
I_{LCDBOOST}	Steady state Current contribution of internal boost.	Internal voltage boost off		0		μA
		Internal voltage boost on, boosting from 2.2 V to 3.0 V.		8.4		μA
V_{BOOST}	Boost Voltage	VBLEV of LCD_DISPCTRL register to LEVEL0		3.02		V
		VBLEV of LCD_DISPCTRL register to LEVEL1		3.15		V
		VBLEV of LCD_DISPCTRL register to LEVEL2		3.28		V
		VBLEV of LCD_DISPCTRL register to LEVEL3		3.41		V
		VBLEV of LCD_DISPCTRL register to LEVEL4		3.54		V
		VBLEV of LCD_DISPCTRL register to LEVEL5		3.67		V
		VBLEV of LCD_DISPCTRL register to LEVEL6		3.73		V
		VBLEV of LCD_DISPCTRL register to LEVEL7		3.74		V

The total LCD current is given by Equation 3.3 (p. 50) . I_{LCDBOOST} is zero if internal boost is off.

Total LCD Current Based on Operational Mode and Internal Boost

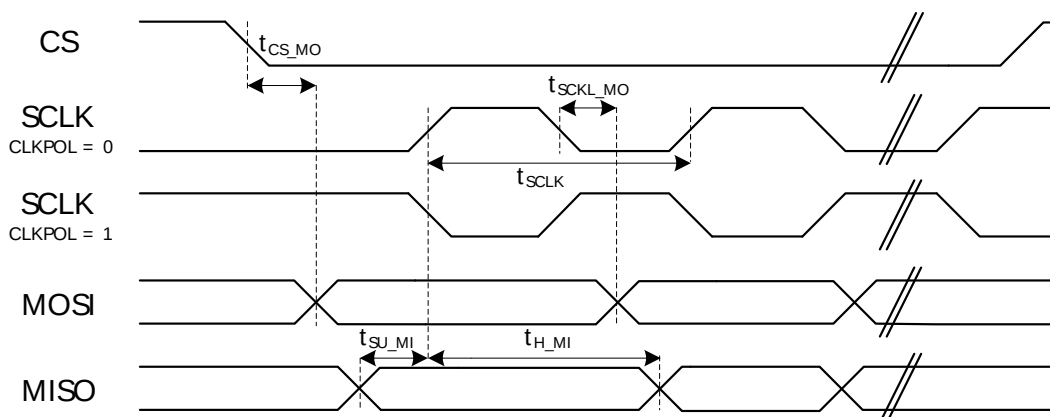
$$I_{\text{LCDTOTAL}} = I_{\text{LCD}} + I_{\text{LCDBOOST}} \quad (3.3)$$

Table 3.23. I2C Fast-mode Plus (Fm+)

Symbol	Parameter	Min	Typ	Max	Unit
f_{SCL}	SCL clock frequency	0		1000 ¹	kHz
t_{LOW}	SCL clock low time	0.5			μ s
t_{HIGH}	SCL clock high time	0.26			μ s
$t_{SU,DAT}$	SDA set-up time	50			ns
$t_{HD,DAT}$	SDA hold time	8			ns
$t_{SU,STA}$	Repeated START condition set-up time	0.26			μ s
$t_{HD,STA}$	(Repeated) START condition hold time	0.26			μ s
$t_{SU,STO}$	STOP condition set-up time	0.26			μ s
t_{BUF}	Bus free time between a STOP and a START condition	0.5			μ s

¹For the minimum HPPERCLK frequency required in Fast-mode Plus, see the I2C chapter in the EFM32WG Reference Manual.

3.17 USART SPI

Figure 3.38. SPI Master Timing**Table 3.24. SPI Master Timing**

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$t_{SCLK}^{1,2}$	SCLK period		$2 * t_{HPPER-CLK}$			ns
$t_{CS_MO}^{1,2}$	CS to MOSI		-2.00		2.00	ns
$t_{SCLK_MO}^{1,2}$	SCLK to MOSI		-1.00		3.00	ns
$t_{SU_MI}^{1,2}$	MISO setup time	IOVDD = 3.0 V	36.00			ns
$t_{H_MI}^{1,2}$	MISO hold time		-6.00			ns

¹Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0)

²Measurement done at 10% and 90% of V_{DD} (figure shows 50% of V_{DD})

QFN64 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
		OPAMP_OUT1ALT			
30	PD2	ADC0_CH2	TIM0_CC1 #3	US1_CLK #1	DBG_SWO #3
31	PD3	ADC0_CH3 OPAMP_N2	TIM0_CC2 #3	US1_CS #1	ETM_TD1 #0/2
32	PD4	ADC0_CH4 OPAMP_P2		LEU0_TX #0	ETM_TD2 #0/2
33	PD5	ADC0_CH5 OPAMP_OUT2 #0		LEU0_RX #0	ETM_TD3 #0/2
34	PD6	ADC0_CH6 DAC0_P1 / OPAMP_P1	TIM1_CC0 #4 LETIM0_OUT0 #0 PCNT0_S0IN #3	US1_RX #2 I2C0_SDA #1	LES_ALTEX0 #0 ACMP0_O #2 ETM_TD0 #0
35	PD7	ADC0_CH7 DAC0_N1 / OPAMP_N1	TIM1_CC1 #4 LETIM0_OUT1 #0 PCNT0_S1IN #3	US1_TX #2 I2C0_SCL #1	CMU_CLK0 #2 LES_ALTEX1 #0 ACMP1_O #2 ETM_TCLK #0
36	PD8	BU_VIN			CMU_CLK1 #1
37	PC6	ACMP0_CH6		LEU1_TX #0 I2C0_SDA #2	LES_CH6 #0 ETM_TCLK #2
38	PC7	ACMP0_CH7		LEU1_RX #0 I2C0_SCL #2	LES_CH7 #0 ETM_TD0 #2
39	VDD_DREG	Power supply for on-chip voltage regulator.			
40	DECOUPLE	Decouple output for on-chip voltage regulator. An external capacitance of size C _{DECOUPLE} is required at this pin.			
41	PE4	LCD_COM0		US0_CS #1	
42	PE5	LCD_COM1		US0_CLK #1	
43	PE6	LCD_COM2		US0_RX #1	
44	PE7	LCD_COM3		US0_TX #1	
45	PC12	ACMP1_CH4 DAC0_OUT1ALT #0/ OPAMP_OUT1ALT			CMU_CLK0 #1 LES_CH12 #0
46	PC13	ACMP1_CH5 DAC0_OUT1ALT #1/ OPAMP_OUT1ALT	TIM0_CDTI0 #1/3 TIM1_CC0 #0 TIM1_CC2 #4 PCNT0_S0IN #0		LES_CH13 #0
47	PC14	ACMP1_CH6 DAC0_OUT1ALT #2/ OPAMP_OUT1ALT	TIM0_CDTI1 #1/3 TIM1_CC1 #0 PCNT0_S1IN #0	US0_CS #3	LES_CH14 #0
48	PC15	ACMP1_CH7 DAC0_OUT1ALT #3/ OPAMP_OUT1ALT	TIM0_CDTI2 #1/3 TIM1_CC2 #0	US0_CLK #3	LES_CH15 #0 DBG_SWO #1
49	PF0		TIM0_CC0 #5 LETIM0_OUT0 #2	US1_CLK #2 LEU0_TX #3 I2C0_SDA #5	DBG_SWCLK #0/1/2/3
50	PF1		TIM0_CC1 #5 LETIM0_OUT1 #2	US1_CS #2 LEU0_RX #3 I2C0_SCL #5	DBG_SWDIO #0/1/2/3 GPIO_EM4WU3
51	PF2	LCD_SEG0	TIM0_CC2 #5	LEU0_TX #4	ACMP1_O #0 DBG_SWO #0 GPIO_EM4WU4
52	PF3	LCD_SEG1	TIM0_CDTI0 #2/5		PRS_CH0 #1 ETM_TD3 #1
53	PF4	LCD_SEG2	TIM0_CDTI1 #2/5		PRS_CH1 #1
54	PF5	LCD_SEG3	TIM0_CDTI2 #2/5		PRS_CH2 #1

QFN64 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
55	IOVDD_5	Digital IO power supply 5.			
56	PE8	LCD_SEG4	PCNT2_S0IN #1		PRS_CH3 #1
57	PE9	LCD_SEG5	PCNT2_S1IN #1		
58	PE10	LCD_SEG6	TIM1_CC0 #1	US0_TX #0	BOOT_TX
59	PE11	LCD_SEG7	TIM1_CC1 #1	US0_RX #0	LES_ALTEX5 #0 BOOT_RX
60	PE12	LCD_SEG8	TIM1_CC2 #1	US0_RX #3 US0_CLK #0 I2C0_SDA #6	CMU_CLK1 #2 LES_ALTEX6 #0
61	PE13	LCD_SEG9		US0_TX #3 US0_CS #0 I2C0_SCL #6	LES_ALTEX7 #0 ACMP0_O #0 GPIO_EM4WU5
62	PE14	LCD_SEG10	TIM3_CC0 #0	LEU0_TX #2	
63	PE15	LCD_SEG11	TIM3_CC1 #0	LEU0_RX #2	
64	PA15	LCD_SEG12	TIM3_CC2 #0		

4.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in Table 4.2 (p. 58). The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

Note

Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Table 4.2. Alternate functionality overview

Alternate	LOCATION							Description
Functionality	0	1	2	3	4	5	6	
ACMP0_CH4	PC4							Analog comparator ACMP0, channel 4.
ACMP0_CH5	PC5							Analog comparator ACMP0, channel 5.
ACMP0_CH6	PC6							Analog comparator ACMP0, channel 6.
ACMP0_CH7	PC7							Analog comparator ACMP0, channel 7.
ACMP0_O	PE13		PD6					Analog comparator ACMP0, digital output.
ACMP1_CH4	PC12							Analog comparator ACMP1, channel 4.
ACMP1_CH5	PC13							Analog comparator ACMP1, channel 5.
ACMP1_CH6	PC14							Analog comparator ACMP1, channel 6.
ACMP1_CH7	PC15							Analog comparator ACMP1, channel 7.
ACMP1_O	PF2		PD7					Analog comparator ACMP1, digital output.
ADC0_CH0	PD0							Analog to digital converter ADC0, input channel number 0.
ADC0_CH1	PD1							Analog to digital converter ADC0, input channel number 1.
ADC0_CH2	PD2							Analog to digital converter ADC0, input channel number 2.
ADC0_CH3	PD3							Analog to digital converter ADC0, input channel number 3.

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
HFX TAL_N	PB14							High Frequency Crystal negative pin. Also used as external optional clock input pin.
HFX TAL_P	PB13							High Frequency Crystal positive pin.
I2C0_SCL	PA1	PD7	PC7			PF1	PE13	I2C0 Serial Clock Line input / output.
I2C0_SDA	PA0	PD6	PC6			PF0	PE12	I2C0 Serial Data input / output.
I2C1_SCL	PC5	PB12						I2C1 Serial Clock Line input / output.
I2C1_SDA	PC4	PB11						I2C1 Serial Data input / output.
LCD_BCAP_N	PA13							LCD voltage booster (optional), boost capacitor, negative pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P.
LCD_BCAP_P	PA12							LCD voltage booster (optional), boost capacitor, positive pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P.
LCD_BEXT	PA14							LCD voltage booster (optional), boost output. If using the LCD voltage booster, connect a 1 uF capacitor between this pin and VSS. An external LCD voltage may also be applied to this pin if the booster is not enabled. If AVDD is used directly as the LCD supply voltage, this pin may be left unconnected or used as a GPIO.
LCD_COM0	PE4							LCD driver common line number 0.
LCD_COM1	PE5							LCD driver common line number 1.
LCD_COM2	PE6							LCD driver common line number 2.
LCD_COM3	PE7							LCD driver common line number 3.
LCD_SEG0	PF2							LCD segment line 0. Segments 0, 1, 2 and 3 are controlled by SEGEN0.
LCD_SEG1	PF3							LCD segment line 1. Segments 0, 1, 2 and 3 are controlled by SEGEN0.
LCD_SEG2	PF4							LCD segment line 2. Segments 0, 1, 2 and 3 are controlled by SEGEN0.
LCD_SEG3	PF5							LCD segment line 3. Segments 0, 1, 2 and 3 are controlled by SEGEN0.
LCD_SEG4	PE8							LCD segment line 4. Segments 4, 5, 6 and 7 are controlled by SEGEN1.
LCD_SEG5	PE9							LCD segment line 5. Segments 4, 5, 6 and 7 are controlled by SEGEN1.
LCD_SEG6	PE10							LCD segment line 6. Segments 4, 5, 6 and 7 are controlled by SEGEN1.
LCD_SEG7	PE11							LCD segment line 7. Segments 4, 5, 6 and 7 are controlled by SEGEN1.
LCD_SEG8	PE12							LCD segment line 8. Segments 8, 9, 10 and 11 are controlled by SEGEN2.
LCD_SEG9	PE13							LCD segment line 9. Segments 8, 9, 10 and 11 are controlled by SEGEN2.
LCD_SEG10	PE14							LCD segment line 10. Segments 8, 9, 10 and 11 are controlled by SEGEN2.
LCD_SEG11	PE15							LCD segment line 11. Segments 8, 9, 10 and 11 are controlled by SEGEN2.
LCD_SEG12	PA15							LCD segment line 12. Segments 12, 13, 14 and 15 are controlled by SEGEN3.
LCD_SEG13	PA0							LCD segment line 13. Segments 12, 13, 14 and 15 are controlled by SEGEN3.
LCD_SEG14	PA1							LCD segment line 14. Segments 12, 13, 14 and 15 are controlled by SEGEN3.

5 PCB Layout and Soldering

5.1 Recommended PCB Layout

Figure 5.1. QFN64 PCB Land Pattern

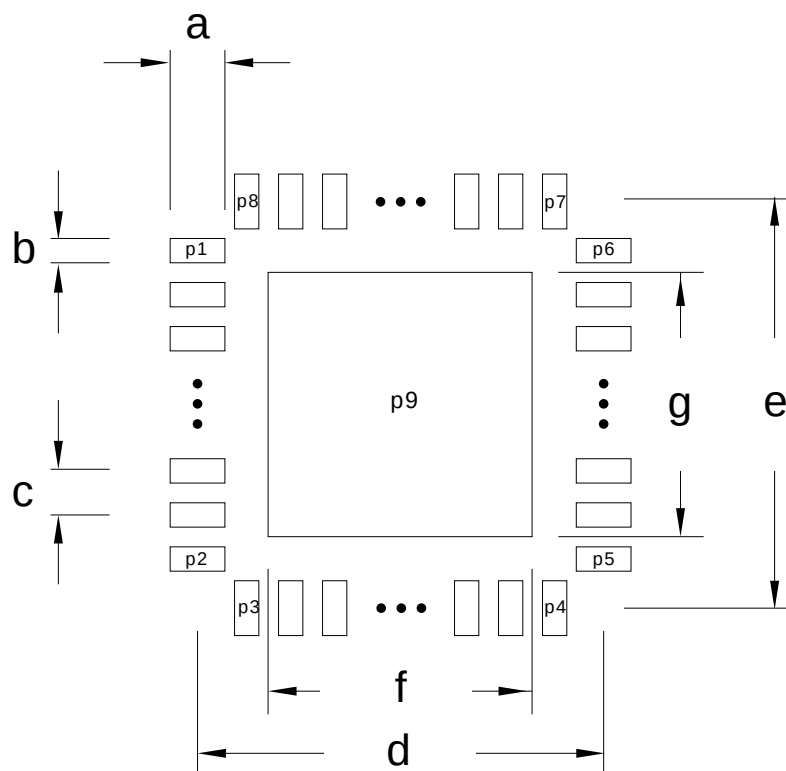


Table 5.1. QFN64 PCB Land Pattern Dimensions (Dimensions in mm)

Symbol	Dim. (mm)	Symbol	Pin number	Symbol	Pin number
a	0.85	P1	1	P8	64
b	0.30	P2	16	P9	65
c	0.50	P3	17	-	-
d	8.90	P4	32	-	-
e	8.90	P5	33	-	-
f	7.20	P6	48	-	-
g	7.20	P7	49	-	-