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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	XCore
Core Size	32-Bit 6-Core
Speed	500MIPS
Connectivity	Configurable
Peripherals	-
Number of I/O	64
Program Memory Size	64KB (16K x 32)
Program Memory Type	SRAM
EEPROM Size	-
RAM Size	-
Voltage - Supply (Vcc/Vdd)	0.95V ~ 3.6V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	128-TQFP Exposed Pad
Supplier Device Package	128-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/xmos/xs1-l6a-64-tq128-c5

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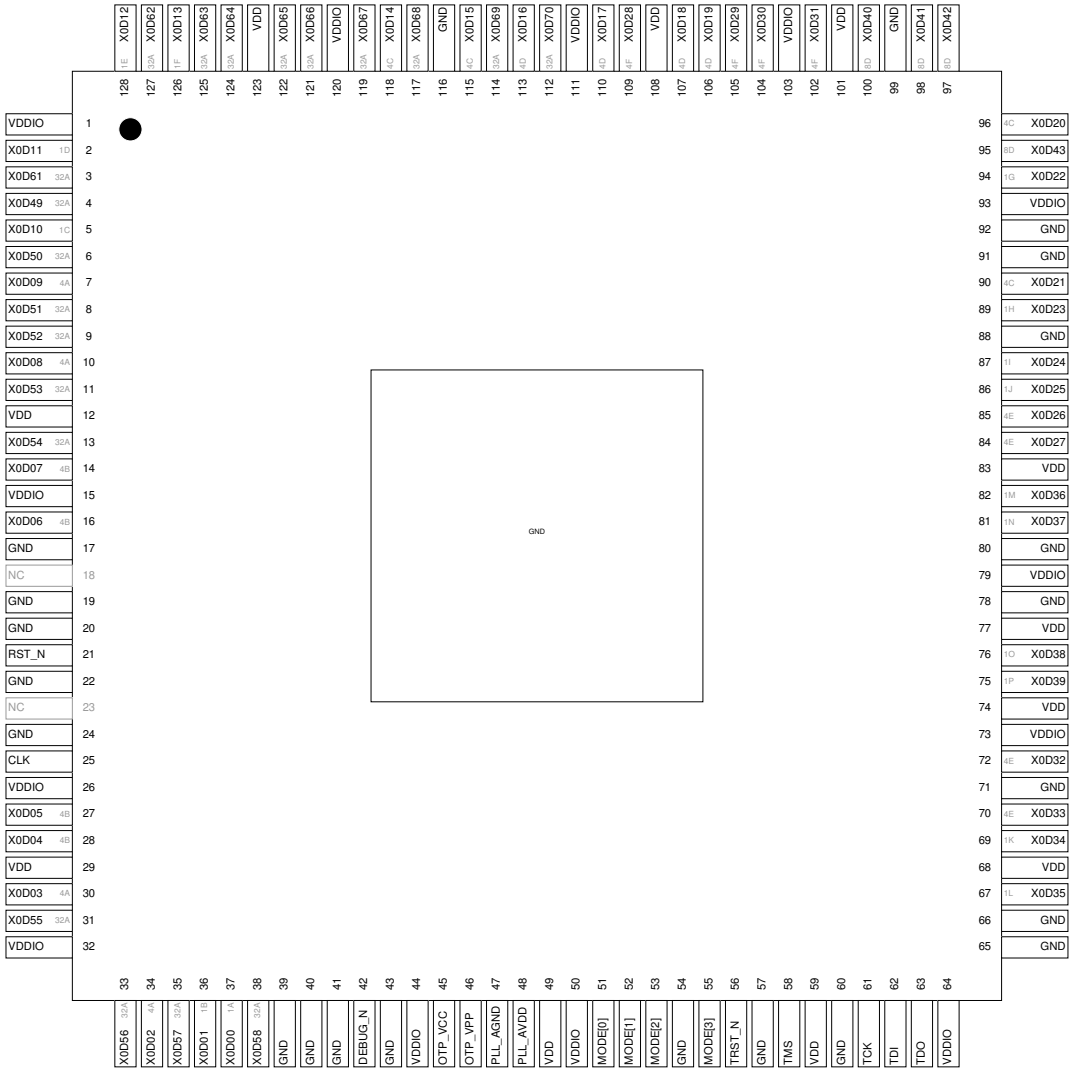
3 Pin Configuration



4 Signal Description

This section lists the signals and I/O pins available on the XS1-L6A-64-TQ128. The device provides a combination of 1bit, 4bit, 8bit and 16bit ports, as well as wider ports that are fully or partially (gray) bonded out. All pins of a port provide either output or input, but signals in different directions cannot be mapped onto the same port.

Pins may have one or more of the following properties:

- PD/PU: The IO pin a weak pull-down or pull-up resistor. On GPIO pins this resistor can be enabled.
- ST: The IO pin has a Schmitt Trigger on its input.

Power pins (8)			
Signal	**Function**	**Type**	**Properties**
GND	Digital ground	GND	
OTP_VCC	OTP power supply	PWR	
OTP_VPP	OTP programming voltage	PWR	
PLL_AGND	Analog ground for PLL	GND	
PLL_AVDD	Analog PLL power	PWR	
RST_N	Global reset input	Input	
VDD	Digital tile power	PWR	
VDDIO	Digital I/O power	PWR	

Clocks pins (2)			
Signal	**Function**	**Type**	**Properties**
CLK	PLL reference clock	Input	PD, ST
MODE[3:0]	Boot mode select	Input	PU, ST

JTAG pins (6)			
Signal	**Function**	**Type**	**Properties**
DEBUG_N	Multi-chip debug	I/O	PU
TCK	Test clock	Input	PU, ST
TDI	Test data input	Input	PU, ST
TDO	Test data output	Output	PD, OT
TMS	Test mode select	Input	PU, ST
TRST_N	Test reset input	Input	PU, ST

I/O pins (64)								
Signal	**Function**						**Type**	**Properties**
X0D00		$1A^0$					I/O	PD_S, R_S
X0D01	XLA^4_{out}	$1B^0$					I/O	PD_S, R_S
X0D02	XLA^3_{out}		$4A^0$	$8A^0$	$16A^0$	$32A^{20}$	I/O	PD_S, R_U
X0D03	XLA^2_{out}		$4A^1$	$8A^1$	$16A^1$	$32A^{21}$	I/O	PD_S, R_U
X0D04	XLA^1_{out}		$4B^0$	$8A^2$	$16A^2$	$32A^{22}$	I/O	PD_S, R_U
X0D05	XLA^0_{out}		$4B^1$	$8A^3$	$16A^3$	$32A^{23}$	I/O	PD_S, R_U
X0D06	XLA^0_{in}		$4B^2$	$8A^4$	$16A^4$	$32A^{24}$	I/O	PD_S, R_U
X0D07	XLA^1_{in}		$4B^3$	$8A^5$	$16A^5$	$32A^{25}$	I/O	PD_S, R_U
X0D08	XLA^2_{in}		$4A^2$	$8A^6$	$16A^6$	$32A^{26}$	I/O	PD_S, R_U
X0D09	XLA^3_{in}		$4A^3$	$8A^7$	$16A^7$	$32A^{27}$	I/O	PD_S, R_U
X0D10	XLA^4_{in}	$1C^0$					I/O	PD_S, R_S
X0D11		$1D^0$					I/O	PD_S, R_S
X0D12		$1E^0$					I/O	PD_S, R_U
X0D13	XLB^4_{out}	$1F^0$					I/O	PD_S, R_U
X0D14	XLB^3_{out}		$4C^0$	$8B^0$	$16A^8$	$32A^{28}$	I/O	PD_S, R_U
X0D15	XLB^2_{out}		$4C^1$	$8B^1$	$16A^9$	$32A^{29}$	I/O	PD_S, R_U
X0D16	XLB^1_{out}		$4D^0$	$8B^2$	$16A^{10}$		I/O	PD_S, R_U
X0D17	XLB^0_{out}		$4D^1$	$8B^3$	$16A^{11}$		I/O	PD_S, R_U
X0D18	XLB^0_{in}		$4D^2$	$8B^4$	$16A^{12}$		I/O	PD_S, R_U
X0D19	XLB^1_{in}		$4D^3$	$8B^5$	$16A^{13}$		I/O	PD_S, R_U
X0D20	XLB^2_{in}		$4C^2$	$8B^6$	$16A^{14}$	$32A^{30}$	I/O	PD_S, R_U
X0D21	XLB^3_{in}		$4C^3$	$8B^7$	$16A^{15}$	$32A^{31}$	I/O	PD_S, R_U
X0D22	XLB^4_{in}	$1G^0$					I/O	PD_S, R_U
X0D23		$1H^0$					I/O	PD_S, R_U
X0D24		$1I^0$					I/O	PD_S
X0D25		$1J^0$					I/O	PD_S
X0D26			$4E^0$	$8C^0$	$16B^0$		I/O	PD_S, R_U
X0D27			$4E^1$	$8C^1$	$16B^1$		I/O	PD_S, R_U
X0D28			$4F^0$	$8C^2$	$16B^2$		I/O	PD_S, R_U
X0D29			$4F^1$	$8C^3$	$16B^3$		I/O	PD_S, R_U
X0D30			$4F^2$	$8C^4$	$16B^4$		I/O	PD_S, R_U
X0D31			$4F^3$	$8C^5$	$16B^5$		I/O	PD_S, R_U
X0D32			$4E^2$	$8C^6$	$16B^6$		I/O	PD_S, R_U
X0D33			$4E^3$	$8C^7$	$16B^7$		I/O	PD_S, R_U
X0D34		$1K^0$					I/O	PD_S
X0D35		$1L^0$					I/O	PD_S
X0D36		$1M^0$		$8D^0$	$16B^8$		I/O	PD_S
X0D37		$1N^0$		$8D^1$	$16B^9$		I/O	PD_S, R_U
X0D38		$1O^0$		$8D^2$	$16B^{10}$		I/O	PD_S, R_U
X0D39		$1P^0$		$8D^3$	$16B^{11}$		I/O	PD_S, R_U
X0D40				$8D^4$	$16B^{12}$		I/O	PD_S, R_U

(continued)

Signal	Function	Type	Properties
X0D41	$8D^{5}$ $16B^{13}$	I/O	PD_S, R_U
X0D42	$8D^{6}$ $16B^{14}$	I/O	PD_S, R_U
X0D43	$8D^{7}$ $16B^{15}$	I/O	PU_S, R_U
X0D49	XLC^{4}_{out} $32A^{0}$	I/O	PD_S
X0D50	XLC^{3}_{out} $32A^{1}$	I/O	PD_S
X0D51	XLC^{2}_{out} $32A^{2}$	I/O	PD_S
X0D52	XLC^{1}_{out} $32A^{3}$	I/O	PD_S
X0D53	XLC^{0}_{out} $32A^{4}$	I/O	PD_S
X0D54	XLC^{0}_{in} $32A^{5}$	I/O	PD_S
X0D55	XLC^{1}_{in} $32A^{6}$	I/O	PD_S
X0D56	XLC^{2}_{in} $32A^{7}$	I/O	PD_S
X0D57	XLC^{3}_{in} $32A^{8}$	I/O	PD_S
X0D58	XLC^{4}_{in} $32A^{9}$	I/O	PD_S
X0D61	XLD^{4}_{out} $32A^{10}$	I/O	PD_S
X0D62	XLD^{3}_{out} $32A^{11}$	I/O	PD_S
X0D63	XLD^{2}_{out} $32A^{12}$	I/O	PD_S
X0D64	XLD^{1}_{out} $32A^{13}$	I/O	PD_S
X0D65	XLD^{0}_{out} $32A^{14}$	I/O	PD_S
X0D66	XLD^{0}_{in} $32A^{15}$	I/O	PD_S
X0D67	XLD^{1}_{in} $32A^{16}$	I/O	PD_S
X0D68	XLD^{2}_{in} $32A^{17}$	I/O	PD_S
X0D69	XLD^{3}_{in} $32A^{18}$	I/O	PD_S
X0D70	XLD^{4}_{in} $32A^{19}$	I/O	PD_S

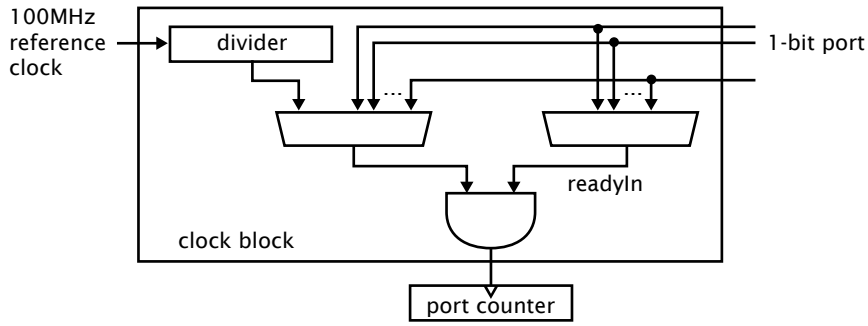


Figure 4: Clock block diagram

In many cases I/O signals are accompanied by strobing signals. The xCORE ports can input and interpret strobe (known as readyIn and readyOut) signals generated by external sources, and ports can generate strobe signals to accompany output data.

On reset, each port is connected to clock block 0, which runs from the xCORE Tile reference clock.

5.5 Channels and Channel Ends

Logical cores communicate using point-to-point connections, formed between two channel ends. A channel-end is a resource on an xCORE tile, that is allocated by the program. Each channel-end has a unique system-wide identifier that comprises a unique number and their tile identifier. Data is transmitted to a channel-end by an output-instruction; and the other side executes an input-instruction. Data can be passed synchronously or asynchronously between the channel ends.

5.6 xCONNECT Switch and Links

XMOS devices provide a scalable architecture, where multiple xCORE devices can be connected together to form one system. Each xCORE device has an xCONNECT interconnect that provides a communication infrastructure for all tasks that run on the various xCORE tiles on the system.

The interconnect relies on a collection of switches and XMOS links. Each xCORE device has an on-chip switch that can set up circuits or route data. The switches are connected by xConnect Links. An XMOS link provides a physical connection between two switches. The switch has a routing algorithm that supports many different topologies, including lines, meshes, trees, and hypercubes.

The links operate in either 2 wires per direction or 5 wires per direction mode, depending on the amount of bandwidth required. Circuit switched, streaming and packet switched data can both be supported efficiently. Streams provide the fastest possible data rates between xCORE Tiles (up to 250 MBit/s), but each stream requires a single link to be reserved between switches on two tiles. All packet communications can be multiplexed onto a single link.

10 Board Integration

The device has the following power supply pins:

- VDD pins for the xCORE Tile
- VDDIO pins for the I/O lines
- PLL_AVDD pins for the PLL
- OTP_VCC pins for the OTP
- OTP_VPP pins for faster programming the OTP (optional)

Several pins of each type are provided to minimize the effect of inductance within the package, all of which must be connected. The power supplies must be brought up monotonically and input voltages must not exceed specification at any time.

The VDD supply must ramp from 0 V to its final value within 10 ms to ensure correct startup.

The VDDIO and OTP_VCC supply must ramp to its final value before VDD reaches 0.4 V.

The PLL_AVDD supply should be separated from the other noisier supplies on the board. The PLL requires a very clean power supply, and a low pass filter (for example, a 4.7 Ω resistor and 100 nF multi-layer ceramic capacitor) is recommended on this pin.

The OTP_VCC supply should be connected to the VDDIO supply.

The OTP_VPP supply can be optionally provided for faster OTP programming times, otherwise an internal charge pump is used.

The following ground pins are provided:

- PLL_AGND for PLL_AVDD
- GND for all other supplies

All ground pins must be connected directly to the board ground.

The VDD and VDDIO supplies should be decoupled close to the chip by several 100 nF low inductance multi-layer ceramic capacitors between the supplies and GND (for example, 4x100nF 0402 low inductance MLCCs per supply rail). The ground side of the decoupling capacitors should have as short a path back to the GND pins as possible. A bulk decoupling capacitor of at least 10 uF should be placed on each of these supplies.

RST_N is an active-low asynchronous-assertion global reset signal. Following a reset, the PLL re-establishes lock after which the device boots up according to the boot mode (*see* §7). RST_N and must be asserted low during and after power up for 100 ns.

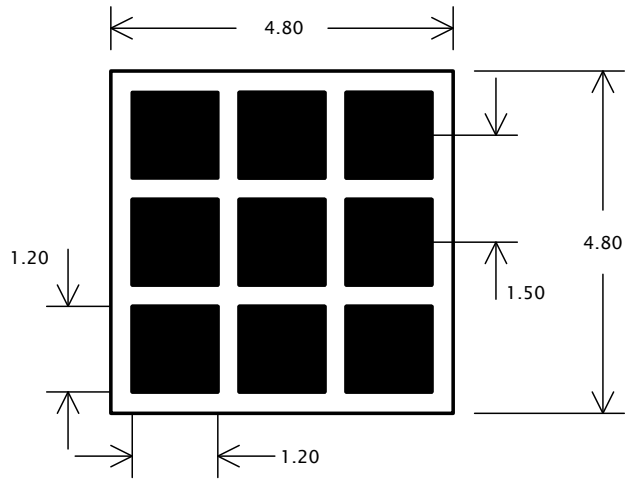


Figure 15: Solder stencil for centre pad

12.1 Part Marking

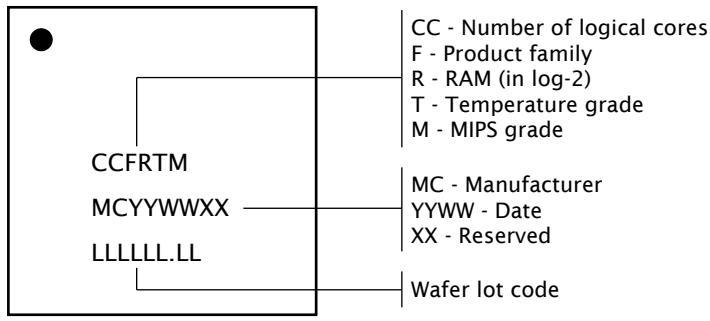


Figure 25: Part marking scheme

13 Ordering Information

Product Code	Marking	Qualification	Speed Grade
XS1-L6A-64-TQ128-C4	6L6C4	Commercial	400 MIPS
XS1-L6A-64-TQ128-C5	6L6C5	Commercial	500 MIPS
XS1-L6A-64-TQ128-I4	6L6I4	Industrial	400 MIPS
XS1-L6A-64-TQ128-I5	6L6I5	Industrial	500 MIPS

Figure 26: Orderable part numbers

The response to a write message comprises either control tokens 3 and 1 (for success), or control tokens 4 and 1 (for failure).

A read message comprises the following:

control-token 193	24-bit response channel-end identifier	16-bit register number	control-token 1

The response to the read message comprises either control token 3, 32-bit of data, and control-token 1 (for success), or control tokens 4 and 1 (for failure).

A.3 Accessing node configuration

Node configuration registers can be accessed through the interconnect using the functions `write_node_config_reg(device, ...)` and `read_node_config_reg(device, ...)`, where `device` is the name of the node. These functions implement the protocols described below.

Instead of using the functions above, a channel-end can be allocated to communicate with the node configuration registers. The destination of the channel-end should be set to `0xnnnnC30C` where `nnnn` is the node-identifier.

A write message comprises the following:

control-token 192	24-bit response channel-end identifier	16-bit register number	32-bit data	control-token 1

The response to a write message comprises either control tokens 3 and 1 (for success), or control tokens 4 and 1 (for failure).

A read message comprises the following:

control-token 193	24-bit response channel-end identifier	16-bit register number	control-token 1

The response to a read message comprises either control token 3, 32-bit of data, and control-token 1 (for success), or control tokens 4 and 1 (for failure).

B Processor Status Configuration

The processor status control registers can be accessed directly by the processor using processor status reads and writes (use `getps(reg)` and `setps(reg,value)` for reads and writes).

Number	Perm	Description
0x00	RW	RAM base address
0x01	RW	Vector base address
0x02	RW	xCORE Tile control
0x03	RO	xCORE Tile boot status
0x05	RO	Security configuration
0x06	RW	Ring Oscillator Control
0x07	RO	Ring Oscillator Value
0x08	RO	Ring Oscillator Value
0x09	RO	Ring Oscillator Value
0x0A	RO	Ring Oscillator Value
0x10	DRW	Debug SSR
0x11	DRW	Debug SPC
0x12	DRW	Debug SSP
0x13	DRW	DGETREG operand 1
0x14	DRW	DGETREG operand 2
0x15	DRW	Debug interrupt type
0x16	DRW	Debug interrupt data
0x18	DRW	Debug core control
0x20 .. 0x27	DRW	Debug scratch
0x30 .. 0x33	DRW	Instruction breakpoint address
0x40 .. 0x43	DRW	Instruction breakpoint control
0x50 .. 0x53	DRW	Data watchpoint address 1
0x60 .. 0x63	DRW	Data watchpoint address 2
0x70 .. 0x73	DRW	Data breakpoint control register
0x80 .. 0x83	DRW	Resources breakpoint mask
0x90 .. 0x93	DRW	Resources breakpoint value
0x9C .. 0x9F	DRW	Resources breakpoint control register

Figure 28: Summary

B.1 RAM base address: 0x00

This register contains the base address of the RAM. It is initialized to 0x00010000.

0x00: RAM base address

Bits	Perm	Init	Description
31:2	RW		Most significant 16 bits of all addresses.
1:0	RO	-	Reserved

B.2 Vector base address: 0x01

Base address of event vectors in each resource. On an interrupt or event, the 16 most significant bits of the destination address are provided by this register; the least significant 16 bits come from the event vector.

0x01: Vector base address

Bits	Perm	Init	Description
31:16	RW		The most significant bits for all event and interrupt vectors.
15:0	RO	-	Reserved

B.3 xCORE Tile control: 0x02

Register to control features in the xCORE tile

0x02: xCORE Tile control

Bits	Perm	Init	Description
31:6	RO	-	Reserved
5	RW	0	Set to 1 to select the dynamic mode for the clock divider when the clock divider is enabled. In dynamic mode the clock divider is only activated when all active logical cores are paused. In static mode the clock divider is always enabled.
4	RW	0	Set to 1 to enable the clock divider. This slows down the xCORE tile clock in order to use less power.
3:0	RO	-	Reserved

B.4 xCORE Tile boot status: 0x03

This read-only register describes the boot status of the xCORE tile.

0x03: xCORE Tile boot status

Bits	Perm	Init	Description
31:24	RO	-	Reserved
23:16	RO		xCORE tile number on the switch.
15:9	RO	-	Reserved
8	RO		Set to 1 if boot from OTP is enabled.
7:0	RO		The boot mode pins MODE0, MODE1, ..., specifying the boot frequency, boot source, etc.

B.5 Security configuration: 0x05

Copy of the security register as read from OTP.

0x05: Security configuration

Bits	Perm	Init	Description
31:0	RO		Value.

B.6 Ring Oscillator Control: 0x06

There are four free-running oscillators that clock four counters. The oscillators can be started and stopped using this register. The counters should only be read when the ring oscillator is stopped. The counter values can be read using four subsequent registers. The ring oscillators are asynchronous to the xCORE tile clock and can be used as a source of random bits.

0x06: Ring Oscillator Control

Bits	Perm	Init	Description
31:2	RO	-	Reserved
1	RW	0	Set to 1 to enable the xCORE tile ring oscillators
0	RW	0	Set to 1 to enable the peripheral ring oscillators

B.7 Ring Oscillator Value: 0x07

This register contains the current count of the xCORE Tile Cell ring oscillator. This value is not reset on a system reset.

0x07: Ring Oscillator Value

Bits	Perm	Init	Description
31:16	RO	-	Reserved
15:0	RO	-	Ring oscillator counter data.

B.8 Ring Oscillator Value: 0x08

This register contains the current count of the xCORE Tile Wire ring oscillator. This value is not reset on a system reset.

0x08: Ring Oscillator Value

Bits	Perm	Init	Description
31:16	RO	-	Reserved
15:0	RO	-	Ring oscillator counter data.

B.9 Ring Oscillator Value: 0x09

This register contains the current count of the Peripheral Cell ring oscillator. This value is not reset on a system reset.

0x09: Ring Oscillator Value

Bits	Perm	Init	Description
31:16	RO	-	Reserved
15:0	RO	-	Ring oscillator counter data.

B.10 Ring Oscillator Value: 0x0A

This register contains the current count of the Peripheral Wire ring oscillator. This value is not reset on a system reset.

0x0A: Ring Oscillator Value

Bits	Perm	Init	Description
31:16	RO	-	Reserved
15:0	RO	-	Ring oscillator counter data.

B.11 Debug SSR: 0x10

This register contains the value of the SSR register when the debugger was called.

0x10: Debug SSR

Bits	Perm	Init	Description
31:0	RO	-	Reserved

B.12 Debug SPC: 0x11

This register contains the value of the SPC register when the debugger was called.

0x06: PLL settings

Bits	Perm	Init	Description
31:26	RO	-	Reserved
25:23	RW		OD: Output divider value The initial value depends on pins MODE0 and MODE1.
22:21	RO	-	Reserved
20:8	RW		F: Feedback multiplication ratio The initial value depends on pins MODE0 and MODE1.
7	RO	-	Reserved
6:0	RW		R: Oscilator input divider value The initial value depends on pins MODE0 and MODE1.

D.6 System switch clock divider: 0x07

Sets the ratio of the PLL clock and the switch clock.

0x07: System switch clock divider

Bits	Perm	Init	Description
31:16	RO	-	Reserved
15:0	RW	0	Switch clock divider. The PLL clock will be divided by this value plus one to derive the switch clock.

D.7 Reference clock: 0x08

Sets the ratio of the PLL clock and the reference clock used by the node.

0x08: Reference clock

Bits	Perm	Init	Description
31:16	RO	-	Reserved
15:0	RW	3	Architecture reference clock divider. The PLL clock will be divided by this value plus one to derive the 100 MHz reference clock.

D.8 Directions 0-7: 0x0C

This register contains eight directions, for packets with a mismatch in bits 7..0 of the node-identifier. The direction in which a packet will be routed is goverened by the most significant mismatching bit.

D.13 PLink status and network: 0x40 .. 0x43

These registers contain status information and the network number that each processor-link belongs to.

0x40 .. 0x43: PLink status and network

Bits	Perm	Init	Description
31:26	RO	-	Reserved
25:24	RO		If this link is currently routing data into the switch, this field specifies the type of link that the data is routed to: 0: plink 1: external link 2: internal control link
23:16	RO	0	If the link is routing data into the switch, this field specifies the destination link number to which all tokens are sent.
15:6	RO	-	Reserved
5:4	RW	0	Determines the network to which this link belongs, set for quality of service.
3	RO	-	Reserved
2	RO	0	Set to 1 if the current packet is junk and being thrown away. A packet is considered junk if, for example, it is not routable.
1	RO	0	Set to 1 if the switch is routing data into the link, and if a route exists from another link.
0	RO	0	Set to 1 if the link is routing data into the switch, and if a route is created to another link on the switch.

D.14 Link configuration and initialization: 0x80 .. 0x87

These registers contain configuration and debugging information specific to external links. The link speed and width can be set, the link can be initialized, and the link status can be monitored. The registers control links C, D, A, B, G, H, E, and F in that order.

G JTAG, xSCOPE and Debugging

If you intend to design a board that can be used with the XMOS toolchain and xTAG debugger, you will need an xSYS header on your board. Figure 32 shows a decision diagram which explains what type of xSYS connectivity you need. The three subsections below explain the options in detail.

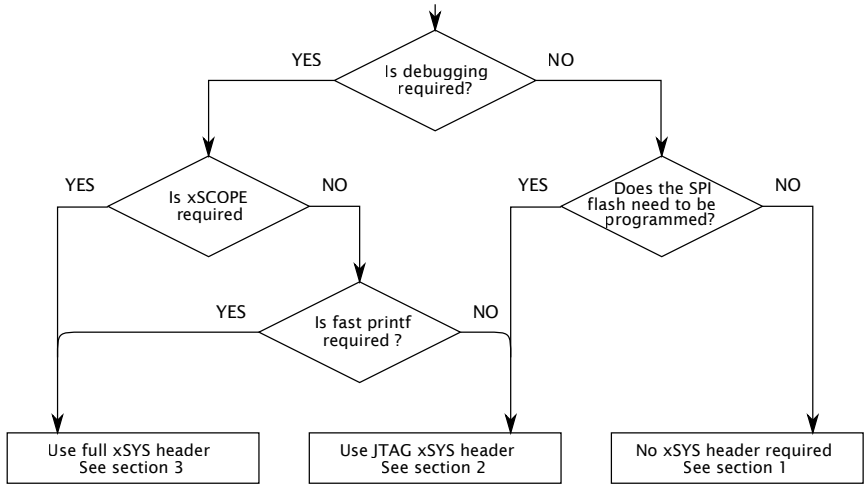


Figure 32: Decision diagram for the xSYS header

G.1 No xSYS header

The use of an xSYS header is optional, and may not be required for volume production designs. However, the XMOS toolchain expects the xSYS header; if you do not have an xSYS header then you must provide your own method for writing to flash/OTP and for debugging.

G.2 JTAG-only xSYS header

The xSYS header connects to an xTAG debugger, which has a 20-pin 0.1" female IDC header. The design will hence need a male IDC header. We advise to use a boxed header to guard against incorrect plug-ins. If you use a 90 degree angled header, make sure that pins 2, 4, 6, ..., 20 are along the edge of the PCB.

Connect pins 4, 8, 12, 16, 20 of the xSYS header to ground, and then connect:

- TDI to pin 5 of the xSYS header
- TMS to pin 7 of the xSYS header
- TCK to pin 9 of the xSYS header
- DEBUG_N to pin 11 of the xSYS header

H Schematics Design Check List

☑ This section is a checklist for use by schematics designers using the XS1-L6A-64-TQ128. Each of the following sections contains items to check for each design.

H.1 Power supplies

☐ VDDIO and OTP_VCC supply is within specification before the VDD (core) supply is turned on. Specifically, the VDDIO and OTP_VCC supply is within specification before VDD (core) reaches 0.4V (Section 10).

☐ The VDD (core) supply ramps monotonically (rises constantly) from 0V to its final value (0.95V - 1.05V) within 10ms (Section 10).

☐ The VDD (core) supply is capable of supplying 300mA (Section 10).

☐ PLL_AVDD is filtered with a low pass filter, for example an RC filter, see Section 10

H.2 Power supply decoupling

☐ The design has multiple decoupling capacitors per supply, for example at least four0402 or 0603 size surface mount capacitors of 100nF in value, per supply (Section 10).

☐ A bulk decoupling capacitor of at least 10uF is placed on each supply (Section 10).

H.3 Power on reset

☐ The RST_N and TRST_N pins are asserted (low) during or after power up. The device is not used until these resets have taken place.
As the errata in the datasheets show, the internal pull-ups on these two pins can occasionally provide stronger than normal pull-up currents. For this reason, an RC type reset circuit is discouraged as behavior would be unpredictable. A voltage supervisor type reset device is recommended to guarantee a good reset. This also has the benefit of resetting the system should the relevant supply go out of specification.

H.4 Clock

☐ The CLK input pin is supplied with a clock with monotonic rising edges and low jitter.

- ☐ Pins MODE0 and MODE1 are set to the correct value for the chosen oscillator frequency. The MODE settings are shown in the Oscillator section, Section 6. If you have a choice between two values, choose the value with the highest multiplier ratio since that will boot faster.

H.5 USB ULPI Mode

This section can be skipped if you do not have an external USB PHY.

- ☐ If using ULPI, the ULPI signals are connected to specific ports as shown in Section E.
- ☐ If using ULPI, the ports that are used internally are not connected, see Section E. (Note that this limitation only applies when the ULPI is enabled, they can still be used before or after the ULPI is being used.)

H.6 Boot

- ☐ The device is connected to a SPI flash for booting, connected to X0D0, X0D01, X0D10, and X0D11 (Section 7). If not, you must boot the device through OTP or JTAG.
- ☐ The device that is connected to flash has both MODE2 and MODE3 connected to pin 3 on the xSYS Header (MSEL). If no debug adapter connection is supported (not recommended) MODE2 and MODE3 are to be left NC (Section 7).
- ☐ The SPI flash that you have chosen is supported by **xflash**, or you have created a specification file for it.

H.7 JTAG, XScope, and debugging

- ☐ You have decided as to whether you need an XSYS header or not (Section G)
- ☐ If you included an XSYS header, you connected pin 3 to any MODE2/MODE3 pin that would otherwise be NC (Section G).
- ☐ If you have not included an XSYS header, you have devised a method to program the SPI-flash or OTP (Section G).

H.8 GPIO

- ☐ You have not mapped both inputs and outputs to the same multi-bit port.

H.9 Multi device designs

Skip this section if your design only includes a single XMOS device.

- ☐ One device is connected to a SPI flash for booting.
- ☐ Devices that boot from link have MODE2 grounded and MODE3 NC. These device must have link XLB connected to a device to boot from (see 7).
- ☐ If you included an XSYS header, you have included buffers for RST_N, TRST_N, TMS, TCK, MODE2, and MODE3 (Section F).