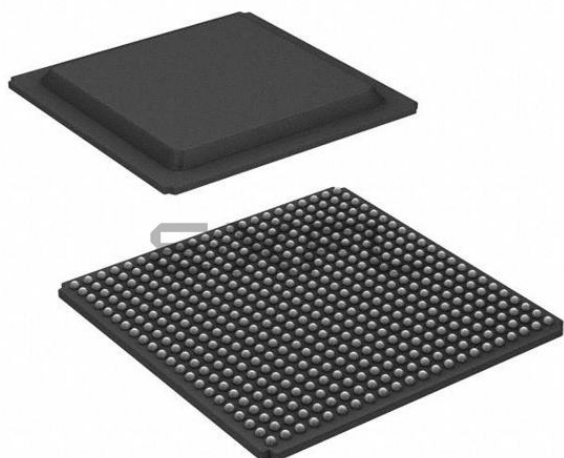




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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	10000
Number of Logic Elements/Cells	128000
Total RAM Bits	9732096
Number of I/O	240
Number of Gates	-
Voltage - Supply	0.95V ~ 1.05V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BBGA
Supplier Device Package	484-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc6vcx130t-1ffg484c

CLB Overview for CXT Devices

Table 5, updated specifically for the CXT family from a similar table in the *Virtex-6 FPGA CLB User Guide*, shows the available resources in all Virtex-6 CXT FPGA CLBs.

Table 5: Virtex-6 CXT FPGA Logic Resources Available in All CLBs

Device	Total Slices	SLICELs	SLICEMs	Number of 6-Input LUTs	Maximum Distributed RAM (Kb)	Shift Register (Kb)	Number of Flip-Flops
XC6VCX75T	11,640	7,460	4,180	46,560	1045	522.5	93,120
XC6VCX130T	20,000	13,040	6,960	80,000	1740	870	160,000
XC6VCX195T	31,200	19,040	12,160	124,800	3140	1570	249,600
XC6VCX240T	37,680	23,080	14,600	150,720	3770	1885	301,440

Regional Clock Management for CXT Devices

Table 6, updated from the *Virtex-6 FPGA Clocking Resources User Guide* specifically for the CXT family, shows the number of clock regions in all Virtex-6 CXT FPGA CLBs.

Table 6: Virtex-6 CXT FPGA Clock Regions

Device	Number of Clock Regions
XC6VCX75T	6
XC6VCX130T	10
XC6VCX195T	10
XC6VCX240T	12

CXT Packaging Specifications

Table 7, updated from the *Virtex-6 FPGA Packaging and Pinout Specifications* specifically for the CXT family, shows the number of GTX transceiver I/O channels. Table 8 shows the number of available I/Os and the number of differential I/O pairs for each Virtex-6 device/package combination.

Table 7: Number of Serial Transceivers (GTs) I/O Channels/Device

I/O Channels	Device			
	CX75T ⁽¹⁾	CX130T ⁽²⁾	CX195T ⁽³⁾	CX240T ⁽⁴⁾
MGTRXP	8 or 12	8, 12, or 16	12 or 16	12 or 16
MGTRXN	8 or 12	8, 12, or 16	12 or 16	12 or 16
MGTTXP	8 or 12	8, 12, or 16	12 or 16	12 or 16
MGTTXN	8 or 12	8, 12, or 16	12 or 16	12 or 16

Notes:

1. The XC6VCX75T has 8 GTX I/O channels in the FF484/FFG484 package and 12 GTX I/O channels in the FF784/FFG784 package.
2. The XC6VCX130T has 8 GTX I/O channels in the FF484/FFG484 package, 12 GTX I/O channels in the FF784/FFG784 package, and 16 GTX I/O channels in the FF1156/FFG1156 package.
3. The XC6VCX195T has 12 GTX I/O channels in the FF784/FFG784 package and 16 GTX I/O channels in the FF1156/FFG1156 package.
4. The XC6VCX240T has 12 GTX I/O channels in the FF784/FFG784 package and 16 GTX I/O channels in the FF1156/FFG1156 package.

Table 8: Available I/O Pin/Device/Package Combinations

Virtex-6 CXT Device	User I/O Pins	Virtex-6 CXT FPGA Package		
		FF484	FF784	FF1156
XC6VCX75T	Available User I/Os	240	360	–
	Differential I/O Pairs	120	180	–
XC6VCX130T	Available User I/Os	240	400	600
	Differential I/O Pairs	120	200	300
XC6VCX195T	Available User I/Os	–	400	600
	Differential I/O Pairs	–	200	300
XC6VCX240T	Available User I/Os	–	400	600
	Differential I/O Pairs	–	200	300

GTX Transceivers in CXT Devices

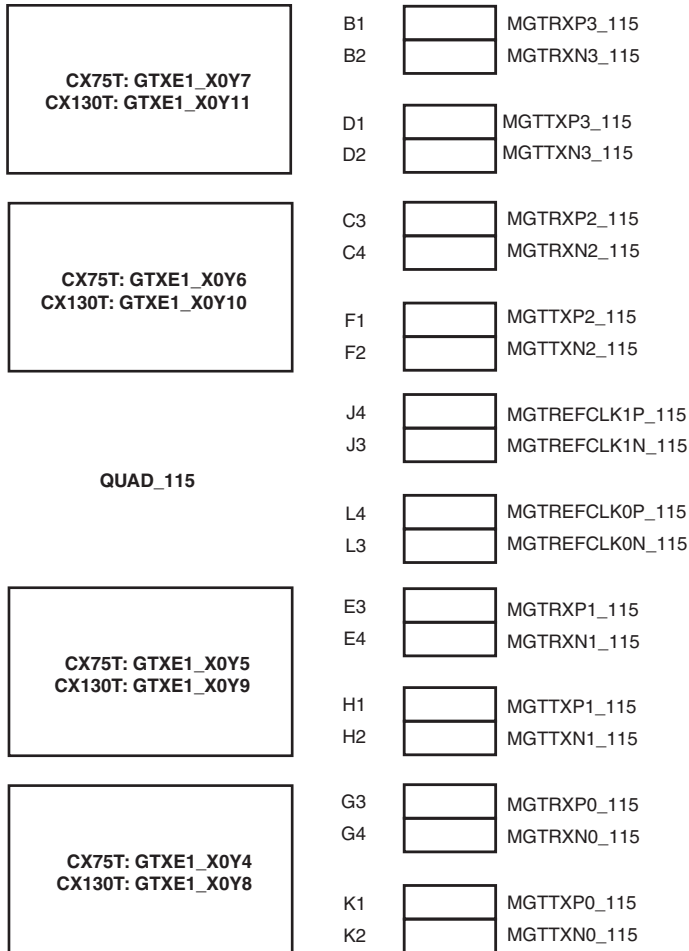
CXT devices have between 8 to 16 gigabit transceiver circuits. Each GTX transceiver is a combined transmitter and receiver capable of operating at a data rate between 480 Mb/s and 3.75 Gb/s. Lower data rates can be achieved using FPGA logic-based oversampling. The transmitter and receiver are independent circuits that use separate PLLs to multiply the reference frequency input by certain programmable numbers between 2 and 25, to become the bit-serial data clock. Each GTX transceiver has a large number of user-definable features and parameters. All of these can be defined during device configuration, and many can also be modified during operation.

FF484 Package Placement Diagrams

Figure 2 and Figure 3 show the placement diagrams for the GTX transceivers in the FF484 package.

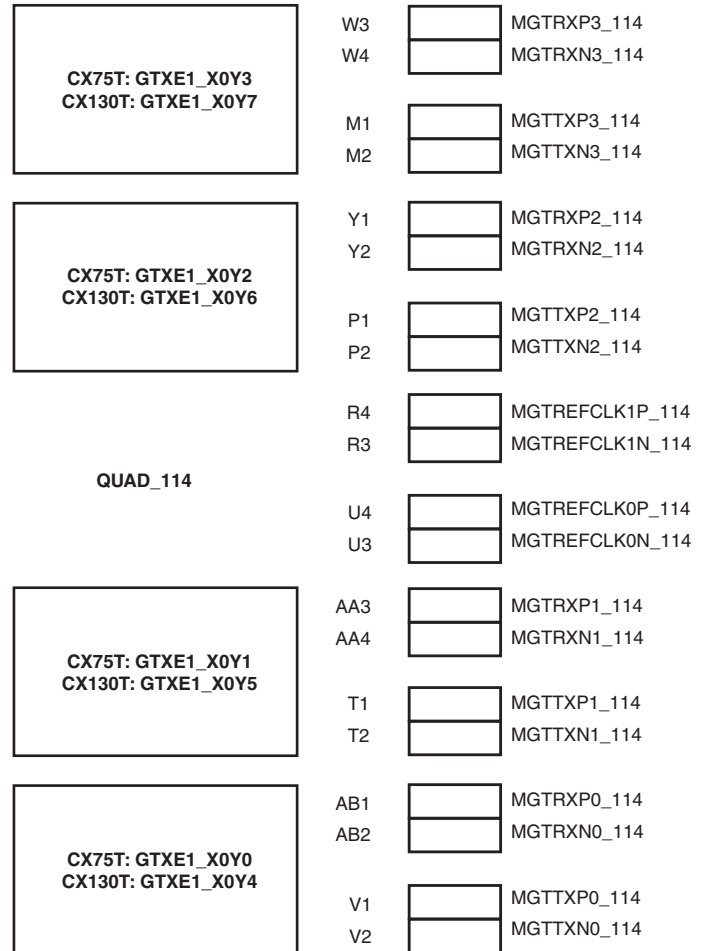
Note: Unbonded locations in the FF484 package are:

- CX75T: X0Y8, X0Y9, X0Y10, X0Y11
- CX130T: X0Y0, X0Y1, X0Y2, X0Y3, and X0Y12, X0Y13, X0Y14, X0Y15



ds153_02_041510

Figure 2: Placement Diagram for the FF484 Package
(1 of 2)



ds153_03_041510

Figure 3: Placement Diagram for the FF484 Package
(2 of 2)

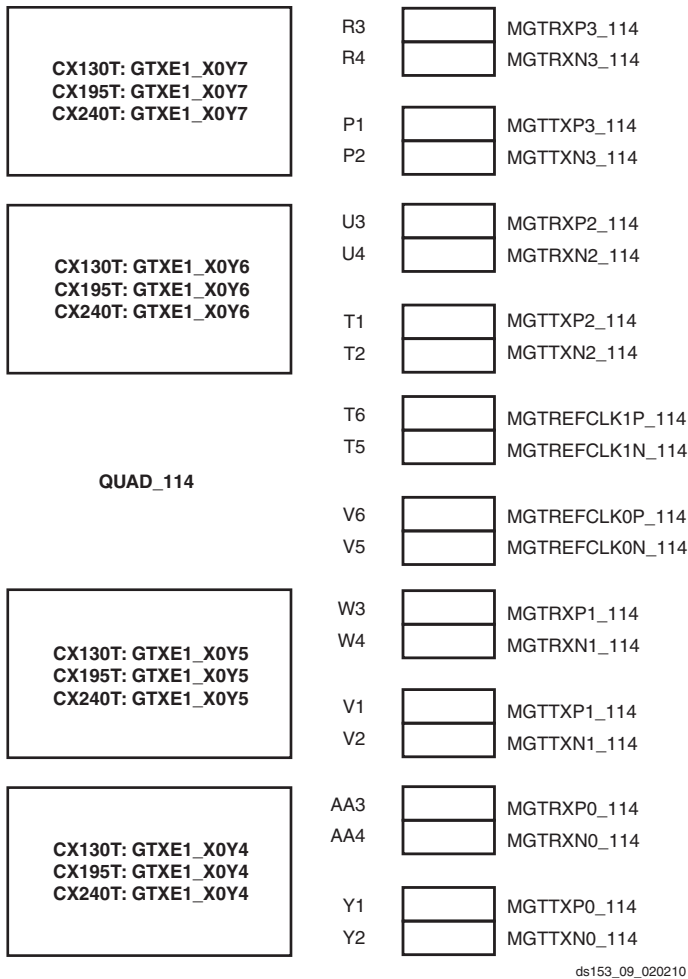


Figure 9: Placement Diagram for the FF1156 Package
(3 of 4)

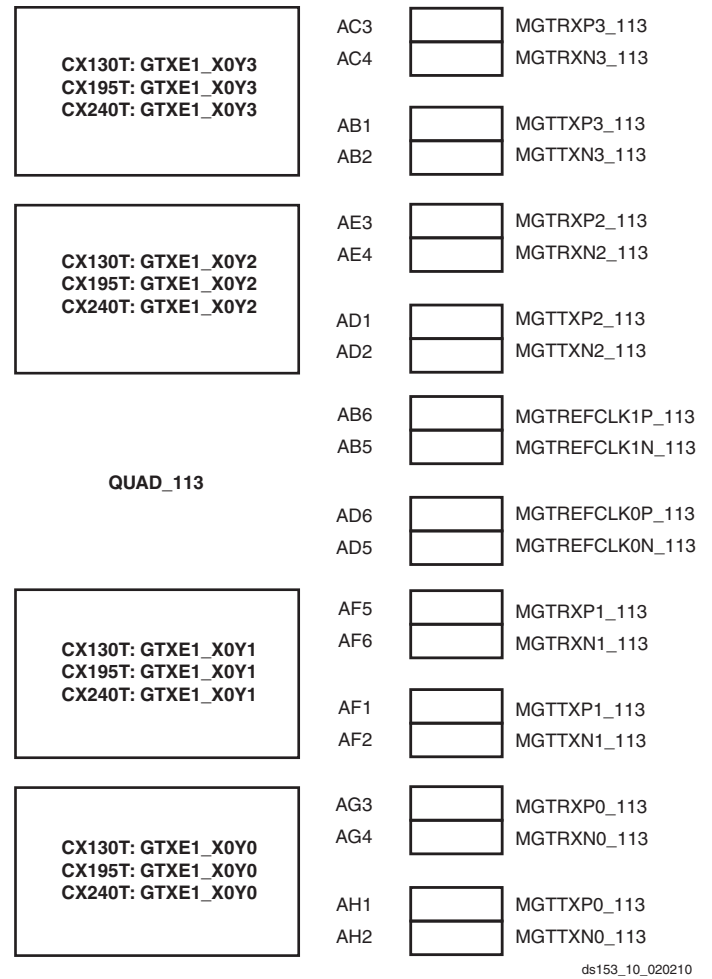


Figure 10: Placement Diagram for the FF1156 Package
(4 of 4)

Table 10: Recommended Operating Conditions

Symbol	Description	Min	Max	Units
V_{CCINT}	Internal supply voltage relative to GND, $T_j = 0^\circ\text{C}$ to $+85^\circ\text{C}$	0.95	1.05	V
	Internal supply voltage relative to GND, $T_j = -40^\circ\text{C}$ to $+100^\circ\text{C}$	0.95	1.05	V
V_{CCAUX}	Auxiliary supply voltage relative to GND, $T_j = 0^\circ\text{C}$ to $+85^\circ\text{C}$	2.375	2.625	V
	Auxiliary supply voltage relative to GND, $T_j = -40^\circ\text{C}$ to $+100^\circ\text{C}$	2.375	2.625	V
$V_{CCO}^{(1)(2)(3)}$	Supply voltage relative to GND, $T_j = 0^\circ\text{C}$ to $+85^\circ\text{C}$	1.14	2.625	V
	Supply voltage relative to GND, $T_j = -40^\circ\text{C}$ to $+100^\circ\text{C}$	1.14	2.625	V
V_{IN}	2.5V supply voltage relative to GND, $T_j = 0^\circ\text{C}$ to $+85^\circ\text{C}$	GND – 0.20	2.625	V
	2.5V supply voltage relative to GND, $T_j = -40^\circ\text{C}$ to $+100^\circ\text{C}$	GND – 0.20	2.625	V
	2.5V and below supply voltage relative to GND, $T_j = 0^\circ\text{C}$ to $+85^\circ\text{C}$	GND – 0.20	$V_{CCO} + 0.2$	V
	2.5V and below supply voltage relative to GND, $T_j = -40^\circ\text{C}$ to $+100^\circ\text{C}$	GND – 0.20	$V_{CCO} + 0.2$	V
$I_{IN}^{(4)}$	Maximum current through any pin in a powered or unpowered bank when forward biasing the clamp diode.	–	10	mA
$V_{BATT}^{(5)}$	Battery voltage relative to GND, $T_j = 0^\circ\text{C}$ to $+85^\circ\text{C}$	1.0	2.5	V
	Battery voltage relative to GND, $T_j = -40^\circ\text{C}$ to $+100^\circ\text{C}$	1.0	2.5	V
$V_{FS}^{(6)}$	External voltage supply for eFUSE programming	2.375	2.625	V

Notes:

1. Configuration data is retained even if V_{CCO} drops to 0V.
2. Includes V_{CCO} of 1.2V, 1.5V, 1.8V, and 2.5V.
3. The configuration supply voltage V_{CC_CONFIG} is also known as V_{CCO_0} .
4. A total of 100 mA per bank should not be exceeded.
5. V_{BATT} is required only when using bitstream encryption. If battery is not used, connect V_{BATT} to either ground or V_{CCAUX} .
6. When not programming eFUSE, connect V_{FS} to GND.
7. All voltages are relative to ground.

Table 11: DC Characteristics Over Recommended Operating Conditions⁽¹⁾⁽²⁾

Symbol	Description	Min	Typ	Max	Units
V_{DRINT}	Data retention V_{CCINT} voltage (below which configuration data might be lost)	0.75	–	–	V
V_{DRI}	Data retention V_{CCAUX} voltage (below which configuration data might be lost)	2.0	–	–	V
I_{REF}	V_{REF} leakage current per pin	–	–	10	μA
I_L	Input or output leakage current per pin (sample-tested)	–	–	10	μA
$C_{IN}^{(3)}$	Die input capacitance at the pad	–	–	8	pF
I_{RPU}	Pad pull-up (when selected) @ $V_{IN} = 0\text{V}$, $V_{CCO} = 2.5\text{V}$	20	–	80	μA
	Pad pull-up (when selected) @ $V_{IN} = 0\text{V}$, $V_{CCO} = 1.8\text{V}$	8	–	40	μA
	Pad pull-up (when selected) @ $V_{IN} = 0\text{V}$, $V_{CCO} = 1.5\text{V}$	5	–	30	μA
	Pad pull-up (when selected) @ $V_{IN} = 0\text{V}$, $V_{CCO} = 1.2\text{V}$	1	–	20	μA
I_{RPD}	Pad pull-down (when selected) @ $V_{IN} = 2.5\text{V}$	3	–	80	μA
I_{BATT}	Battery supply current	–	–	150	nA
n	Temperature diode ideality factor	–	1.0002	–	n
r	Series resistance	–	5	–	Ω

Notes:

1. Typical values are specified at nominal voltage, 25°C .
2. Maximum value specified for worst case process at 25°C .
3. This measurement represents the die capacitance at the pad, not including the package.

Quiescent Supply Current: Important Note

Typical values for quiescent supply current are specified at nominal voltage, 85°C junction temperatures (T_j). Xilinx recommends analyzing static power consumption at $T_j = 85^\circ\text{C}$ because the majority of designs operate near the high end of the commercial temperature range. Quiescent supply current is specified by speed grade for Virtex-6 CXT devices. Use the XPOWER™ Estimator (XPE) spreadsheet tool (download at <http://www.xilinx.com/power>) to calculate static power consumption for conditions other than those specified in Table 12.

Table 12: Typical Quiescent Supply Current

Symbol	Description	Device	Speed and Temperature Grade		Units
			-2 (C & I)	-1 (C & I)	
I_{CCINTQ}	Quiescent V_{CCINT} supply current	XC6VCX75T	927	927	mA
		XC6VCX130T	1563	1563	mA
		XC6VCX195T	2059	2059	mA
		XC6VCX240T	2478	2478	mA
I_{CCOQ}	Quiescent V_{CCO} supply current	XC6VCX75T	1	1	mA
		XC6VCX130T	1	1	mA
		XC6VCX195T	1	1	mA
		XC6VCX240T	2	2	mA
I_{CCAUXQ}	Quiescent V_{CCAUX} supply current	XC6VCX75T	45	45	mA
		XC6VCX130T	75	75	mA
		XC6VCX195T	113	113	mA
		XC6VCX240T	135	135	mA

Notes:

1. Typical values are specified at nominal voltage, 85°C junction temperatures (T_j). Industrial (I) grade devices have the same typical values as commercial (C) grade devices at 85°C, but higher values at 100°C. Use the XPE tool to calculate 100°C values.
2. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
3. If DCI or differential signaling is used, more accurate quiescent current estimates can be obtained by using the XPOWER Estimator (XPE) or XPOWER Analyzer (XPA) tools.

Power-On Power Supply Requirements

Xilinx FPGAs require a certain amount of supply current during power-on to insure proper device initialization. The actual current consumed depends on the power-on ramp rate of the power supply.

Virtex-6 CXT devices require a power-on sequence of V_{CCINT} , V_{CCAUX} , and V_{CCO} . If the requirement can not be met, then V_{CCAUX} must always be powered prior to V_{CCO} . V_{CCAUX} and V_{CCO} can be powered by the same supply, therefore, both V_{CCAUX} and V_{CCO} are permitted to ramp simultaneously. Similarly, for the power-down sequence, V_{CCO} must be powered down prior to V_{CCAUX} or if powered by the same supply, V_{CCAUX} and V_{CCO} power-down simultaneously.

Table 13 shows the minimum current, in addition to I_{CCOQ} , that are required by Virtex-6 CXT devices for proper power-on and configuration. If the current minimums shown in Table 12 and Table 13 are met, the device powers on after all three supplies have passed through their power-on reset threshold voltages. The FPGA must be configured after V_{CCINT} is applied.

Once initialized and configured, use the XPOWER tools to estimate current drain on these supplies.

Table 13: Power-On Current for Virtex-6 CXT Devices

Device	$I_{CCINTMIN}$	$I_{CCAUXMIN}$	I_{CCOMIN}	Units
	Typ ⁽¹⁾	Typ ⁽¹⁾	Typ ⁽¹⁾	
XC6VCX75T	See I_{CCINTQ} in Table 12	$I_{CCAUXQ} + 10$	$I_{CCOQ} + 30$ mA per bank	mA
XC6VCX130T	See I_{CCINTQ} in Table 12	$I_{CCAUXQ} + 10$	$I_{CCOQ} + 30$ mA per bank	mA
XC6VCX195T	See I_{CCINTQ} in Table 12	$I_{CCAUXQ} + 40$	$I_{CCOQ} + 30$ mA per bank	mA
XC6VCX240T	See I_{CCINTQ} in Table 12	$I_{CCAUXQ} + 40$	$I_{CCOQ} + 30$ mA per bank	mA

Notes:

1. Typical values are specified at nominal voltage, 25°C.
2. Use the XPOWER™ Estimator (XPE) spreadsheet tool (download at <http://www.xilinx.com/power>) to calculate maximum power-on currents.

Table 14: Power Supply Ramp Time

Symbol	Description	Ramp Time	Units
V_{CCINT}	Internal supply voltage relative to GND	0.20 to 50.0	ms
V_{CCO}	Output drivers supply voltage relative to GND	0.20 to 50.0	ms
V_{CCAUX}	Auxiliary supply voltage relative to GND	0.20 to 50.0	ms

SelectIO™ DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

Table 15: SelectIO DC Input and Output Levels

I/O Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
LVC MOS25, LVDCI25	-0.3	0.7	1.7	$V_{CCO} + 0.3$	0.4	$V_{CCO} - 0.4$	Note(3)	Note(3)
LVC MOS18, LVDCI18	-0.3	35% V_{CCO}	65% V_{CCO}	$V_{CCO} + 0.3$	0.45	$V_{CCO} - 0.45$	Note(4)	Note(4)
LVC MOS15, LVDCI15	-0.3	35% V_{CCO}	65% V_{CCO}	$V_{CCO} + 0.3$	25% V_{CCO}	75% V_{CCO}	Note(4)	Note(4)
LVC MOS12	-0.3	35% V_{CCO}	65% V_{CCO}	$V_{CCO} + 0.3$	25% V_{CCO}	75% V_{CCO}	Note(5)	Note(5)
HSTL I ₁₂	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	$V_{CCO} + 0.3$	25% V_{CCO}	75% V_{CCO}	6.3	6.3
HSTL I ⁽²⁾	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	$V_{CCO} + 0.3$	0.4	$V_{CCO} - 0.4$	8	-8
HSTL II ⁽²⁾	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	$V_{CCO} + 0.3$	0.4	$V_{CCO} - 0.4$	16	-16
HSTL III ⁽²⁾	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	$V_{CCO} + 0.3$	0.4	$V_{CCO} - 0.4$	24	-8
DIFF HSTL I ⁽²⁾	-0.3	50% $V_{CCO} - 0.1$	50% $V_{CCO} + 0.1$	$V_{CCO} + 0.3$	—	—	—	—
DIFF HSTL II ⁽²⁾	-0.3	50% $V_{CCO} - 0.1$	50% $V_{CCO} + 0.1$	$V_{CCO} + 0.3$	—	—	—	—
SSTL2 I	-0.3	$V_{REF} - 0.15$	$V_{REF} + 0.15$	$V_{CCO} + 0.3$	$V_{TT} - 0.61$	$V_{TT} + 0.61$	8.1	-8.1
SSTL2 II	-0.3	$V_{REF} - 0.15$	$V_{REF} + 0.15$	$V_{CCO} + 0.3$	$V_{TT} - 0.81$	$V_{TT} + 0.81$	16.2	-16.2
DIFF SSTL2 I	-0.3	50% $V_{CCO} - 0.15$	50% $V_{CCO} + 0.15$	$V_{CCO} + 0.3$	—	—	—	—
DIFF SSTL2 II	-0.3	50% $V_{CCO} - 0.15$	50% $V_{CCO} + 0.15$	$V_{CCO} + 0.3$	—	—	—	—
SSTL18 I	-0.3	$V_{REF} - 0.125$	$V_{REF} + 0.125$	$V_{CCO} + 0.3$	$V_{TT} - 0.47$	$V_{TT} + 0.47$	6.7	-6.7
SSTL18 II	-0.3	$V_{REF} - 0.125$	$V_{REF} + 0.125$	$V_{CCO} + 0.3$	$V_{TT} - 0.60$	$V_{TT} + 0.60$	13.4	-13.4
DIFF SSTL18 I	-0.3	50% $V_{CCO} - 0.125$	50% $V_{CCO} + 0.125$	$V_{CCO} + 0.3$	—	—	—	—
DIFF SSTL18 II	-0.3	50% $V_{CCO} - 0.125$	50% $V_{CCO} + 0.125$	$V_{CCO} + 0.3$	—	—	—	—
SSTL15	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	$V_{CCO} + 0.3$	$V_{TT} - 0.175$	$V_{TT} + 0.175$	14.3	14.3

Notes:

1. Tested according to relevant specifications.
2. Applies to both 1.5V and 1.8V HSTL.
3. Using drive strengths of 2, 4, 6, 8, 12, 16, or 24 mA.
4. Using drive strengths of 2, 4, 6, 8, 12, or 16 mA.
5. Supported drive strengths of 2, 4, 6, or 8 mA.
6. For detailed interface specific DC voltage levels, see the *Virtex-6 FPGA SelectIO Resources User Guide*.

HT DC Specifications (HT_25)

Table 16: HT DC Specifications

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply Voltage		2.38	2.5	2.63	V
V_{OD}	Differential Output Voltage	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	480	600	885	mV
ΔV_{OD}	Change in V_{OD} Magnitude		-15	-	15	mV
V_{OCM}	Output Common Mode Voltage	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	480	600	885	mV
ΔV_{OCM}	Change in V_{OCM} Magnitude		-15	-	15	mV
V_{ID}	Input Differential Voltage		200	600	1000	mV
ΔV_{ID}	Change in V_{ID} Magnitude		-15	-	15	mV
V_{ICM}	Input Common Mode Voltage		440	600	780	mV
ΔV_{ICM}	Change in V_{ICM} Magnitude		-15	-	15	mV

LVDS DC Specifications (LVDS_25)

Table 17: LVDS DC Specifications

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply Voltage		2.38	2.5	2.63	V
V_{OH}	Output High Voltage for Q and $\overline{Q}$	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	-	-	1.675	V
V_{OL}	Output Low Voltage for Q and $\overline{Q}$	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	0.825	-	-	V
V_{ODIFF}	Differential Output Voltage (Q - $\overline{Q}$), Q = High ($\overline{Q}$ - Q), $\overline{Q}$ = High	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	247	350	600	mV
V_{OCM}	Output Common-Mode Voltage	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	1.075	1.250	1.425	V
V_{IDIFF}	Differential Input Voltage (Q - $\overline{Q}$), Q = High ($\overline{Q}$ - Q), $\overline{Q}$ = High		100	350	600	mV
V_{ICM}	Input Common-Mode Voltage		0.3	1.2	2.2	V

Extended LVDS DC Specifications (LVDSEXT_25)

Table 18: Extended LVDS DC Specifications

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply Voltage		2.38	2.5	2.63	V
V_{OH}	Output High Voltage for Q and $\overline{Q}$	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	-	-	1.785	V
V_{OL}	Output Low Voltage for Q and $\overline{Q}$	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	0.715	-	-	V
V_{ODIFF}	Differential Output Voltage (Q - $\overline{Q}$), Q = High ($\overline{Q}$ - Q), $\overline{Q}$ = High	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	350	-	840	mV
V_{OCM}	Output Common-Mode Voltage	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	1.075	1.250	1.425	V
V_{IDIFF}	Differential Input Voltage (Q - $\overline{Q}$), Q = High ($\overline{Q}$ - Q), $\overline{Q}$ = High	Common-mode input voltage = 1.25V	100	-	1000	mV
V_{ICM}	Input Common-Mode Voltage	Differential input voltage = ± 350 mV	0.3	1.2	2.2	V

LVPECL DC Specifications (LVPECL_25)

These values are valid when driving a 100Ω differential load only, i.e., a 100Ω resistor between the two receiver pins. The V_{OH} levels are 200 mV below standard LVPECL levels and are compatible with devices tolerant of lower common-mode ranges. Table 19 summarizes the DC output specifications of LVPECL. For more information on using LVPECL, see the *Virtex-6 FPGA SelectIO Resources User Guide*.

Table 19: LVPECL DC Specifications

Symbol	DC Parameter	Min	Typ	Max	Units
V_{OH}	Output High Voltage	$V_{CC} - 1.025$	1.545	$V_{CC} - 0.88$	V
V_{OL}	Output Low Voltage	$V_{CC} - 1.81$	0.795	$V_{CC} - 1.62$	V
V_{ICM}	Input Common-Mode Voltage	0.6	—	2.2	V
V_{IDIFF}	Differential Input Voltage ⁽¹⁾⁽²⁾	0.100	—	1.5	V

Notes:

1. Recommended input maximum voltage not to exceed $V_{CCAUX} + 0.2V$.
2. Recommended input minimum voltage not to go below $-0.5V$.

eFUSE Read Endurance

Table 20 lists the maximum number of read cycle operations expected. For more information, see the *Virtex-6 FPGA Configuration User Guide*.

Table 20: eFUSE Read Endurance

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
DNA_CYCLES	Number of DNA_PORT READ operations or JTAG ISC_DNA read command operations. Unaffected by SHIFT operations.	30,000,000				Read Cycles
AES_CYCLES	Number of JTAG FUSE_KEY or FUSE_CNTL read command operations. Unaffected by SHIFT operations.	30,000,000				Read Cycles

GTX Transceiver Specifications

GTX Transceiver DC Characteristics

Table 21: Absolute Maximum Ratings for GTX Transceivers⁽¹⁾

Symbol	Description	Min	Max	Units
MGTAVCC	Analog supply voltage for the GTX transmitter and receiver circuits relative to GND	-0.5	1.1	V
MGTAVTT	Analog supply voltage for the GTX transmitter and receiver termination circuits relative to GND	-0.5	1.32	V
MGTAVTTRCAL	Analog supply voltage for the resistor calibration circuit of the GTX transceiver column	-0.5	1.32	V
V_{IN}	Receiver (RXP/RXN) and Transmitter (TXP/TXN) absolute input voltage	-0.5	1.32	V
$V_{MGTRFCLK}$	Reference clock absolute input voltage	-0.5	1.32	V

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.

Table 22: Recommended Operating Conditions for GTX Transceivers⁽¹⁾⁽²⁾

Symbol	Description	Min	Typ	Max	Units
MGTAVCC	Analog supply voltage for the GTX transmitter and receiver circuits relative to GND	0.95	1.0	1.06	V
MGTAVTT	Analog supply voltage for the GTX transmitter and receiver termination circuits relative to GND	1.14	1.2	1.26	V
MGTAVTTRCAL	Analog supply voltage for the resistor calibration circuit of the GTX transceiver column	1.14	1.2	1.26	V

Notes:

- Each voltage listed requires the filter circuit described in *Virtex-6 FPGA GTX Transceivers User Guide*.
- Voltages are specified for the temperature range of $T_j = -40^{\circ}\text{C}$ to $+100^{\circ}\text{C}$.

Table 23: GTX Transceiver Supply Current (per Lane) ⁽¹⁾⁽²⁾

Symbol	Description	Typ	Max	Units
I _{MGTAVTT}	MGTAVTT supply current for one GTX transceiver	55.9	Note 2	mA
I _{MGTAVCC}	MGTAVCC supply current for one GTX transceiver	56.1		mA
MGTR _{REF}	Precision reference resistor for internal calibration termination	100.0 ± 1% tolerance		Ω

Notes:

- Typical values are specified at nominal voltage, 25°C, with a 3.125 Gb/s line rate.
- Values for currents other than the values specified in this table can be obtained by using the XPOWER Estimator (XPE) or XPOWER Analyzer (XPA) tools.

Table 24: GTX Transceiver Quiescent Supply Current (per Lane)⁽¹⁾⁽²⁾⁽³⁾

Symbol	Description	Typ ⁽⁴⁾	Max	Units
I_{MGTAVTTQ}	Quiescent MGTAVTT supply current for one GTX transceiver	0.9	Note 2	mA
I_{MGTAVCCQ}	Quiescent MGTAVCC supply current for one GTX transceiver	3.5		mA

Notes:

- Device powered and unconfigured.
- Currents for conditions other than values specified in this table can be obtained by using the XPOWER Estimator (XPE) or XPOWER Analyzer (XPA) tools.
- GTX transceiver quiescent supply current for an entire device can be calculated by multiplying the values in this table by the number of available GTX transceivers.
- Typical values are specified at nominal voltage, 25°C.

GTX Transceiver DC Input and Output Levels

Table 25 summarizes the DC output specifications of the GTX transceivers in Virtex-6 CXT FPGAs. Consult the *Virtex-6 FPGA GTX Transceivers User Guide* for further details.

Table 25: GTX Transceiver DC Specifications

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
DV _{PPIN}	Differential peak-to-peak input voltage	External AC coupled	125	–	2000	mV
V _{IN}	Absolute input voltage	DC coupled MGTA VTT = 1.2V	–400	–	MGTA VTT	mV
V _{CMIN}	Common mode input voltage	DC coupled MGTA VTT = 1.2V	–	2/3 MGTA VTT	–	mV
DV _{PPOUT}	Differential peak-to-peak output voltage ⁽¹⁾	Transmitter output swing is set to maximum setting	–	–	1000	mV
V _{CMOUTDC}	DC common mode output voltage	Equation based	MGTA VTT – DV _{PPOUT} /4			mV
R _{IN}	Differential input resistance		80	100	130	Ω
R _{OUT}	Differential output resistance		80	100	120	Ω
T _{OSKEW}	Transmitter output pair (TXP and TXN) intra-pair skew		–	2	8	ps
C _{EXT}	Recommended external AC coupling capacitor ⁽²⁾		–	100	–	nF

Notes:

1. The output swing and preemphasis levels are programmable using the attributes discussed in *Virtex-6 FPGA GTX Transceivers User Guide* and can result in values lower than reported in this table.
2. Other values can be used as appropriate to conform to specific protocols and standards.

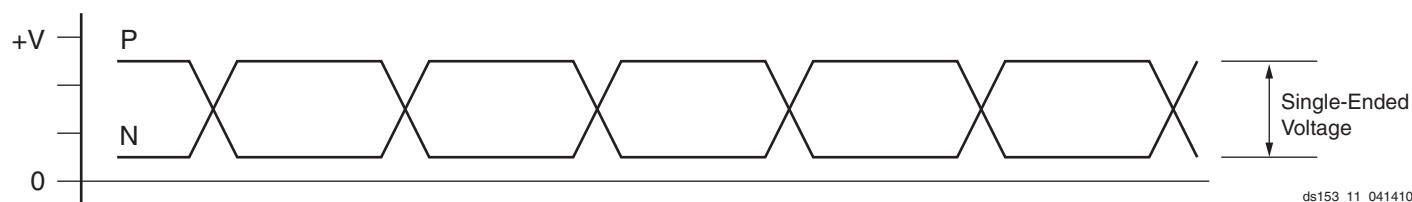


Figure 11: Single-Ended Peak-to-Peak Voltage

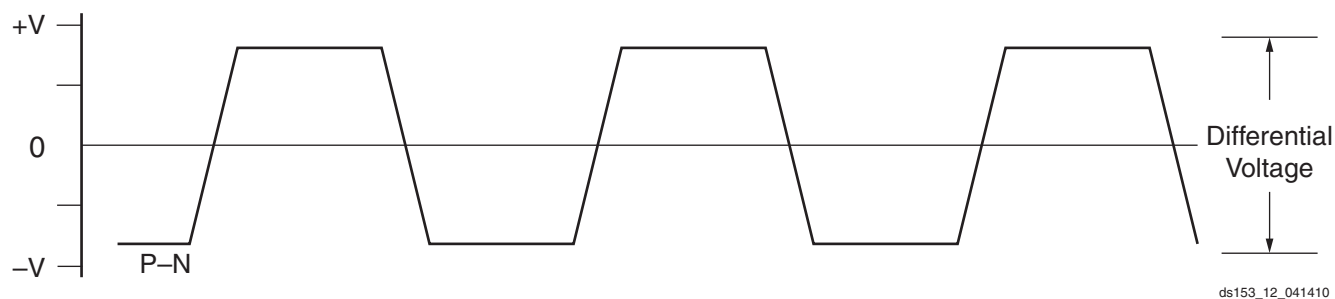


Figure 12: Differential Peak-to-Peak Voltage

Table 30: GTX Transceiver User Clock Switching Characteristics⁽¹⁾

Symbol	Description	Conditions	Speed Grade		Units
			-2	-1	
F _{TXOUT}	TXOUTCLK maximum frequency	Internal 20-bit data path	187.5	187.5	MHz
		Internal 16-bit data path	234.38	234.38	MHz
F _{RXREC}	RXRECCLK maximum frequency	Internal 20-bit data path	187.5	187.5	MHz
		Internal 16-bit data path	234.38	234.38	MHz
T _{RX}	RXUSRCLK maximum frequency		234.38	234.38	MHz
T _{RX2}	RXUSRCLK2 maximum frequency	1 byte interface	376	312.5	MHz
		2 byte interface	234.38	234.38	MHz
		4 byte interface	117.19	117.19	MHz
T _{TX}	TXUSRCLK maximum frequency		234.38	234.38	MHz
T _{TX2}	TXUSRCLK2 maximum frequency	1 byte interface	376	312.5	MHz
		2 byte interface	234.38	234.38	MHz
		4 byte interface	117.19	117.19	MHz

Notes:

1. Clocking must be implemented as described in *Virtex-6 FPGA GTX Transceivers User Guide*.

Table 31: GTX Transceiver Transmitter Switching Characteristics

Symbol	Description	Condition	Min	Typ	Max	Units
F _{GTXTX}	Serial data rate range		0.480	—	F _{GTXMAX}	Gb/s
T _{RTX}	TX Rise time	20%–80%	—	120	—	ps
T _{FTX}	TX Fall time	80%–20%	—	120	—	ps
T _{LLSKEW}	TX lane-to-lane skew ⁽¹⁾		—	—	350	ps
V _{TXOOBVDPP}	Electrical idle amplitude		—	—	15	mV
T _{TXOOBTRANSITION}	Electrical idle transition time		—	—	75	ns
T _{J3.75}	Total Jitter ⁽²⁾⁽³⁾	3.75 Gb/s	—	—	0.34	UI
D _{J3.75}	Deterministic Jitter ⁽²⁾⁽³⁾		—	—	0.16	UI
T _{J3.125}	Total Jitter ⁽²⁾⁽³⁾	3.125 Gb/s	—	—	0.2	UI
D _{J3.125}	Deterministic Jitter ⁽²⁾⁽³⁾		—	—	0.1	UI
T _{J3.125L}	Total Jitter ⁽²⁾⁽³⁾	3.125 Gb/s ⁽⁴⁾	—	—	0.35	UI
D _{J3.125L}	Deterministic Jitter ⁽²⁾⁽³⁾		—	—	0.16	UI
T _{J2.5}	Total Jitter ⁽²⁾⁽³⁾	2.5 Gb/s ⁽⁵⁾	—	—	0.20	UI
D _{J2.5}	Deterministic Jitter ⁽²⁾⁽³⁾		—	—	0.08	UI
T _{J1.25}	Total Jitter ⁽²⁾⁽³⁾	1.25 Gb/s ⁽⁶⁾	—	—	0.15	UI
D _{J1.25}	Deterministic Jitter ⁽²⁾⁽³⁾		—	—	0.06	UI
T _{J600}	Total Jitter ⁽²⁾⁽³⁾	600 Mb/s	—	—	0.1	UI
D _{J600}	Deterministic Jitter ⁽²⁾⁽³⁾		—	—	0.03	UI

IOB Pad Input/Output/3-State Switching Characteristics

Table 38 summarizes the values of standard-specific data input delay adjustments, output delays terminating at pads (based on standard) and 3-state delays.

T_{IOPI} is described as the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.

T_{IOOP} is described as the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.

T_{IOTP} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer.

Table 39 summarizes the value of T_{IOTPHZ} . T_{IOTPHZ} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is enabled (i.e., a high impedance state).

Table 38: IOB Switching Characteristics

I/O Standard	T _{IOPI}		T _{IOOP}		T _{IOTP}		Units
	Speed Grade		Speed Grade		Speed Grade		
	-2	-1	-2	-1	-2	-1	
LVDS_25	1.09	1.09	1.68	1.68	1.68	1.68	ns
LVDSEXT_25	1.09	1.09	1.84	1.84	1.84	1.84	ns
HT_25	1.09	1.09	1.78	1.78	1.78	1.78	ns
BLVDS_25	1.09	1.09	1.67	1.67	1.67	1.67	ns
RSDS_25 (point to point)	1.09	1.09	1.68	1.68	1.68	1.68	ns
HSTL_I	1.06	1.06	1.73	1.73	1.73	1.73	ns
HSTL_II	1.06	1.06	1.74	1.74	1.74	1.74	ns
HSTL_III	1.06	1.06	1.71	1.71	1.71	1.71	ns
HSTL_I_18	1.06	1.06	1.75	1.75	1.75	1.75	ns
HSTL_II_18	1.06	1.06	1.81	1.81	1.81	1.81	ns
HSTL_III_18	1.06	1.06	1.71	1.71	1.71	1.71	ns
SSTL2_I	1.06	1.06	1.77	1.77	1.77	1.77	ns
SSTL2_II	1.06	1.06	1.72	1.72	1.72	1.72	ns
SSTL15	1.06	1.06	1.71	1.71	1.71	1.71	ns
LVC MOS25, Slow, 2 mA	0.66	0.66	6.01	6.01	6.01	6.01	ns
LVC MOS25, Slow, 4 mA	0.66	0.66	3.79	3.79	3.79	3.79	ns
LVC MOS25, Slow, 6 mA	0.66	0.66	3.08	3.08	3.08	3.08	ns
LVC MOS25, Slow, 8 mA	0.66	0.66	2.72	2.72	2.72	2.72	ns
LVC MOS25, Slow, 12 mA	0.66	0.66	2.17	2.17	2.17	2.17	ns
LVC MOS25, Slow, 16 mA	0.66	0.66	2.29	2.29	2.29	2.29	ns
LVC MOS25, Slow, 24 mA	0.66	0.66	2.02	2.02	2.02	2.02	ns
LVC MOS25, Fast, 2 mA	0.66	0.66	6.04	6.04	6.04	6.04	ns
LVC MOS25, Fast, 4 mA	0.66	0.66	3.82	3.82	3.82	3.82	ns
LVC MOS25, Fast, 6 mA	0.66	0.66	2.99	2.99	2.99	2.99	ns
LVC MOS25, Fast, 8 mA	0.66	0.66	2.65	2.65	2.65	2.65	ns
LVC MOS25, Fast, 12 mA	0.66	0.66	2.08	2.08	2.08	2.08	ns
LVC MOS25, Fast, 16 mA	0.66	0.66	2.13	2.13	2.13	2.13	ns
LVC MOS25, Fast, 24 mA	0.66	0.66	1.99	1.99	1.99	1.99	ns

Table 38: IOB Switching Characteristics (Cont'd)

I/O Standard	T _{IOPI}		T _{IOOP}		T _{IOTP}		Units
	Speed Grade		Speed Grade		Speed Grade		
	-2	-1	-2	-1	-2	-1	
LVC MOS18, Slow, 2 mA	0.71	0.71	4.87	4.87	4.87	4.87	ns
LVC MOS18, Slow, 4 mA	0.71	0.71	3.21	3.21	3.21	3.21	ns
LVC MOS18, Slow, 6 mA	0.71	0.71	2.64	2.64	2.64	2.64	ns
LVC MOS18, Slow, 8 mA	0.71	0.71	2.27	2.27	2.27	2.27	ns
LVC MOS18, Slow, 12 mA	0.71	0.71	2.15	2.15	2.15	2.15	ns
LVC MOS18, Slow, 16 mA	0.71	0.71	2.11	2.11	2.11	2.11	ns
LVC MOS18, Fast, 2 mA	0.71	0.71	4.57	4.57	4.57	4.57	ns
LVC MOS18, Fast, 4 mA	0.71	0.71	2.97	2.97	2.97	2.97	ns
LVC MOS18, Fast, 6 mA	0.71	0.71	2.46	2.46	2.46	2.46	ns
LVC MOS18, Fast, 8 mA	0.71	0.71	2.13	2.13	2.13	2.13	ns
LVC MOS18, Fast, 12 mA	0.71	0.71	1.97	1.97	1.97	1.97	ns
LVC MOS18, Fast, 16 mA	0.71	0.71	1.91	1.91	1.91	1.91	ns
LVC MOS15, Slow, 2 mA	0.85	0.85	4.29	4.29	4.29	4.29	ns
LVC MOS15, Slow, 4 mA	0.85	0.85	3.10	3.10	3.10	3.10	ns
LVC MOS15, Slow, 6 mA	0.85	0.85	2.68	2.68	2.68	2.68	ns
LVC MOS15, Slow, 8 mA	0.85	0.85	2.23	2.23	2.23	2.23	ns
LVC MOS15, Slow, 12 mA	0.85	0.85	2.13	2.13	2.13	2.13	ns
LVC MOS15, Slow, 16 mA	0.85	0.85	2.04	2.04	2.04	2.04	ns
LVC MOS15, Fast, 2 mA	0.85	0.85	4.28	4.28	4.28	4.28	ns
LVC MOS15, Fast, 4 mA	0.85	0.85	2.78	2.78	2.78	2.78	ns
LVC MOS15, Fast, 6 mA	0.85	0.85	2.42	2.42	2.42	2.42	ns
LVC MOS15, Fast, 8 mA	0.85	0.85	2.11	2.11	2.11	2.11	ns
LVC MOS15, Fast, 12 mA	0.85	0.85	1.97	1.97	1.97	1.97	ns
LVC MOS15, Fast, 16 mA	0.85	0.85	1.96	1.96	1.96	1.96	ns
LVC MOS12, Slow, 2 mA	0.93	0.93	3.75	3.75	3.75	3.75	ns
LVC MOS12, Slow, 4 mA	0.93	0.93	2.93	2.93	2.93	2.93	ns
LVC MOS12, Slow, 6 mA	0.93	0.93	2.41	2.41	2.41	2.41	ns
LVC MOS12, Slow, 8 mA	0.93	0.93	2.25	2.25	2.25	2.25	ns
LVC MOS12, Fast, 2 mA	0.93	0.93	3.39	3.39	3.39	3.39	ns
LVC MOS12, Fast, 4 mA	0.93	0.93	2.51	2.51	2.51	2.51	ns
LVC MOS12, Fast, 6 mA	0.93	0.93	2.11	2.11	2.11	2.11	ns
LVC MOS12, Fast, 8 mA	0.93	0.93	2.02	2.02	2.02	2.02	ns
LVDCI_25	0.66	0.66	2.26	2.26	2.26	2.26	ns
LVDCI_18	0.71	0.71	2.47	2.47	2.47	2.47	ns
LVDCI_15	0.85	0.85	2.24	2.24	2.24	2.24	ns
LVDCI_DV2_25	0.66	0.66	2.01	2.01	2.01	2.01	ns
LVDCI_DV2_18	0.71	0.71	2.00	2.00	2.00	2.00	ns
LVDCI_DV2_15	0.85	0.85	1.91	1.91	1.91	1.91	ns

Output Delay Measurements

Output delays are measured using a Tektronix P6245 TDS500/600 probe (< 1 pF) across approximately 4" of FR4 microstrip trace. Standard termination was used for all testing. The propagation delay of the 4" trace is characterized separately and subtracted from the final measurement, and is therefore not included in the generalized test setups shown in Figure 14 and Figure 15.

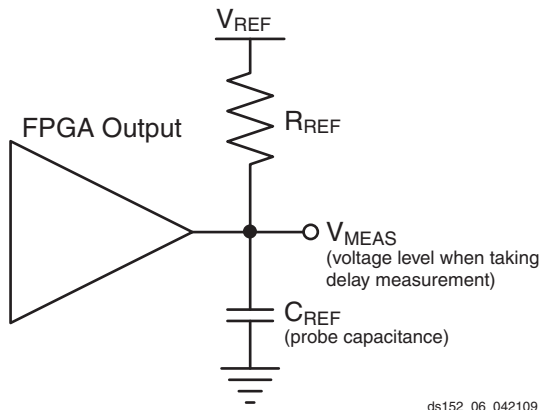
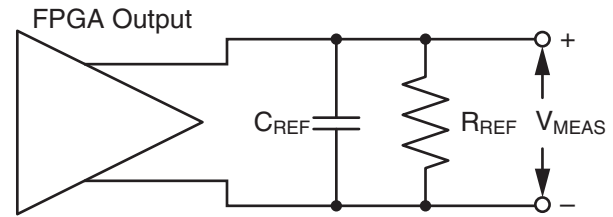


Figure 14: Single Ended Test Setup



ds152_07_042109

Figure 15: Differential Test Setup

Measurements and test conditions are reflected in the IBIS models except where the IBIS format precludes it. Parameters V_{REF} , R_{REF} , C_{REF} , and V_{MEAS} fully describe the test conditions for each I/O standard. The most accurate prediction of propagation delay in any given application can be obtained through IBIS simulation, using the following method:

1. Simulate the output driver of choice into the generalized test setup, using values from Table 41.
2. Record the time to V_{MEAS} .
3. Simulate the output driver of choice into the actual PCB trace and load, using the appropriate IBIS model or capacitance value to represent the load.
4. Record the time to V_{MEAS} .
5. Compare the results of steps 2 and 4. The increase or decrease in delay yields the actual propagation delay of the PCB trace.

Table 41: Output Delay Measurement Methodology

Description	I/O Standard Attribute	R_{REF} (Ω)	$C_{REF}^{(1)}$ (pF)	V_{MEAS} (V)	V_{REF} (V)
LVC MOS, 2.5V	LVC MOS25	1M	0	1.25	0
LVC MOS, 1.8V	LVC MOS18	1M	0	0.9	0
LVC MOS, 1.5V	LVC MOS15	1M	0	0.75	0
LVC MOS, 1.2V	LVC MOS12	1M	0	0.75	0
HSTL (High-Speed Transceiver Logic), Class I	HSTL_I	50	0	V_{REF}	0.75
HSTL, Class II	HSTL_II	25	0	V_{REF}	0.75
HSTL, Class III	HSTL_III	50	0	0.9	1.5
HSTL, Class I, 1.8V	HSTL_I_18	50	0	V_{REF}	0.9
HSTL, Class II, 1.8V	HSTL_II_18	25	0	V_{REF}	0.9
HSTL, Class III, 1.8V	HSTL_III_18	50	0	1.1	1.8
SSTL (Stub Series Terminated Logic), Class I, 1.8V	SSTL18_I	50	0	V_{REF}	0.9
SSTL, Class II, 1.8V	SSTL18_II	25	0	V_{REF}	0.9
SSTL, Class I, 2.5V	SSTL2_I	50	0	V_{REF}	1.25
SSTL, Class II, 2.5V	SSTL2_II	25	0	V_{REF}	1.25
LVDS (Low-Voltage Differential Signaling), 2.5V	LVDS_25	100	0	0 ⁽²⁾	1.2
LVDS EXT (LVDS Extended Mode), 2.5V	LVDS_25	100	0	0 ⁽²⁾	1.2
BLVDS (Bus LVDS), 2.5V	BLVDS_25	100	0	0 ⁽²⁾	0

DSP48E1 Switching Characteristics

Table 51: DSP48E1 Switching Characteristics

Symbol	Description	Speed Grade		Units
		-2	-1	
Setup and Hold Times of Data/Control Pins to the Input Register Clock				
$T_{DSPDCK_A, ACIN; B, BCIN_AREG; BREG}/T_{DSPCKD_A, ACIN; B, BCIN_AREG; BREG}$	{A, ACIN, B, BCIN} input to {A, B} register CLK	0.35/0.34	0.41/0.39	ns
$T_{DSPDCK_C_CREG}/T_{DSPCKD_C_CREG}$	C input to C register CLK	0.22/0.24	0.26/0.27	ns
$T_{DSPDCK_D_DREG}/T_{DSPCKD_D_DREG}$	D input to D register CLK	0.15/0.39	0.17/0.44	ns
Setup and Hold Times of Data Pins to the Pipeline Register Clock				
$T_{DSPDCK_A, ACIN, B, BCIN_PREG_MULT}/T_{DSPCKD_A, ACIN, B, BCIN_PREG_MULT}$	{A, ACIN, B, BCIN} input to M register CLK	3.21/0.02	3.69/0.02	ns
$T_{DSPDCK_A, D_ADREG}/T_{DSPCKD_A, D_ADREG}$	{A, D} input to AD register CLK	1.69/0.13	1.94/0.15	ns
Setup and Hold Times of Data/Control Pins to the Output Register Clock				
$T_{DSPDCK_A, ACIN, B, BCIN_PREG_MULT}/T_{DSPCKD_A, ACIN, B, BCIN_PREG_MULT}$	{A, ACIN, B, BCIN} input to P register CLK using multiplier	5.20/−0.19	5.97/−0.22	ns
$T_{DSPDCK_D_DREG_MULT}/T_{DSPCKD_D_DREG_MULT}$	D input to P register CLK	4.90/−0.65	5.63/−0.75	ns
$T_{DSPDCK_A, ACIN, B, BCIN_PREG}/T_{DSPCKD_A, ACIN, B, BCIN_PREG}$	{A, ACIN, B, BCIN} input to P register CLK not using multiplier	2.15/−0.19	2.47/−0.22	ns
$T_{DSPDCK_C_PREG}/T_{DSPCKD_C_PREG}$	C input to P register CLK	1.91/−0.14	2.19/−0.17	ns
$T_{DSPDCK_PCIN, CARRYCASCIN, MULTSIGNIN_PREG}/T_{DSPCKD_PCIN, CARRYCASCIN, MULTSIGNIN_PREG}$	{PCIN, CARRYCASCIN, MULTSIGNIN} input to P register CLK	1.67/−0.04	1.92/−0.05	ns
Setup and Hold Times of the CE Pins				
$T_{DSPDCK_CEA; CEB_AREG; BREG}/T_{DSPCKD_CEA; CEB_AREG; BREG}$	{CEA; CEB} input to {A; B} register CLK	0.22/0.25	0.25/0.29	ns
$T_{DSPDCK_CEC_CREG}/T_{DSPCKD_CEC_CREG}$	CEC input to C register CLK	0.24/0.23	0.28/0.27	ns
$T_{DSPDCK_CED_DREG}/T_{DSPCKD_CED_DREG}$	CED input to D register CLK	0.31/0.14	0.35/0.16	ns
$T_{DSPDCK_CEM_MREG}/T_{DSPCKD_CEM_MREG}$	CEM input to M register CLK	0.26/0.25	0.30/0.28	ns
$T_{DSPDCK_CEP_PREG}/T_{DSPCKD_CEP_PREG}$	CEP input to P register CLK	0.46/0.03	0.53/0.03	ns
Setup and Hold Times of the RST Pins				
$T_{DSPDCK_RSTA; RSTB_AREG; BREG}/T_{DSPCKD_RSTA; RSTB_AREG; BREG}$	{RSTA, RSTB} input to {A, B} register CLK	0.38/0.22	0.43/0.25	ns
$T_{DSPDCK_RSTC_CREG}/T_{DSPCKD_RSTC_CREG}$	RSTC input to C register CLK	0.23/0.09	0.27/0.11	ns
$T_{DSPDCK_RSTD_DREG}/T_{DSPCKD_RSTD_DREG}$	RSTD input to D register CLK	0.38/0.19	0.44/0.21	ns
$T_{DSPDCK_RSTM_MREG}/T_{DSPCKD_RSTM_MREG}$	RSTM input to M register CLK	0.26/0.30	0.30/0.35	ns
$T_{DSPDCK_RSTP_PREG}/T_{DSPCKD_RSTP_PREG}$	RSTP input to P register CLK	0.33/0.05	0.41/0.06	ns
Combinatorial Delays from Input Pins to Output Pins				
$T_{DSPDO_A, B_P, CARRYOUT_MULT}$	{A, B} input to {P, CARRYOUT} output using multiplier	5.08	5.84	ns
$T_{DSPDO_D_P, CARRYOUT_MULT}$	D input to {P, CARRYOUT} output using multiplier	4.82	5.54	ns
$T_{DSPDO_A, B_P, CARRYOUT}$	{A, B} input to {P, CARRYOUT} output not using multiplier	2.07	2.38	ns
$T_{DSPDO_C, CARRYIN_P, CARRYOUT}$	{C, CARRYIN} input to {P, CARRYOUT} output	1.83	2.10	ns

Clock Switching Characteristics

The parameters in this section provide the necessary values for calculating timing budgets for Virtex-6 CXT FPGA clock transmitter and receiver data-valid windows.

Table 64: Duty Cycle Distortion and Clock-Tree Skew

Symbol	Description	Device	Speed Grade		Units
			-2	-1	
T_{DCD_CLK}	Global Clock Tree Duty Cycle Distortion ⁽¹⁾	All	0.12	0.12	ns
T_{CKSKEW}	Global Clock Tree Skew ⁽²⁾	XC6VCX75T	0.18	0.18	ns
		XC6VCX130T	0.29	0.29	ns
		XC6VCX195T	0.31	0.31	ns
		XC6VCX240T	0.31	0.31	ns
T_{DCD_BUFIO}	I/O clock tree duty cycle distortion	All	0.08	0.08	ns
T_{BUFIO_SKEW}	I/O clock tree skew across one clock region	All	0.03	0.03	ns
T_{BUFIO_SKEW2}	I/O clock tree skew across three clock regions	All	0.22	0.22	ns
T_{DCD_BUFR}	Regional clock tree duty cycle distortion	All	0.15	0.15	ns

Notes:

- These parameters represent the worst-case duty cycle distortion observable at the pins of the device using LVDS output buffers. For cases where other I/O standards are used, IBIS can be used to calculate any additional duty cycle distortion that might be caused by asymmetrical rise/fall times.
- The T_{CKSKEW} value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx FPGA_Editor and Timing Analyzer tools to evaluate clock skew specific to your application.

Table 65: Package Skew

Symbol	Description	Device	Package	Value	Units
$T_{PKGSKEW}$	Package Skew ⁽¹⁾	XC6VCX75T	FF484		ps
			FF784		ps
		XC6VCX130T	FF484	95	ps
			FF784	146	ps
			FF1156	165	ps
		XC6VCX195T	FF784		ps
			FF1156		ps
		XC6VCX240T	FF784	146	ps
			FF1156	182	ps

Notes:

- These values represent the worst-case skew between any two SelectIO resources in the package: shortest flight time to longest flight time from Pad to Ball (7.0 ps per mm).
- Package trace length information is available for these device/package combinations. This information can be used to deskew the package.

Table 66: Sample Window

Symbol	Description	Device	Speed Grade		Units
			-2	-1	
T_{SAMP}	Sampling Error at Receiver Pins ⁽¹⁾	All	610	610	ps
$T_{\text{SAMP_BUFIO}}$	Sampling Error at Receiver Pins using BUFIO ⁽²⁾	All	400	400	ps

Notes:

1. This parameter indicates the total sampling error of Virtex-6 CXT FPGA DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the MMCM to capture the DDR input registers' edges of operation. These measurements include:
 - CLK0 MMCM jitter
 - MMCM accuracy (phase offset)
 - MMCM phase shift resolution
 These measurements do not include package or clock tree skew.
2. This parameter indicates the total sampling error of Virtex-6 CXT FPGA DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the BUFIO clock network and IODELAY to capture the DDR input registers' edges of operation. These measurements do not include package or clock tree skew.

Table 67: Pin-to-Pin Setup/Hold and Clock-to-Out

Symbol	Description	Speed Grade		Units
		-2	-1	
Data Input Setup and Hold Times Relative to a Forwarded Clock Input Pin Using BUFIO				
T _{PSCS} /T _{PHCS}	Setup/Hold of I/O clock	−0.33/1.31	−0.33/1.31	ns
Pin-to-Pin Clock-to-Out Using BUFIO				
T _{ICKOFCS}	Clock-to-Out of I/O clock	5.19	5.19	ns

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
07/08/09	1.0	Initial Xilinx release.
02/05/10	1.1	Removed Figure 11: Placement Diagram for the FF1156 Package (5 of 5) from page 11 as there are only 16 GTX transceivers in the FF1156 package. Corrected the placement diagrams in Figure 2 through Figure 10 .

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