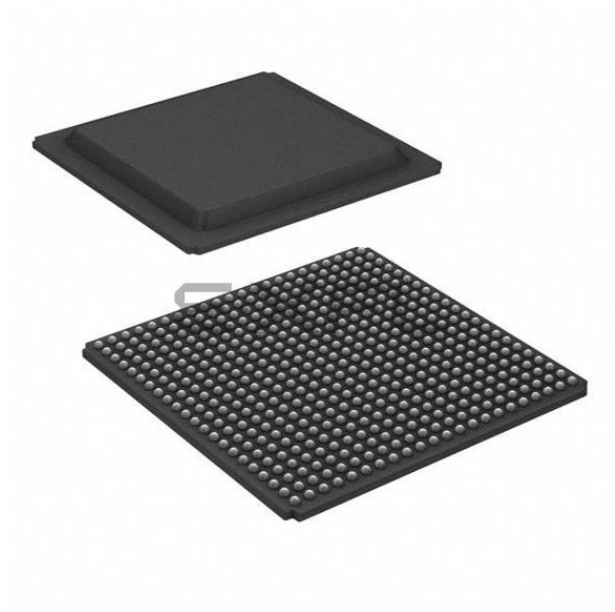
AMD Xilinx - XC6VCX130T-1FFG484I Datasheet



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The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	10000
Number of Logic Elements/Cells	128000
Total RAM Bits	9732096
Number of I/O	240
Number of Gates	-
Voltage - Supply	0.95V ~ 1.05V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	484-BBGA
Supplier Device Package	484-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc6vcx130t-1ffg484i

Virtex-6 CXT FPGA Feature Summary

Table 1: **Virtex-6 CXT FPGA Feature Summary by Device**

Device	Logic Cells	Configurable Logic Blocks (CLBs)		DSP48E1 Slices(2)	Block RAM Blocks			MMCMs(4)	Interface Blocks for PCI Express	Ethernet MACs(5)	Maximum GTX Transceivers	Total I/O Banks(6)	Max User I/O(7)
		Slices(1)	Max Distributed RAM (Kb)		18 Kb(3)	36 Kb	Max (Kb)						
XC6VCX75T	74,496	11,640	1,045	288	312	156	5,616	6	1	1	12	9	360
XC6VCX130T	128,000	20,000	1,740	480	528	264	9,504	10	2	1	16	15	600
XC6VCX195T	199,680	31,200	3,040	640	688	344	12,384	10	2	1	16	15	600
XC6VCX240T	241,152	37,680	3,650	768	832	416	14,976	12	2	1	16	18	600

Notes:

1. Each Virtex-6 CXT FPGA slice contains four LUTs and eight flip-flops, only some slices can use their LUTs as distributed RAM or SRLs.
2. Each DSP48E1 slice contains a 25 x 18 multiplier, an adder, and an accumulator.
3. Block RAMs are fundamentally 36 Kbits in size. Each block can also be used as two independent 18 Kb blocks.
4. Each CMT contains two mixed-mode clock managers (MMCM).
5. This table lists individual Ethernet MACs per device.
6. Does not include configuration Bank 0.
7. This number does not include GTX transceivers.

Virtex-6 CXT FPGA Device-Package Combinations and Maximum I/Os

Virtex-6 CXT FPGA package combinations with the maximum available I/Os per package are shown in Table 2.

Table 2: **Virtex-6 CXT FPGA Device-Package Combinations and Maximum Available I/Os**

Package	FF484 FFG484		FF784 FFG784		FF1156 FFG1156	
Size (mm)	23 x 23		29 x 29		35 x 35	
Device	GTs	I/O	GTs	I/O	GTs	I/O
XC6VCX75T	8 GTXs	240	12 GTXs	360		
XC6VCX130T	8 GTXs	240	12 GTXs	400	16 GTXs	600
XC6VCX195T			12 GTXs	400	16 GTXs	600
XC6VCX240T			12 GTXs	400	16 GTXs	600

Notes:

1. Flip-chip packages are also available in Pb-Free versions (FFG).

Virtex-6 CXT FPGA Ordering Information

The Virtex-6 CXT FPGA ordering information shown in Figure 1 applies to all packages including Pb-Free.

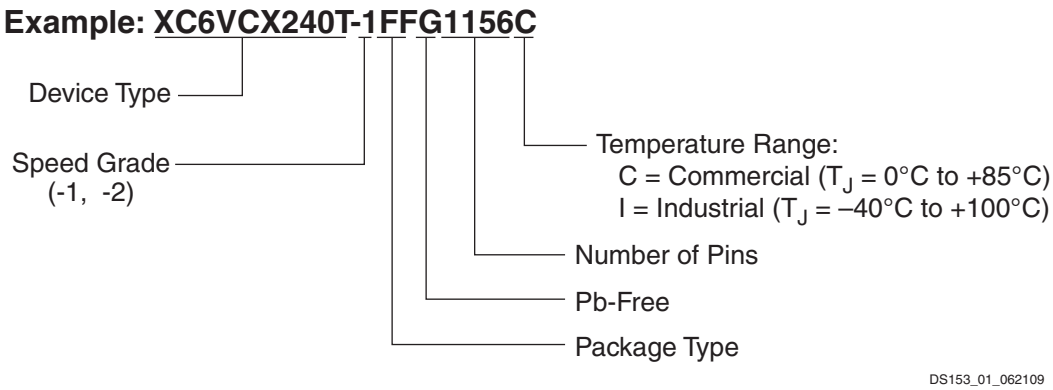

Figure 1: **Virtex-6 CXT FPGA Ordering Information**

FF484 Package Placement Diagrams

Figure 2 and Figure 3 show the placement diagrams for the GTX transceivers in the FF484 package.

Note: Unbonded locations in the FF484 package are:

- CX75T: X0Y8, X0Y9, X0Y10, X0Y11
- CX130T: X0Y0, X0Y1, X0Y2, X0Y3, and X0Y12, X0Y13, X0Y14, X0Y15

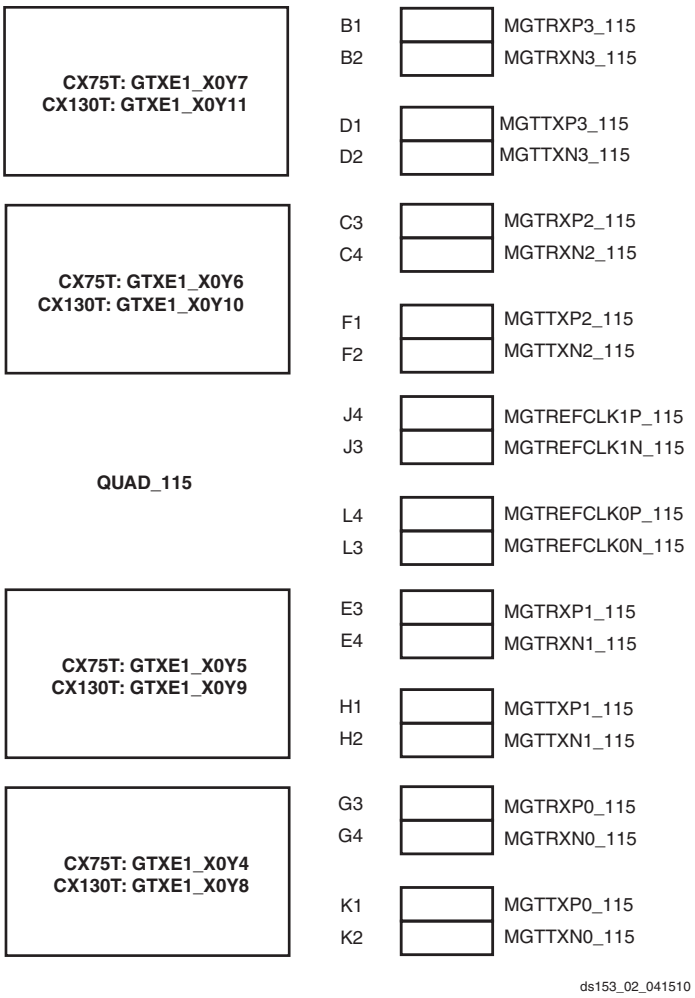

Figure 2: **Placement Diagram for the FF484 Package (1 of 2)**

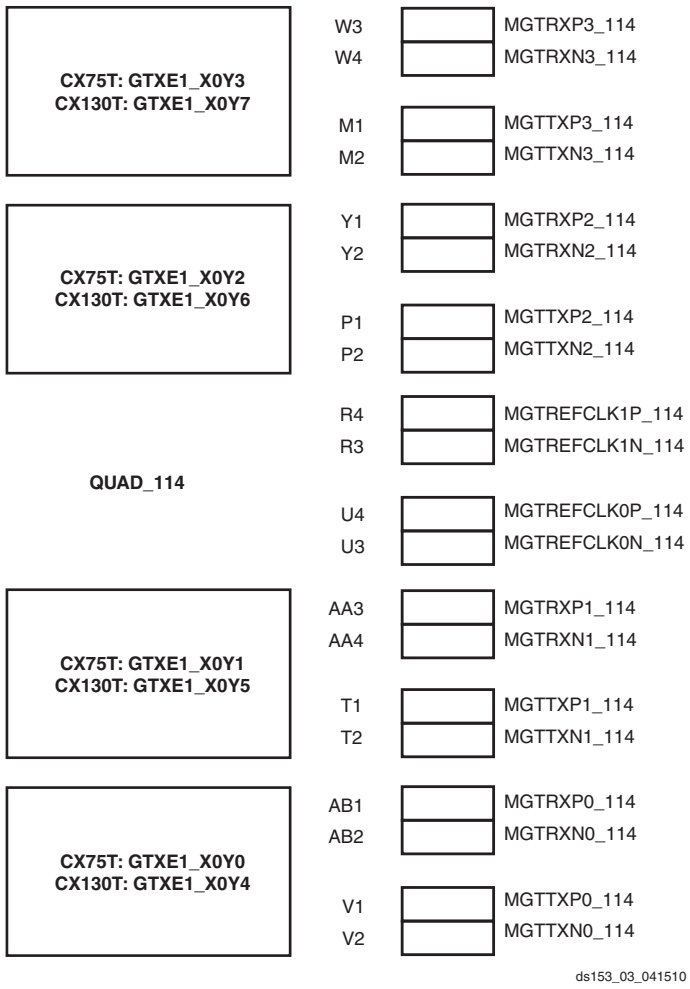

Figure 3: **Placement Diagram for the FF484 Package (2 of 2)**

HT DC Specifications (HT_25)

Table 16: **HT DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply Voltage		2.38	2.5	2.63	V
V_{OD}	Differential Output Voltage	R_T = 100 Ω across Q and $\overline{Q}$ signals	480	600	885	mV
ΔV_{OD}	Change in V_{OD} Magnitude		–15	–	15	mV
V_{OCM}	Output Common Mode Voltage	R_T = 100 Ω across Q and $\overline{Q}$ signals	480	600	885	mV
ΔV_{OCM}	Change in V_{OCM} Magnitude		–15	–	15	mV
V_{ID}	Input Differential Voltage		200	600	1000	mV
ΔV_{ID}	Change in V_{ID} Magnitude		–15	–	15	mV
V_{ICM}	Input Common Mode Voltage		440	600	780	mV
ΔV_{ICM}	Change in V_{ICM} Magnitude		–15	–	15	mV

LVDS DC Specifications (LVDS_25)

Table 17: **LVDS DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply Voltage		2.38	2.5	2.63	V
V_{OH}	Output High Voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals	–	–	1.675	V
V_{OL}	Output Low Voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals	0.825	–	–	V
V_{ODIFF}	Differential Output Voltage (Q – $\overline{Q}$), Q = High (($\overline{Q}$ – Q), $\overline{Q}$ = High	R_T = 100 Ω across Q and $\overline{Q}$ signals	247	350	600	mV
V_{OCM}	Output Common-Mode Voltage	R_T = 100 Ω across Q and $\overline{Q}$ signals	1.075	1.250	1.425	V
V_{IDIFF}	Differential Input Voltage (Q – $\overline{Q}$), Q = High (($\overline{Q}$ – Q), $\overline{Q}$ = High		100	350	600	mV
V_{ICM}	Input Common-Mode Voltage		0.3	1.2	2.2	V

Extended LVDS DC Specifications (LVDSEXT_25)

Table 18: **Extended LVDS DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply Voltage		2.38	2.5	2.63	V
V_{OH}	Output High Voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals	–	–	1.785	V
V_{OL}	Output Low Voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals	0.715	–	–	V
V_{ODIFF}	Differential Output Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	R_T = 100 Ω across Q and $\overline{Q}$ signals	350	–	840	mV
V_{OCM}	Output Common-Mode Voltage	R_T = 100 Ω across Q and $\overline{Q}$ signals	1.075	1.250	1.425	V
V_{IDIFF}	Differential Input Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	Common-mode input voltage = 1.25V	100	–	1000	mV
V_{ICM}	Input Common-Mode Voltage	Differential input voltage = ±350 mV	0.3	1.2	2.2	V

LVPECL DC Specifications (LVPECL_25)

These values are valid when driving a 100Ω differential load only, i.e., a 100Ω resistor between the two receiver pins. The V_{OH} levels are 200 mV below standard LVPECL levels and are compatible with devices tolerant of lower common-mode ranges. Table 19 summarizes the DC output specifications of LVPECL. For more information on using LVPECL, see the *Virtex-6 FPGA SelectIO Resources User Guide*.

Table 19: **LVPECL DC Specifications**

Symbol	DC Parameter	Min	Typ	Max	Units
V_{OH}	Output High Voltage	V_{CC} – 1.025	1.545	V_{CC} – 0.88	V
V_{OL}	Output Low Voltage	V_{CC} – 1.81	0.795	V_{CC} – 1.62	V
V_{ICM}	Input Common-Mode Voltage	0.6	–	2.2	V
V_{IDIFF}	Differential Input Voltage(1)(2)	0.100	–	1.5	V

Notes:

1. Recommended input maximum voltage not to exceed V_{CCAUX} + 0.2V.
2. Recommended input minimum voltage not to go below –0.5V.

eFUSE Read Endurance

Table 20 lists the maximum number of read cycle operations expected. For more information, see the *Virtex-6 FPGA Configuration User Guide*.

Table 20: **eFUSE Read Endurance**

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
DNA_CYCLES	Number of DNA_PORT READ operations or JTAG ISC_DNA read command operations. Unaffected by SHIFT operations.	30,000,000				Read Cycles
AES_CYCLES	Number of JTAG FUSE_KEY or FUSE_CNTL read command operations. Unaffected by SHIFT operations.	30,000,000				Read Cycles

GTX Transceiver Specifications

GTX Transceiver DC Characteristics

Table 21: **Absolute Maximum Ratings for GTX Transceivers(1)**

Symbol	Description	Min	Max	Units
MGTAVCC	Analog supply voltage for the GTX transmitter and receiver circuits relative to GND	–0.5	1.1	V
MGTAVTT	Analog supply voltage for the GTX transmitter and receiver termination circuits relative to GND	–0.5	1.32	V
MGTAVTTRCAL	Analog supply voltage for the resistor calibration circuit of the GTX transceiver column	–0.5	1.32	V
V_{IN}	Receiver (RXP/RXN) and Transmitter (TXP/TXN) absolute input voltage	–0.5	1.32	V
$V_{MGTREFCLK}$	Reference clock absolute input voltage	–0.5	1.32	V

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.

Table 22: **Recommended Operating Conditions for GTX Transceivers(1)(2)**

Symbol	Description	Min	Typ	Max	Units
MGTAVCC	Analog supply voltage for the GTX transmitter and receiver circuits relative to GND	0.95	1.0	1.06	V
MGTAVTT	Analog supply voltage for the GTX transmitter and receiver termination circuits relative to GND	1.14	1.2	1.26	V
MGTAVTTRCAL	Analog supply voltage for the resistor calibration circuit of the GTX transceiver column	1.14	1.2	1.26	V

Notes:

1. Each voltage listed requires the filter circuit described in *Virtex-6 FPGA GTX Transceivers User Guide*.
2. Voltages are specified for the temperature range of T_j = –40°C to +100°C.

Table 23: **GTX Transceiver Supply Current (per Lane) (1)(2)**

Symbol	Description	Typ	Max	Units
$I_{MGTAVTT}$	MGTAVTT supply current for one GTX transceiver	55.9	Note 2	mA
$I_{MGTAVCC}$	MGTAVCC supply current for one GTX transceiver	56.1		mA
$MGTR_{REF}$	Precision reference resistor for internal calibration termination	100.0 ± 1% tolerance		Ω

Notes:

1. Typical values are specified at nominal voltage, 25°C, with a 3.125 Gb/s line rate.
2. Values for currents other than the values specified in this table can be obtained by using the XPOWER Estimator (XPE) or XPOWER Analyzer (XPA) tools.

Table 24: **GTX Transceiver Quiescent Supply Current (per Lane)(1)(2)(3)**

Symbol	Description	Typ(4)	Max	Units
$I_{MGTAVTTQ}$	Quiescent MGTAVTT supply current for one GTX transceiver	0.9	Note 2	mA
$I_{MGTAVCCQ}$	Quiescent MGTAVCC supply current for one GTX transceiver	3.5		mA

Notes:

1. Device powered and unconfigured.
2. Currents for conditions other than values specified in this table can be obtained by using the XPOWER Estimator (XPE) or XPOWER Analyzer (XPA) tools.
3. GTX transceiver quiescent supply current for an entire device can be calculated by multiplying the values in this table by the number of available GTX transceivers.
4. Typical values are specified at nominal voltage, 25°C.

Table 26 summarizes the DC specifications of the clock input of the GTX transceiver. Consult the *Virtex-6 FPGA GTX Transceivers User Guide* for further details.

Table 26: **GTX Transceiver Clock DC Input Level Specification**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{IDIFF}	Differential peak-to-peak input voltage		210	800	2000	mV
R_{IN}	Differential input resistance		90	100	130	Ω
C_{EXT}	Required external AC coupling capacitor		–	100	–	nF

GTX Transceiver Switching Characteristics

Consult *Virtex-6 FPGA GTX Transceivers User Guide* for further information.

Table 27: **GTX Transceiver Performance**

Symbol	Description	Speed Grade		Units
		-2	-1	
F_{GTXMAX}	Maximum GTX transceiver data rate	3.75	3.75	Gb/s
$F_{GPLLMAX}$	Maximum PLL frequency	2.5	2.5	GHz
$F_{GPLLMIN}$	Minimum PLL frequency	1.2	1.2	GHz

Table 28: **GTX Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics**

Symbol	Description	Speed Grade		Units
		-2	-1	
$F_{GTXDRPCLK}$	GTXDRPCLK maximum frequency	100	100	MHz

Table 29: **GTX Transceiver Reference Clock Switching Characteristics**

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
F_{GCLK}	Reference clock frequency range		67.5	–	375	MHz
T_{RCLK}	Reference clock rise time	20% – 80%	–	200	–	ps
T_{FCLK}	Reference clock fall time	80% – 20%	–	200	–	ps
T_{DCREF}	Reference clock duty cycle	Transceiver PLL only	45	50	55	%
T_{LOCK}	Clock recovery frequency acquisition time	Initial PLL lock	–	–	1	ms
T_{PHASE}	Clock recovery phase acquisition time	Lock to data after PLL has locked to the reference clock	–	–	200	µs

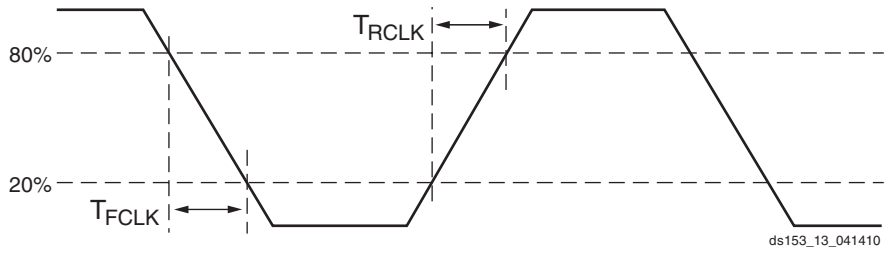

Figure 13: **Reference Clock Timing Parameters**

Table 30: **GTX Transceiver User Clock Switching Characteristics(1)**

Symbol	Description	Conditions	Speed Grade		Units
			-2	-1	
F_{TXOUT}	TXOUTCLK maximum frequency	Internal 20-bit data path	187.5	187.5	MHz
		Internal 16-bit data path	234.38	234.38	MHz
F_{RXREC}	RXRECCLK maximum frequency	Internal 20-bit data path	187.5	187.5	MHz
		Internal 16-bit data path	234.38	234.38	MHz
T_{RX}	RXUSRCLK maximum frequency		234.38	234.38	MHz
T_{RX2}	RXUSRCLK2 maximum frequency	1 byte interface	376	312.5	MHz
		2 byte interface	234.38	234.38	MHz
		4 byte interface	117.19	117.19	MHz
T_{TX}	TXUSRCLK maximum frequency		234.38	234.38	MHz
T_{TX2}	TXUSRCLK2 maximum frequency	1 byte interface	376	312.5	MHz
		2 byte interface	234.38	234.38	MHz
		4 byte interface	117.19	117.19	MHz

Notes:

1. Clocking must be implemented as described in *Virtex-6 FPGA GTX Transceivers User Guide*.

Table 31: **GTX Transceiver Transmitter Switching Characteristics**

Symbol	Description	Condition	Min	Typ	Max	Units
F_{GTXTX}	Serial data rate range		0.480	–	F_{GTXMAX}	Gb/s
T_{RTX}	TX Rise time	20%–80%	–	120	–	ps
T_{FTX}	TX Fall time	80%–20%	–	120	–	ps
T_{LLSKEW}	TX lane-to-lane skew(1)		–	–	350	ps
$V_{TXOOBVDPP}$	Electrical idle amplitude		–	–	15	mV
$T_{TXOOBTRANSITION}$	Electrical idle transition time		–	–	75	ns
$T_{J3.75}$	Total Jitter(2)(3)	3.75 Gb/s	–	–	0.34	UI
$D_{J3.75}$	Deterministic Jitter(2)(3)		–	–	0.16	UI
$T_{J3.125}$	Total Jitter(2)(3)	3.125 Gb/s	–	–	0.2	UI
$D_{J3.125}$	Deterministic Jitter(2)(3)		–	–	0.1	UI
$T_{J3.125L}$	Total Jitter(2)(3)	3.125 Gb/s(4)	–	–	0.35	UI
$D_{J3.125L}$	Deterministic Jitter(2)(3)		–	–	0.16	UI
$T_{J2.5}$	Total Jitter(2)(3)	2.5 Gb/s(5)	–	–	0.20	UI
$D_{J2.5}$	Deterministic Jitter(2)(3)		–	–	0.08	UI
$T_{J1.25}$	Total Jitter(2)(3)	1.25 Gb/s(6)	–	–	0.15	UI
$D_{J1.25}$	Deterministic Jitter(2)(3)		–	–	0.06	UI
T_{J600}	Total Jitter(2)(3)	600 Mb/s	–	–	0.1	UI
D_{J600}	Deterministic Jitter(2)(3)		–	–	0.03	UI

Ethernet MAC Switching Characteristics

Consult *Virtex-6 FPGA Embedded Tri-mode Ethernet MAC User Guide* for further information.

Table 33: **Maximum Ethernet MAC Performance**

Symbol	Description	Conditions	Speed Grade		Units
			-2	-1	
$F_{TEMACCLIENT}$	Client interface maximum frequency	10 Mb/s – 8-bit width	2.5(1)	2.5(1)	MHz
		100 Mb/s – 8-bit width	25(2)	25(2)	MHz
		1000 Mb/s – 8-bit width	125	125	MHz
		1000 Mb/s – 16-bit width	62.5	62.5	MHz
$F_{TEMACPHY}$	Physical interface maximum frequency	10 Mb/s – 4-bit width	2.5	2.5	MHz
		100 Mb/s – 4-bit width	25	25	MHz
		1000 Mb/s – 8-bit width	125	125	MHz

Notes:

1. When not using clock enable, the F_{MAX} is lowered to 1.25 MHz.
2. When not using clock enable, the F_{MAX} is lowered to 12.5 MHz.

Integrated Interface Block for PCI Express Designs Switching Characteristics

More information and documentation on solutions for PCI Express designs can be found at:
http://www.xilinx.com/technology/protocols/pciexpress.htm

Table 34: **Maximum Performance for PCI Express Designs**

Symbol	Description	Speed Grade		Units
		-2	-1	
$F_{PIPECLK}$	Pipe clock maximum frequency	125	125	MHz
$F_{USERCLK}$	User clock maximum frequency	250	250	MHz
F_{DRPCLK}	DRP clock maximum frequency	250	250	MHz

Table 38: **IOB Switching Characteristics *(Cont'd)***

I/O Standard	T_{IOPI}		T_{IOOP}		T_{IOTP}		Units
	Speed Grade		Speed Grade		Speed Grade		
	-2	-1	-2	-1	-2	-1	
LVPECL_25	1.09	1.09	1.65	1.65	1.65	1.65	ns
HSTL_I_12	1.06	1.06	1.78	1.78	1.78	1.78	ns
HSTL_I_DCI	1.06	1.06	1.66	1.66	1.66	1.66	ns
HSTL_II_DCI	1.06	1.06	1.68	1.68	1.68	1.68	ns
HSTL_II_T_DCI	1.06	1.06	1.66	1.66	1.66	1.66	ns
HSTL_III_DCI	1.06	1.06	1.62	1.62	1.62	1.62	ns
HSTL_I_DCI_18	1.06	1.06	1.68	1.68	1.68	1.68	ns
HSTL_II_DCI_18	1.06	1.06	1.62	1.62	1.62	1.62	ns
HSTL_II _T_DCI_18	1.06	1.06	1.68	1.68	1.68	1.68	ns
HSTL_III_DCI_18	1.06	1.06	1.69	1.69	1.69	1.69	ns
DIFF_HSTL_I_18	1.09	1.09	1.75	1.75	1.75	1.75	ns
DIFF_HSTL_I_DCI_18	1.09	1.09	1.68	1.68	1.68	1.68	ns
DIFF_HSTL_I	1.09	1.09	1.73	1.73	1.73	1.73	ns
DIFF_HSTL_I_DCI	1.09	1.09	1.66	1.66	1.66	1.66	ns
DIFF_HSTL_II_18	1.09	1.09	1.81	1.81	1.81	1.81	ns
DIFF_HSTL_II_DCI_18	1.09	1.09	1.62	1.62	1.62	1.62	ns
DIFF_HSTL_II _T_DCI_18	1.09	1.09	1.68	1.68	1.68	1.68	ns
DIFF_HSTL_II	1.09	1.09	1.74	1.74	1.74	1.74	ns
DIFF_HSTL_II_DCI	1.09	1.09	1.68	1.68	1.68	1.68	ns
SSTL2_I_DCI	1.06	1.06	1.70	1.70	1.70	1.70	ns
SSTL2_II_DCI	1.06	1.06	1.67	1.67	1.67	1.67	ns
SSTL2_II_T_DCI	1.06	1.06	1.70	1.70	1.70	1.70	ns
SSTL18_I	1.06	1.06	1.75	1.75	1.75	1.75	ns
SSTL18_II	1.06	1.06	1.67	1.67	1.67	1.67	ns
SSTL18_I_DCI	1.06	1.06	1.67	1.67	1.67	1.67	ns
SSTL18_II_DCI	1.06	1.06	1.63	1.63	1.63	1.63	ns
SSTL18_II_T_DCI	1.06	1.06	1.67	1.67	1.67	1.67	ns
SSTL15_T_DCI	1.06	1.06	1.68	1.68	1.68	1.68	ns
SSTL15_DCI	1.06	1.06	1.68	1.68	1.68	1.68	ns
DIFF_SSTL2_I	1.09	1.09	1.77	1.77	1.77	1.77	ns
DIFF_SSTL2_I_DCI	1.09	1.09	1.70	1.70	1.70	1.70	ns
DIFF_SSTL2_II	1.09	1.09	1.72	1.72	1.72	1.72	ns
DIFF_SSTL2_II_DCI	1.09	1.09	1.67	1.67	1.67	1.67	ns
DIFF_SSTL2_II_T_DCI	1.09	1.09	1.70	1.70	1.70	1.70	ns
DIFF_SSTL18_I	1.09	1.09	1.75	1.75	1.75	1.75	ns
DIFF_SSTL18_I_DCI	1.09	1.09	1.67	1.67	1.67	1.67	ns
DIFF_SSTL18_II	1.09	1.09	1.67	1.67	1.67	1.67	ns
DIFF_SSTL18_II_DCI	1.09	1.09	1.63	1.63	1.63	1.63	ns

Table 41: **Output Delay Measurement Methodology *(Cont'd)***

Description	I/O Standard Attribute	R_{REF} (Ω)	C_{REF}[1] (pF)	V_{MEAS} (V)	V_{REF} (V)
HT (HyperTransport), 2.5V	LDT_25	100	0	0[2]	0.6
LVPECL (Low-Voltage Positive Emitter-Coupled Logic), 2.5V	LVPECL_25	100	0	0[2]	0
LVDCI/HSLVDCI, 2.5V	LVDCI_25, HSLVDCI_25	1M	0	1.25	0
LVDCI/HSLVDCI, 1.8V	LVDCI_18, HSLVDCI_18	1M	0	0.9	0
LVDCI/HSLVDCI, 1.5V	LVDCI_15, HSLVDCI_15	1M	0	0.75	0
HSTL (High-Speed Transceiver Logic), Class I & II, with DCI	HSTL_I_DCI, HSTL_II_DCI	50	0	V_{REF}	0.75
HSTL, Class III, with DCI	HSTL_III_DCI	50	0	0.9	1.5
HSTL, Class I & II, 1.8V, with DCI	HSTL_I_DCI_18, HSTL_II_DCI_18	50	0	V_{REF}	0.9
HSTL, Class III, 1.8V, with DCI	HSTL_III_DCI_18	50	0	1.1	1.8
SSTL (Stub Series Termi.Logic), Class I & II, 1.8V, with DCI	SSTL18_I_DCI, SSTL18_II_DCI	50	0	V_{REF}	0.9
SSTL, Class I & II, 2.5V, with DCI	SSTL2_I_DCI, SSTL2_II_DCI	50	0	V_{REF}	1.25

Notes:

1. C_{REF} is the capacitance of the probe, nominally 0 pF.
2. The value given is the differential output voltage.

Input/Output Logic Switching Characteristics

Table 42: **ILOGIC Switching Characteristics**

Symbol	Description	Speed Grade		Units
		-2	-1	
Setup/Hold				
T_{ICE1CK}/T_{ICKCE1}	CE1 pin Setup/Hold with respect to CLK	0.27/0.04	0.27/0.04	ns
T_{ISRCK}/T_{ICKSR}	SR pin Setup/Hold with respect to CLK	0.96/–0.10	0.96/–0.10	ns
T_{IDOCK}/T_{IOCKD}	D pin Setup/Hold with respect to CLK without Delay	0.10/0.54	0.10/0.54	ns
T_{IDOCKD}/T_{IOCKDD}	DDLY pin Setup/Hold with respect to CLK (using IODELAY)	0.14/0.42	0.14/0.40	ns
Combinatorial				
T_{IDI}	D pin to O pin propagation delay, no Delay	0.20	0.20	ns
T_{IDID}	DDLY pin to O pin propagation delay (using IODELAY)	0.25	0.25	ns
Sequential Delays				
T_{IDLO}	D pin to Q1 pin using flip-flop as a latch without Delay	0.64	0.64	ns
T_{IDLOD}	DDLY pin to Q1 pin using flip-flop as a latch (using IODELAY)	0.68	0.68	ns
T_{ICKQ}	CLK to Q outputs	0.71	0.71	ns
T_{RQ_ILOGIC}	SR pin to OQ/TQ out	1.15	1.15	ns
T_{GSRQ_ILOGIC}	Global Set/Reset to Q outputs	10.51	10.51	ns
Set/Reset				
T_{RPW_ILOGIC}	Minimum Pulse Width, SR inputs	1.20	1.20	ns, Min

Output Serializer/Deserializer Switching Characteristics

Table 45: **OSERDES Switching Characteristics**

Symbol	Description	Speed Grade		Units
		-2	-1	
Setup/Hold				
T_{OSDCK_D}/T_{OSCKD_D}	D input Setup/Hold with respect to CLKDIV	0.31/–0.12	0.31/–0.12	ns
T_{OSDCK_T}/T_{OSCKD_T}(1)	T input Setup/Hold with respect to CLK	0.56/–0.08	0.56/–0.08	ns
$T_{OSDCK\_T2}/T_{OSCKD\_T2}$(1)	T input Setup/Hold with respect to CLKDIV	0.31/–0.08	0.31/–0.08	ns
$T_{OSCCK\_OCE}/T_{OSCKC\_OCE}$	OCE input Setup/Hold with respect to CLK	0.22/–0.05	0.22/–0.05	ns
T_{OSCCK_S}	SR (Reset) input Setup with respect to CLKDIV	0.07	0.07	ns
$T_{OSCCK\_TCE}/T_{OSCKC\_TCE}$	TCE input Setup/Hold with respect to CLK	0.21/–0.05	0.21/–0.05	ns
Sequential Delays				
T_{OSCKO_OQ}	Clock to out from CLK to OQ	0.82	0.82	ns
T_{OSCKO_TQ}	Clock to out from CLK to TQ	0.82	0.82	ns
Combinatorial				
T_{OSDO_TTQ}	T input to TQ Out	0.97	0.97	ns

Notes:

1. T_{OSDCK_T2} and T_{OSCKD_T2} are reported as T_{OSDCK_T}/T_{OSCKD_T} in the TRACE report.

Input/Output Delay Switching Characteristics

Table 46: **Input/Output Delay Switching Characteristics**

Symbol	Description	Speed Grade		Units
		-2	-1	
IDELAYCTRL				
T_{DLYCCO_RDY}	Reset to Ready for IDELAYCTRL	3	3	µs
$F_{IDELAYCTRL\_REF}$	REFCLK frequency	200	200	MHz
IDELAYCTRL_REF_PRECISION	REFCLK precision	±10	±10	MHz
$T_{IDELAYCTRL\_RPW}$	Minimum Reset pulse width	50	50	ns
IODELAY				
$T_{IDELAYRESOLUTION}$	IODELAY Chain Delay Resolution	1/(32 x 2 x F_{REF})		ps
$T_{IDELAYPAT\_JIT}$	Pattern dependent period jitter in delay chain for clock pattern.(1)	0	0	ps per tap
	Pattern dependent period jitter in delay chain for random data pattern.(2)	±5	±5	ps per tap
	Pattern dependent period jitter in delay chain for random data pattern.(3)	±9	±9	ps per tap
$T_{IODELAY\_CLK\_MAX}$	Maximum frequency of CLK input to IODELAY	300	300	MHz
T_{IODCCK_CE} / T_{IODCKC_CE}	CE pin Setup/Hold with respect to CK	0.65/–0.09	0.65/–0.09	ns
T_{IODCK_INC}/ T_{IODCKC_INC}	INC pin Setup/Hold with respect to CK	0.31/–0.00	0.31/–0.00	ns
T_{IODCCK_RST}/ T_{IODCKC_RST}	RST pin Setup/Hold with respect to CK	0.69/–0.08	0.69/–0.08	ns
T_{IODDO_T}	TSCONTROL delay to MUXE/MUXF switching and through IODELAY	Note 4	Note 4	ps
$T_{IODDO\_IDATAIN}$	Propagation delay through IODELAY	Note 4	Note 4	ps
$T_{IODDO\_ODATAIN}$	Propagation delay through IODELAY	Note 4	Note 4	ps

Notes:

1. When HIGH_PERFORMANCE mode is set to TRUE or FALSE.
2. When HIGH_PERFORMANCE mode is set to TRUE
3. When HIGH_PERFORMANCE mode is set to FALSE.
4. Delay depends on IODELAY tap setting. See the TRACE report for actual values.

CLB Switching Characteristics

Table 47: **CLB Switching Characteristics**

Symbol	Description	Speed Grade		Units
		-2	-1	
Combinatorial Delays				
T_{ILO}	An – Dn LUT address to A	0.08	0.08	ns, Max
	An – Dn LUT address to AMUX/CMUX	0.23	0.25	ns, Max
	An – Dn LUT address to BMUX_A	0.37	0.41	ns, Max
T_{ITO}	An – Dn inputs to A – D Q outputs	0.79	0.91	ns, Max
T_{AXA}	AX inputs to AMUX output	0.42	0.48	ns, Max
T_{AXB}	AX inputs to BMUX output	0.47	0.53	ns, Max
T_{AXC}	AX inputs to CMUX output	0.52	0.60	ns, Max
T_{AXD}	AX inputs to DMUX output	0.55	0.63	ns, Max

Table 51: **DSP48E1 Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade		Units
		-2	-1	
Clock to Outs from Input Register Clock to Cascading Output Pins				
$T_{DSPCKO\_\{ACOUT;\ BCOUT\}\_\{AREG;\ BREG\}}$	CLK (AREG, BREG) to {P, CARRYOUT} output	0.89	1.02	ns
$T_{DSPCKO\_\{PCOUT,\ CARRYCASCOUT,\ MULTSIGNOUT\}\_\{AREG,\ BREG\}\_MULT}$	CLK (AREG, BREG) to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output using multiplier	5.49	6.31	ns
$T_{DSPCKO\_\{PCOUT,\ CARRYCASCOUT,\ MULTSIGNOUT\}\_\{AREG,\ BREG\}}$	CLK (AREG, BREG) to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output not using multiplier	2.40	2.76	ns
$T_{DSPCKO\_\{PCOUT,\ CARRYCASCOUT,\ MULTSIGNOUT\}\_DREG\_MULT}$	CLK (DREG) to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output using multiplier	5.38	6.18	ns
$T_{DSPCKO\_\{PCOUT,\ CARRYCASCOUT,\ MULTSIGNOUT\}\_CREG}$	CLK (CREG) to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output	2.40	2.76	ns
Maximum Frequency				
F_{MAX}	With all registers used	350	275	MHz
F_{MAX_PATDET}	With pattern detector	350	275	MHz
$F_{MAX\_MULT\_NOMREG}$	Two register multiply without MREG	262	227	MHz
$F_{MAX\_MULT\_NOMREG\_PATDET}$	Two register multiply without MREG with pattern detect	241	209	MHz
$F_{MAX\_PREADD\_MULT\_NOADREG}$	Without ADREG	292	253	MHz
$F_{MAX\_PREADD\_MULT\_NOADREG\_PATDET}$	Without ADREG with pattern detect	292	253	MHz
$F_{MAX\_NOPIPELINEREG}$	Without pipeline registers (MREG, ADREG)	196	170	MHz
$F_{MAX\_NOPIPELINEREG\_PATDET}$	Without pipeline registers (MREG, ADREG) with pattern detect	184	160	MHz

Configuration Switching Characteristics

Table 52: **Configuration Switching Characteristics**

Symbol	Description	Speed Grade		Units
		-2	-1	
Power-up Timing Characteristics				
T_{PL} (1)	Program Latency	3	3	ms, Max
T_{POR} (1)	Power-on-Reset	15/55	15/55	ms, Min/Max
T_{ICCK}	CCLK (output) delay	400	400	ns, Min
$T_{PROGRAM}$	Program Pulse Width	250	250	ns, Min
Master/Slave Serial Mode Programming Switching (1)				
T_{DCCK}/T_{CCKD}	DIN Setup/Hold, slave mode	4.0/0.0	4.0/0.0	ns, Min
T_{DSCCK}/T_{SCCKD}	DIN Setup/Hold, master mode	4.0/0.0	4.0/0.0	ns, Min
T_{CCO}	DOUT at 2.5V	6	6	ns, Max
	DOUT at 1.8V	6	6	ns, Max
F_{MCCK}	Maximum CCLK frequency, serial modes	100	100	MHz, Max
$F_{MCCKTOL}$	Frequency Tolerance, master mode with respect to nominal CCLK	55	55	%
F_{MSCCK}	Slave mode external CCLK	100	100	MHz
SelectMAP Mode Programming Switching				
T_{SMDCCK}/T_{SMCCKD}	SelectMAP Data Setup/Hold	4.0/0.0	4.0/0.0	ns, Min
$T_{SMCSCCK}/T_{SMCCKCS}$	CSI_B Setup/Hold	4.0/0.0	4.0/0.0	ns, Min
T_{SMCCKW}/T_{SMWCCK}	RDWR_B Setup/Hold	10.0/0.0	10.0/0.0	ns, Min
$T_{SMCKCSO}$	CSO_B clock to out (330 Ω pull-up resistor required)	7	7	ns, Min
T_{SMCO}	CCLK to DATA out in readback at 2.5V	8	8	ns, Max
	CCLK to DATA out in readback at 1.8V	8	8	ns, Max
T_{SMCKBY}	CCLK to BUSY out in readback at 2.5V	6	6	ns, Max
	CCLK to BUSY out in readback at 1.8V	6	6	ns, Max
F_{SMCCK}	Maximum Frequency with respect to nominal CCLK	100	100	MHz, Max
F_{RBCCK}	Maximum Readback Frequency with respect to nominal CCLK	100	100	MHz, Max
$F_{MCCKTOL}$	Frequency Tolerance with respect to nominal CCLK	55	55	%
Boundary-Scan Port Timing Specifications				
T_{TAPTCK}/T_{TCKTAP}	TMS and TDI Setup time before TCK/ Hold time after TCK	3.0/2.0	3.0/2.0	ns, Min
T_{TCKTDO}	TCK falling edge to TDO output valid at 2.5V	6	6	ns, Max
	TCK falling edge to TDO output valid at 1.8V	6	6	ns, Max
F_{TCK}	Maximum configuration TCK clock frequency	66	66	MHz, Max
F_{TCKB_MIN}	Minimum boundary-scan TCK clock frequency when using IEEE Std 1149.6 (AC-JTAG). Minimum operating temperature for IEEE Std 1149.6 is 0°C.	15	15	MHz, Min
F_{TCKB}	Maximum boundary-scan TCK clock frequency	66	66	MHz, Max

Table 52: **Configuration Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade		Units
		-2	-1	
BPI Master Flash Mode Programming Switching				
T_{BPICCO}(2)	ADDR[25:0], RS[1:0], FCS_B, FOE_B, FWE_B outputs valid after CCLK rising edge at 2.5V	6	6	ns
	ADDR[25:0], RS[1:0], FCS_B, FOE_B, FWE_B outputs valid after CCLK rising edge at 1.8V	6	6	ns
T_{BPIDCC}/T_{BPICCD}	Setup/Hold on D[15:0] data input pins	4.0/0.0	4.0/0.0	ns
$T_{INITADDR}$	Minimum period of initial ADDR[25:0] address cycles	3	3	CCLK cycles
SPI Master Flash Mode Programming Switching				
$T_{SPIDCC}/T_{SPIDCCD}$	DIN Setup/Hold before/after the rising CCLK edge	3.0/0.0	3.0/0.0	ns
T_{SPICCM}	MOSI clock to out at 2.5V	6	6	ns
	MOSI clock to out at 1.8V	6	6	ns
$T_{SPICCFC}$	FCS_B clock to out at 2.5V	6	6	ns
	FCS_B clock to out at 1.8V	6	6	ns
$T_{FSINIT}/T_{FSINITH}$	FS[2:0] to INIT_B rising edge Setup and Hold	2	2	µs
CCLK Output (Master Modes)				
T_{MCCKL}	Master CCLK clock Low time duty cycle	45/55	45/55	%, Min/Max
T_{MCCKH}	Master CCLK clock High time duty cycle	45/55	45/55	%, Min/Max
CCLK Input (Slave Modes)				
T_{SCCKL}	Slave CCLK clock minimum Low time	2.5	2.5	ns, Min
T_{SCCKH}	Slave CCLK clock minimum High time	2.5	2.5	ns, Min
Dynamic Reconfiguration Port (DRP) for MMCM Before and After DCLK				
F_{DCK}	Maximum frequency for DCLK	200	200	MHz
$T_{MMCMDCK\_DADDR}/T_{MMCMCKD\_DADDR}$	DADDR Setup/Hold	1.63/0.00	1.63/0.00	ns
$T_{MMCMDCK\_DI}/T_{MMCMCKD\_DI}$	DI Setup/Hold	1.63/0.00	1.63/0.00	ns
$T_{MMCMDCK\_DEN}/T_{MMCMCKD\_DEN}$	DEN Setup/Hold time	1.63/0.00	1.63/0.00	ns
$T_{MMCMDCK\_DWE}/T_{MMCMCKD\_DWE}$	DWE Setup/Hold time	1.63/0.00	1.63/0.00	ns
$T_{MMCMCKO\_DO}$	CLK to out of DO(3)	3.64	3.64	ns
$T_{MMCMCKO\_DRDY}$	CLK to out of DRDY	0.38	0.38	ns

Notes:

1. To support longer delays in configuration, use the design solutions described in *Virtex-6 FPGA Configuration Guide*.
2. Only during configuration, the last edge is determined by a weak pull-up/pull-down resistor in the I/O.
3. DO will hold until next DRP operation.

Clock Buffers and Networks

Table 53: **Global Clock Switching Characteristics (Including BUFGCTRL)**

Symbol	Description	Speed Grade		Units
		-2	-1	
$T_{BCCCK\_CE}/T_{BCCKC\_CE}$(1)	CE pins Setup/Hold	0.16/0.00	0.16/0.00	ns
T_{BCCCK_S}/T_{BCCKC_S}(1)	S pins Setup/Hold	0.16/0.00	0.16/0.00	ns
T_{BCCKO_O}(2)	BUFGCTRL delay from I0/I1 to O	0.10	0.10	ns
Maximum Frequency				
F_{MAX}	Global clock tree (BUFG)	700	700	MHz

Notes:

1. T_{BCCCK_CE} and T_{BCCKC_CE} must be satisfied to assure glitch-free operation of the global clock when switching between clocks. These parameters do not apply to the BUFGMUX_VIRTEX4 primitive that assures glitch-free operation. The other global clock setup and hold times are optional; only needing to be satisfied if device operation requires simulation matches on a cycle-for-cycle basis when switching between clocks.
2. T_{BGCKO_O} (BUFG delay from I0 to O) values are the same as T_{BCCKO_O} values.

Table 54: **Input/Output Clock Switching Characteristics (BUFIO)**

Symbol	Description	Speed Grade		Units
		-2	-1	
T_{BIOCKO_O}	Clock to out delay from I to O	0.18	0.18	ns
Maximum Frequency				
F_{MAX}	I/O clock tree (BUFIO)	710	710	MHz

Table 55: **Regional Clock Switching Characteristics (BUFR)**

Symbol	Description	Speed Grade		Units
		-2	-1	
T_{BRCKO_O}	Clock to out delay from I to O	0.75	0.75	ns
		0.75	0.75	ns
		0.75	0.75	ns
		0.75	0.75	ns
$T_{BRCKO\_O\_BYP}$	Clock to out delay from I to O with Divide Bypass attribute set	0.37	0.37	ns
		0.37	0.37	ns
		0.37	0.37	ns
		0.37	0.37	ns
T_{BRDO_O}	Propagation delay from CLR to O	0.83	0.83	ns
Maximum Frequency				
F_{MAX}	Regional clock tree (BUFR)	300	300	MHz

Table 56: **Horizontal Clock Buffer Switching Characteristics (BUFH)**

Symbol	Description	Speed Grade		Units
		-2	-1	
T_{BHCKO_O}	BUFH delay from I to O	0.13	0.13	ns
$T_{BHCCK\_CE}/T_{BHCKC\_CE}$	CE pin Setup and Hold	0.05/0.05	0.05/0.05	ns
Maximum Frequency				
F_{MAX}	Horizontal clock buffer (BUFH)	700	700	MHz

MMCM Switching Characteristics

Table 57: **MMCM Specification**

Symbol	Description	Speed Grade		Units
		-2	-1	
F_{INMAX}	Maximum Input Clock Frequency(1)	700	700	MHz
F_{INMIN}	Minimum Input Clock Frequency	10	10	MHz
$F_{INJITTER}$	Maximum Input Clock Period Jitter	< 20% of clock input period or 1 ns Max		
F_{INDUTY}	Allowable Input Duty Cycle: 10—49 MHz	25/75		%
	Allowable Input Duty Cycle: 50—199 MHz	30/70		%
	Allowable Input Duty Cycle: 200—399 MHz	35/65		%
	Allowable Input Duty Cycle: 400—499 MHz	40/60		%
	Allowable Input Duty Cycle: >500 MHz	45/55		%
F_{MIN_PSCLK}	Minimum Dynamic Phase Shift Clock Frequency	0.01	0.01	MHz
F_{MAX_PSCLK}	Maximum Dynamic Phase Shift Clock Frequency	450	450	MHz
F_{VCOMIN}	Minimum MMCM VCO Frequency	600	600	MHz
F_{VCOMAX}	Maximum MMCM VCO Frequency	1200	1200	MHz
$F_{BANDWIDTH}$	Low MMCM Bandwidth at Typical(2)	1.00	1.00	MHz
	High MMCM Bandwidth at Typical(2)	4.00	4.00	MHz

Virtex-6 CXT Device Pin-to-Pin Output Parameter Guidelines

All devices are 100% functionally tested. The representative values for typical pin locations and normal clock loading are listed in Table 58. Values are expressed in nanoseconds unless otherwise noted.

Table 58: **Global Clock Input to Output Delay Without MMCM**

Symbol	Description	Device	Speed Grade		Units
			-2	-1	
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, *without* MMCM.					
T_{ICKOF}	Global Clock input and OUTFF *without* MMCM	XC6VCX75T	5.88	5.88	ns
		XC6VCX130T	6.00	6.00	ns
		XC6VCX195T	6.13	6.13	ns
		XC6VCX240T	6.13	6.13	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

Table 59: **Global Clock Input to Output Delay With MMCM**

Symbol	Description	Device	Speed Grade		Units
			-2	-1	
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, *with* MMCM.					
$T_{ICKOFMMCMGC}$	Global Clock Input and OUTFF *with* MMCM	XC6VCX75T	2.77	2.77	ns
		XC6VCX130T	2.78	2.78	ns
		XC6VCX195T	2.78	2.78	ns
		XC6VCX240T	2.79	2.79	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. MMCM output jitter is already included in the timing calculation.

Table 60: **Clock-Capable Clock Input to Output Delay With MMCM**

Symbol	Description	Device	Speed Grade		Units
			-2	-1	
LVCMOS25 Clock-capable Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, *with* MMCM.					
$T_{ICKOFMMCMCC}$	Clock-capable Clock Input and OUTFF *with* MMCM	XC6VCX75T	2.63	2.63	ns
		XC6VCX130T	2.65	2.65	ns
		XC6VCX195T	2.65	2.65	ns
		XC6VCX240T	2.65	2.65	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. MMCM output jitter is already included in the timing calculation.

Virtex-6 CXT Device Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. The representative values for typical pin locations and normal clock loading are listed in Table 61. Values are expressed in nanoseconds unless otherwise noted.

Table 61: **Global Clock Input Setup and Hold Without MMCM**

Symbol	Description	Device	Speed Grade		Units
			-2	-1	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard.(1)					
T_{PSFD}/ T_{PHFD}	Full Delay (Legacy Delay or Default Delay) Global Clock Input and IFF(2) without MMCM	XC6VCX75T	1.75/–0.01	1.75/–0.01	ns
		XC6VCX130T	1.88/–0.11	1.88/–0.11	ns
		XC6VCX195T	1.97/–0.14	1.97/–0.14	ns
		XC6VCX240T	1.97/–0.14	1.97/–0.14	ns

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input Flip-Flop or Latch.
3. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.

Table 62: **Global Clock Input Setup and Hold With MMCM**

Symbol	Description	Device	Speed Grade		Units
			-2	-1	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard.(1)					
$T_{PSMMCMGC}$/ $T_{PHMMCMGC}$	No Delay Global Clock Input and IFF(2) with MMCM	XC6VCX75T	1.72/–0.22	1.72/–0.22	ns
		XC6VCX130T	1.81/–0.21	1.81/–0.21	ns
		XC6VCX195T	1.82/–0.20	1.82/–0.20	ns
		XC6VCX240T	1.82/–0.20	1.82/–0.20	ns

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input Flip-Flop or Latch.
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 63: **Clock-Capable Clock Input Setup and Hold With MMCM**

Symbol	Description	Device	Speed Grade		Units
			-2	-1	
Input Setup and Hold Time Relative to Clock-capable Clock Input Signal for LVCMOS25 Standard.(1)					
$T_{PSMMCMCC}$/ $T_{PHMMCMCC}$	No Delay Clock-capable Clock Input and IFF(2) with MMCM	XC6VCX75T	1.86/–0.28	1.86/–0.28	ns
		XC6VCX130T	1.93/–0.28	1.93/–0.28	ns
		XC6VCX195T	1.96/–0.27	1.96/–0.27	ns
		XC6VCX240T	1.96/–0.27	1.96/–0.27	ns

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input Flip-Flop or Latch.
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 66: **Sample Window**

Symbol	Description	Device	Speed Grade		Units
			-2	-1	
T_{SAMP}	Sampling Error at Receiver Pins(1)	All	610	610	ps
T_{SAMP_BUFIO}	Sampling Error at Receiver Pins using BUFIO(2)	All	400	400	ps

Notes:

1. This parameter indicates the total sampling error of Virtex-6 CXT FPGA DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the MMCM to capture the DDR input registers' edges of operation. These measurements include:
   - CLK0 MMCM jitter
   - MMCM accuracy (phase offset)
   - MMCM phase shift resolution

   These measurements do not include package or clock tree skew.
2. This parameter indicates the total sampling error of Virtex-6 CXT FPGA DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the BUFIO clock network and IODELAY to capture the DDR input registers' edges of operation. These measurements do not include package or clock tree skew.

Table 67: **Pin-to-Pin Setup/Hold and Clock-to-Out**

Symbol	Description	Speed Grade		Units
		-2	-1	
Data Input Setup and Hold Times Relative to a Forwarded Clock Input Pin Using BUFIO				
T_{PSCS}/T_{PHCS}	Setup/Hold of I/O clock	–0.33/1.31	–0.33/1.31	ns
Pin-to-Pin Clock-to-Out Using BUFIO				
$T_{ICKOFCS}$	Clock-to-Out of I/O clock	5.19	5.19	ns

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
07/08/09	1.0	Initial Xilinx release.
02/05/10	1.1	Removed Figure 11: Placement Diagram for the FF1156 Package (5 of 5) from page 11 as there are only 16 GTX transceivers in the FF1156 package. Corrected the placement diagrams in Figure 2 through Figure 10.