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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	10000
Number of Logic Elements/Cells	128000
Total RAM Bits	9732096
Number of I/O	600
Number of Gates	-
Voltage - Supply	0.95V ~ 1.05V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1156-BBGA, FCBGA
Supplier Device Package	1156-FCBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc6vcx130t-2ffg1156c

Virtex-6 CXT FPGA Feature Summary

Table 1: Virtex-6 CXT FPGA Feature Summary by Device

Device	Logic Cells	Configurable Logic Blocks (CLBs)		DSP48E1 Slices ⁽²⁾	Block RAM Blocks			MMCMs ⁽⁴⁾	Interface Blocks for PCI Express	Ethernet MACs ⁽⁵⁾	Maximum GTX Transceivers	Total I/O Banks ⁽⁶⁾	Max User I/O ⁽⁷⁾
		Slices ⁽¹⁾	Max Distributed RAM (Kb)		18 Kb ⁽³⁾	36 Kb	Max (Kb)						
XC6VCX75T	74,496	11,640	1,045	288	312	156	5,616	6	1	1	12	9	360
XC6VCX130T	128,000	20,000	1,740	480	528	264	9,504	10	2	1	16	15	600
XC6VCX195T	199,680	31,200	3,040	640	688	344	12,384	10	2	1	16	15	600
XC6VCX240T	241,152	37,680	3,650	768	832	416	14,976	12	2	1	16	18	600

Notes:

- Each Virtex-6 CXT FPGA slice contains four LUTs and eight flip-flops, only some slices can use their LUTs as distributed RAM or SRLs.
- Each DSP48E1 slice contains a 25 x 18 multiplier, an adder, and an accumulator.
- Block RAMs are fundamentally 36 Kbits in size. Each block can also be used as two independent 18 Kb blocks.
- Each CMT contains two mixed-mode clock managers (MMCM).
- This table lists individual Ethernet MACs per device.
- Does not include configuration Bank 0.
- This number does not include GTX transceivers.

Virtex-6 CXT FPGA Device-Package Combinations and Maximum I/Os

Virtex-6 CXT FPGA package combinations with the maximum available I/Os per package are shown in Table 2.

Table 2: Virtex-6 CXT FPGA Device-Package Combinations and Maximum Available I/Os

Package	FF484 FFG484		FF784 FFG784		FF1156 FFG1156	
Size (mm)	23 x 23		29 x 29		35 x 35	
Device	GTs	I/O	GTs	I/O	GTs	I/O
XC6VCX75T	8 GTXs	240	12 GTXs	360		
XC6VCX130T	8 GTXs	240	12 GTXs	400	16 GTXs	600
XC6VCX195T			12 GTXs	400	16 GTXs	600
XC6VCX240T			12 GTXs	400	16 GTXs	600

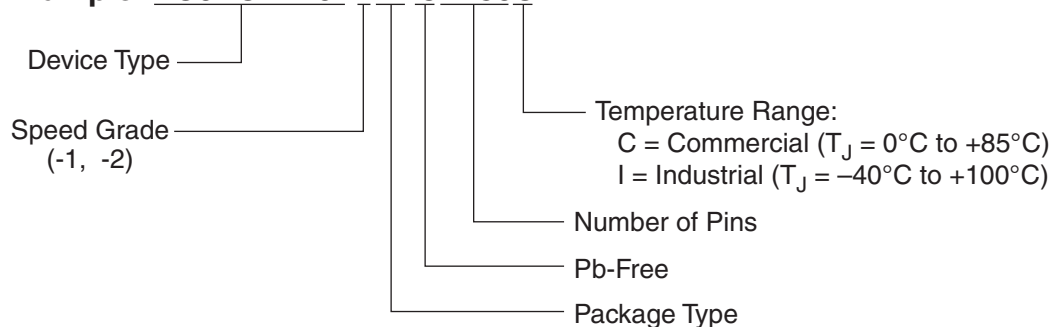
Notes:

- Flip-chip packages are also available in Pb-Free versions (FFG).

Virtex-6 CXT FPGA Ordering Information

The Virtex-6 CXT FPGA ordering information shown in Figure 1 applies to all packages including Pb-Free.

Example: XC6VCX240T-1FFG1156C



DS153_01_062109

Figure 1: Virtex-6 CXT FPGA Ordering Information

CLB Overview for CXT Devices

Table 5, updated specifically for the CXT family from a similar table in the *Virtex-6 FPGA CLB User Guide*, shows the available resources in all Virtex-6 CXT FPGA CLBs.

Table 5: Virtex-6 CXT FPGA Logic Resources Available in All CLBs

Device	Total Slices	SLICELs	SLICEMs	Number of 6-Input LUTs	Maximum Distributed RAM (Kb)	Shift Register (Kb)	Number of Flip-Flops
XC6VCX75T	11,640	7,460	4,180	46,560	1045	522.5	93,120
XC6VCX130T	20,000	13,040	6,960	80,000	1740	870	160,000
XC6VCX195T	31,200	19,040	12,160	124,800	3140	1570	249,600
XC6VCX240T	37,680	23,080	14,600	150,720	3770	1885	301,440

Regional Clock Management for CXT Devices

Table 6, updated from the *Virtex-6 FPGA Clocking Resources User Guide* specifically for the CXT family, shows the number of clock regions in all Virtex-6 CXT FPGA CLBs.

Table 6: Virtex-6 CXT FPGA Clock Regions

Device	Number of Clock Regions
XC6VCX75T	6
XC6VCX130T	10
XC6VCX195T	10
XC6VCX240T	12

CXT Packaging Specifications

Table 7, updated from the *Virtex-6 FPGA Packaging and Pinout Specifications* specifically for the CXT family, shows the number of GTX transceiver I/O channels. Table 8 shows the number of available I/Os and the number of differential I/O pairs for each Virtex-6 device/package combination.

Table 7: Number of Serial Transceivers (GTs) I/O Channels/Device

I/O Channels	Device			
	CX75T ⁽¹⁾	CX130T ⁽²⁾	CX195T ⁽³⁾	CX240T ⁽⁴⁾
MGTRXP	8 or 12	8, 12, or 16	12 or 16	12 or 16
MGTRXN	8 or 12	8, 12, or 16	12 or 16	12 or 16
MGTTXP	8 or 12	8, 12, or 16	12 or 16	12 or 16
MGTTXN	8 or 12	8, 12, or 16	12 or 16	12 or 16

Notes:

1. The XC6VCX75T has 8 GTX I/O channels in the FF484/FFG484 package and 12 GTX I/O channels in the FF784/FFG784 package.
2. The XC6VCX130T has 8 GTX I/O channels in the FF484/FFG484 package, 12 GTX I/O channels in the FF784/FFG784 package, and 16 GTX I/O channels in the FF1156/FFG1156 package.
3. The XC6VCX195T has 12 GTX I/O channels in the FF784/FFG784 package and 16 GTX I/O channels in the FF1156/FFG1156 package.
4. The XC6VCX240T has 12 GTX I/O channels in the FF784/FFG784 package and 16 GTX I/O channels in the FF1156/FFG1156 package.

FF784 Package Placement Diagrams

Figure 4 through Figure 6 show the placement diagrams for the GTX transceivers in the FF784 package.

Note: Unbonded locations in the FF784 package are:

- CX130T: X0Y0, X0Y1, X0Y2, X0Y3
- CX195T: X0Y0, X0Y1, X0Y2, X0Y3
- CX240T: X0Y0, X0Y1, X0Y2, X0Y3

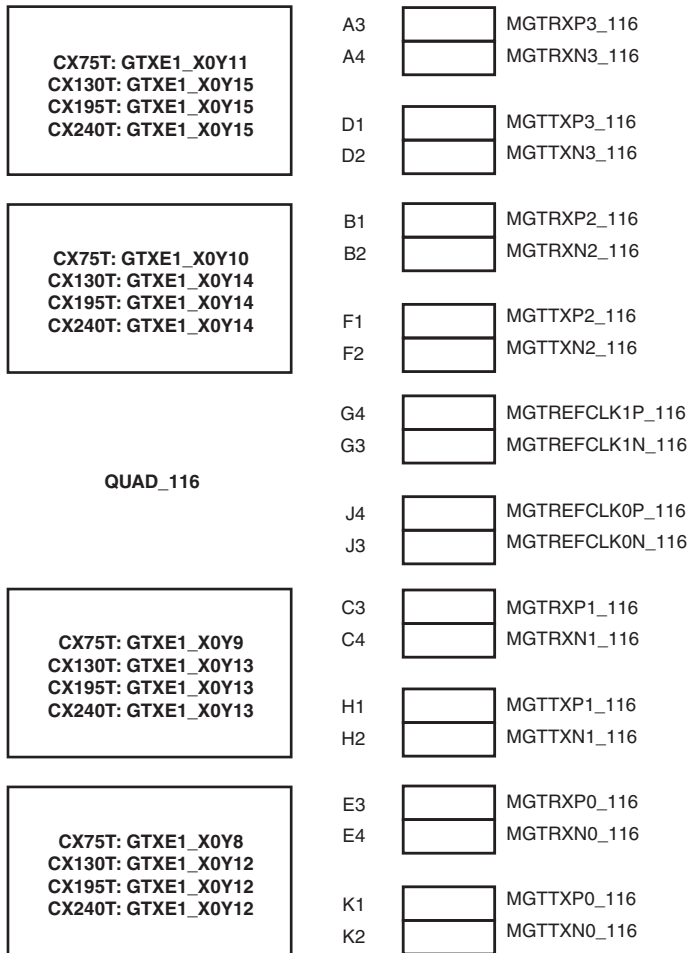


Figure 4: Placement Diagram for the FF784 Package
(1 of 3)

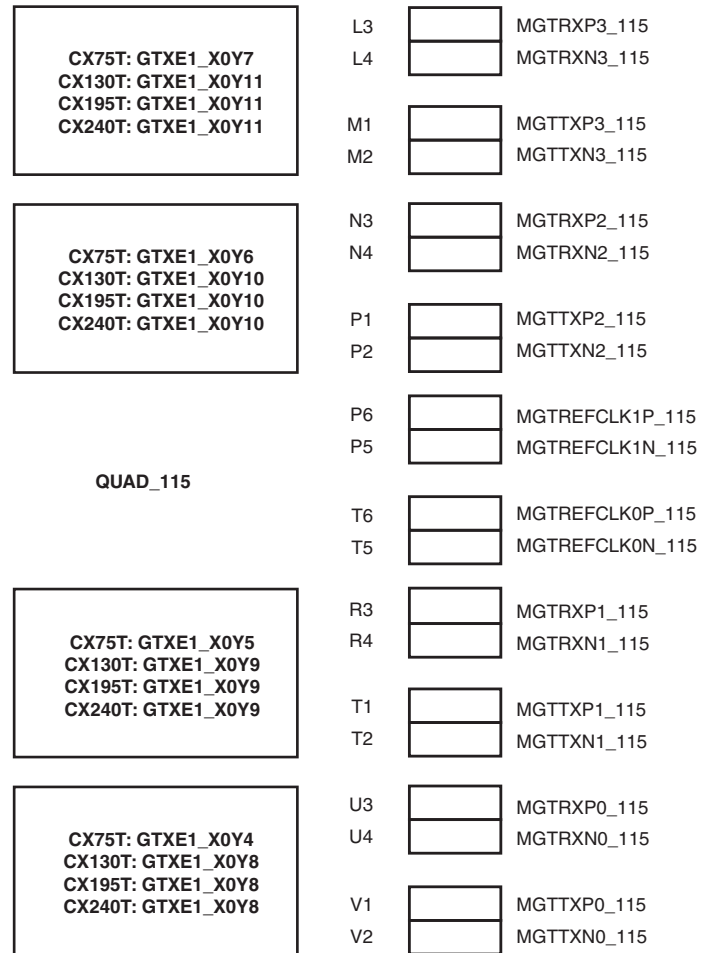


Figure 5: Placement Diagram for the FF784 Package
(2 of 3)

Table 10: Recommended Operating Conditions

Symbol	Description	Min	Max	Units
V_{CCINT}	Internal supply voltage relative to GND, $T_j = 0^\circ\text{C}$ to $+85^\circ\text{C}$	0.95	1.05	V
	Internal supply voltage relative to GND, $T_j = -40^\circ\text{C}$ to $+100^\circ\text{C}$	0.95	1.05	V
V_{CCAUX}	Auxiliary supply voltage relative to GND, $T_j = 0^\circ\text{C}$ to $+85^\circ\text{C}$	2.375	2.625	V
	Auxiliary supply voltage relative to GND, $T_j = -40^\circ\text{C}$ to $+100^\circ\text{C}$	2.375	2.625	V
$V_{CCO}^{(1)(2)(3)}$	Supply voltage relative to GND, $T_j = 0^\circ\text{C}$ to $+85^\circ\text{C}$	1.14	2.625	V
	Supply voltage relative to GND, $T_j = -40^\circ\text{C}$ to $+100^\circ\text{C}$	1.14	2.625	V
V_{IN}	2.5V supply voltage relative to GND, $T_j = 0^\circ\text{C}$ to $+85^\circ\text{C}$	GND – 0.20	2.625	V
	2.5V supply voltage relative to GND, $T_j = -40^\circ\text{C}$ to $+100^\circ\text{C}$	GND – 0.20	2.625	V
	2.5V and below supply voltage relative to GND, $T_j = 0^\circ\text{C}$ to $+85^\circ\text{C}$	GND – 0.20	$V_{CCO} + 0.2$	V
	2.5V and below supply voltage relative to GND, $T_j = -40^\circ\text{C}$ to $+100^\circ\text{C}$	GND – 0.20	$V_{CCO} + 0.2$	V
$I_{IN}^{(4)}$	Maximum current through any pin in a powered or unpowered bank when forward biasing the clamp diode.	–	10	mA
$V_{BATT}^{(5)}$	Battery voltage relative to GND, $T_j = 0^\circ\text{C}$ to $+85^\circ\text{C}$	1.0	2.5	V
	Battery voltage relative to GND, $T_j = -40^\circ\text{C}$ to $+100^\circ\text{C}$	1.0	2.5	V
$V_{FS}^{(6)}$	External voltage supply for eFUSE programming	2.375	2.625	V

Notes:

1. Configuration data is retained even if V_{CCO} drops to 0V.
2. Includes V_{CCO} of 1.2V, 1.5V, 1.8V, and 2.5V.
3. The configuration supply voltage V_{CC_CONFIG} is also known as V_{CCO_0} .
4. A total of 100 mA per bank should not be exceeded.
5. V_{BATT} is required only when using bitstream encryption. If battery is not used, connect V_{BATT} to either ground or V_{CCAUX} .
6. When not programming eFUSE, connect V_{FS} to GND.
7. All voltages are relative to ground.

Table 11: DC Characteristics Over Recommended Operating Conditions⁽¹⁾⁽²⁾

Symbol	Description	Min	Typ	Max	Units
V_{DRINT}	Data retention V_{CCINT} voltage (below which configuration data might be lost)	0.75	–	–	V
V_{DRI}	Data retention V_{CCAUX} voltage (below which configuration data might be lost)	2.0	–	–	V
I_{REF}	V_{REF} leakage current per pin	–	–	10	μA
I_L	Input or output leakage current per pin (sample-tested)	–	–	10	μA
$C_{IN}^{(3)}$	Die input capacitance at the pad	–	–	8	pF
I_{RPU}	Pad pull-up (when selected) @ $V_{IN} = 0\text{V}$, $V_{CCO} = 2.5\text{V}$	20	–	80	μA
	Pad pull-up (when selected) @ $V_{IN} = 0\text{V}$, $V_{CCO} = 1.8\text{V}$	8	–	40	μA
	Pad pull-up (when selected) @ $V_{IN} = 0\text{V}$, $V_{CCO} = 1.5\text{V}$	5	–	30	μA
	Pad pull-up (when selected) @ $V_{IN} = 0\text{V}$, $V_{CCO} = 1.2\text{V}$	1	–	20	μA
I_{RPD}	Pad pull-down (when selected) @ $V_{IN} = 2.5\text{V}$	3	–	80	μA
I_{BATT}	Battery supply current	–	–	150	nA
n	Temperature diode ideality factor	–	1.0002	–	n
r	Series resistance	–	5	–	Ω

Notes:

1. Typical values are specified at nominal voltage, 25°C .
2. Maximum value specified for worst case process at 25°C .
3. This measurement represents the die capacitance at the pad, not including the package.

Quiescent Supply Current: Important Note

Typical values for quiescent supply current are specified at nominal voltage, 85°C junction temperatures (T_j). Xilinx recommends analyzing static power consumption at $T_j = 85^\circ\text{C}$ because the majority of designs operate near the high end of the commercial temperature range. Quiescent supply current is specified by speed grade for Virtex-6 CXT devices. Use the XPOWER™ Estimator (XPE) spreadsheet tool (download at <http://www.xilinx.com/power>) to calculate static power consumption for conditions other than those specified in Table 12.

Table 12: Typical Quiescent Supply Current

Symbol	Description	Device	Speed and Temperature Grade		Units
			-2 (C & I)	-1 (C & I)	
I_{CCINTQ}	Quiescent V_{CCINT} supply current	XC6VCX75T	927	927	mA
		XC6VCX130T	1563	1563	mA
		XC6VCX195T	2059	2059	mA
		XC6VCX240T	2478	2478	mA
I_{CCOQ}	Quiescent V_{CCO} supply current	XC6VCX75T	1	1	mA
		XC6VCX130T	1	1	mA
		XC6VCX195T	1	1	mA
		XC6VCX240T	2	2	mA
I_{CCAUXQ}	Quiescent V_{CCAUX} supply current	XC6VCX75T	45	45	mA
		XC6VCX130T	75	75	mA
		XC6VCX195T	113	113	mA
		XC6VCX240T	135	135	mA

Notes:

1. Typical values are specified at nominal voltage, 85°C junction temperatures (T_j). Industrial (I) grade devices have the same typical values as commercial (C) grade devices at 85°C, but higher values at 100°C. Use the XPE tool to calculate 100°C values.
2. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
3. If DCI or differential signaling is used, more accurate quiescent current estimates can be obtained by using the XPOWER Estimator (XPE) or XPOWER Analyzer (XPA) tools.

Power-On Power Supply Requirements

Xilinx FPGAs require a certain amount of supply current during power-on to insure proper device initialization. The actual current consumed depends on the power-on ramp rate of the power supply.

Virtex-6 CXT devices require a power-on sequence of V_{CCINT} , V_{CCAUX} , and V_{CCO} . If the requirement can not be met, then V_{CCAUX} must always be powered prior to V_{CCO} . V_{CCAUX} and V_{CCO} can be powered by the same supply, therefore, both V_{CCAUX} and V_{CCO} are permitted to ramp simultaneously. Similarly, for the power-down sequence, V_{CCO} must be powered down prior to V_{CCAUX} or if powered by the same supply, V_{CCAUX} and V_{CCO} power-down simultaneously.

Table 13 shows the minimum current, in addition to I_{CCOQ} , that are required by Virtex-6 CXT devices for proper power-on and configuration. If the current minimums shown in Table 12 and Table 13 are met, the device powers on after all three supplies have passed through their power-on reset threshold voltages. The FPGA must be configured after V_{CCINT} is applied.

Once initialized and configured, use the XPOWER tools to estimate current drain on these supplies.

Table 13: Power-On Current for Virtex-6 CXT Devices

Device	$I_{CCINTMIN}$	$I_{CCAUXMIN}$	I_{CCOMIN}	Units
	Typ ⁽¹⁾	Typ ⁽¹⁾	Typ ⁽¹⁾	
XC6VCX75T	See I_{CCINTQ} in Table 12	$I_{CCAUXQ} + 10$	$I_{CCOQ} + 30$ mA per bank	mA
XC6VCX130T	See I_{CCINTQ} in Table 12	$I_{CCAUXQ} + 10$	$I_{CCOQ} + 30$ mA per bank	mA
XC6VCX195T	See I_{CCINTQ} in Table 12	$I_{CCAUXQ} + 40$	$I_{CCOQ} + 30$ mA per bank	mA
XC6VCX240T	See I_{CCINTQ} in Table 12	$I_{CCAUXQ} + 40$	$I_{CCOQ} + 30$ mA per bank	mA

Notes:

1. Typical values are specified at nominal voltage, 25°C.
2. Use the XPOWER™ Estimator (XPE) spreadsheet tool (download at <http://www.xilinx.com/power>) to calculate maximum power-on currents.

Table 14: Power Supply Ramp Time

Symbol	Description	Ramp Time	Units
V_{CCINT}	Internal supply voltage relative to GND	0.20 to 50.0	ms
V_{CCO}	Output drivers supply voltage relative to GND	0.20 to 50.0	ms
V_{CCAUX}	Auxiliary supply voltage relative to GND	0.20 to 50.0	ms

SelectIO™ DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

Table 15: SelectIO DC Input and Output Levels

I/O Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
LVC MOS25, LVDCI25	-0.3	0.7	1.7	$V_{CCO} + 0.3$	0.4	$V_{CCO} - 0.4$	Note(3)	Note(3)
LVC MOS18, LVDCI18	-0.3	35% V_{CCO}	65% V_{CCO}	$V_{CCO} + 0.3$	0.45	$V_{CCO} - 0.45$	Note(4)	Note(4)
LVC MOS15, LVDCI15	-0.3	35% V_{CCO}	65% V_{CCO}	$V_{CCO} + 0.3$	25% V_{CCO}	75% V_{CCO}	Note(4)	Note(4)
LVC MOS12	-0.3	35% V_{CCO}	65% V_{CCO}	$V_{CCO} + 0.3$	25% V_{CCO}	75% V_{CCO}	Note(5)	Note(5)
HSTL I ₁₂	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	$V_{CCO} + 0.3$	25% V_{CCO}	75% V_{CCO}	6.3	6.3
HSTL I ⁽²⁾	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	$V_{CCO} + 0.3$	0.4	$V_{CCO} - 0.4$	8	-8
HSTL II ⁽²⁾	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	$V_{CCO} + 0.3$	0.4	$V_{CCO} - 0.4$	16	-16
HSTL III ⁽²⁾	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	$V_{CCO} + 0.3$	0.4	$V_{CCO} - 0.4$	24	-8
DIFF HSTL I ⁽²⁾	-0.3	50% $V_{CCO} - 0.1$	50% $V_{CCO} + 0.1$	$V_{CCO} + 0.3$	—	—	—	—
DIFF HSTL II ⁽²⁾	-0.3	50% $V_{CCO} - 0.1$	50% $V_{CCO} + 0.1$	$V_{CCO} + 0.3$	—	—	—	—
SSTL2 I	-0.3	$V_{REF} - 0.15$	$V_{REF} + 0.15$	$V_{CCO} + 0.3$	$V_{TT} - 0.61$	$V_{TT} + 0.61$	8.1	-8.1
SSTL2 II	-0.3	$V_{REF} - 0.15$	$V_{REF} + 0.15$	$V_{CCO} + 0.3$	$V_{TT} - 0.81$	$V_{TT} + 0.81$	16.2	-16.2
DIFF SSTL2 I	-0.3	50% $V_{CCO} - 0.15$	50% $V_{CCO} + 0.15$	$V_{CCO} + 0.3$	—	—	—	—
DIFF SSTL2 II	-0.3	50% $V_{CCO} - 0.15$	50% $V_{CCO} + 0.15$	$V_{CCO} + 0.3$	—	—	—	—
SSTL18 I	-0.3	$V_{REF} - 0.125$	$V_{REF} + 0.125$	$V_{CCO} + 0.3$	$V_{TT} - 0.47$	$V_{TT} + 0.47$	6.7	-6.7
SSTL18 II	-0.3	$V_{REF} - 0.125$	$V_{REF} + 0.125$	$V_{CCO} + 0.3$	$V_{TT} - 0.60$	$V_{TT} + 0.60$	13.4	-13.4
DIFF SSTL18 I	-0.3	50% $V_{CCO} - 0.125$	50% $V_{CCO} + 0.125$	$V_{CCO} + 0.3$	—	—	—	—
DIFF SSTL18 II	-0.3	50% $V_{CCO} - 0.125$	50% $V_{CCO} + 0.125$	$V_{CCO} + 0.3$	—	—	—	—
SSTL15	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	$V_{CCO} + 0.3$	$V_{TT} - 0.175$	$V_{TT} + 0.175$	14.3	14.3

Notes:

1. Tested according to relevant specifications.
2. Applies to both 1.5V and 1.8V HSTL.
3. Using drive strengths of 2, 4, 6, 8, 12, 16, or 24 mA.
4. Using drive strengths of 2, 4, 6, 8, 12, or 16 mA.
5. Supported drive strengths of 2, 4, 6, or 8 mA.
6. For detailed interface specific DC voltage levels, see the *Virtex-6 FPGA SelectIO Resources User Guide*.

LVPECL DC Specifications (LVPECL_25)

These values are valid when driving a 100Ω differential load only, i.e., a 100Ω resistor between the two receiver pins. The V_{OH} levels are 200 mV below standard LVPECL levels and are compatible with devices tolerant of lower common-mode ranges. Table 19 summarizes the DC output specifications of LVPECL. For more information on using LVPECL, see the *Virtex-6 FPGA SelectIO Resources User Guide*.

Table 19: LVPECL DC Specifications

Symbol	DC Parameter	Min	Typ	Max	Units
V_{OH}	Output High Voltage	$V_{CC} - 1.025$	1.545	$V_{CC} - 0.88$	V
V_{OL}	Output Low Voltage	$V_{CC} - 1.81$	0.795	$V_{CC} - 1.62$	V
V_{ICM}	Input Common-Mode Voltage	0.6	—	2.2	V
V_{IDIFF}	Differential Input Voltage ⁽¹⁾⁽²⁾	0.100	—	1.5	V

Notes:

1. Recommended input maximum voltage not to exceed $V_{CCAUX} + 0.2V$.
2. Recommended input minimum voltage not to go below $-0.5V$.

eFUSE Read Endurance

Table 20 lists the maximum number of read cycle operations expected. For more information, see the *Virtex-6 FPGA Configuration User Guide*.

Table 20: eFUSE Read Endurance

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
DNA_CYCLES	Number of DNA_PORT READ operations or JTAG ISC_DNA read command operations. Unaffected by SHIFT operations.	30,000,000				Read Cycles
AES_CYCLES	Number of JTAG FUSE_KEY or FUSE_CNTL read command operations. Unaffected by SHIFT operations.	30,000,000				Read Cycles

GTX Transceiver Specifications

GTX Transceiver DC Characteristics

Table 21: Absolute Maximum Ratings for GTX Transceivers⁽¹⁾

Symbol	Description	Min	Max	Units
MGTA VCC	Analog supply voltage for the GTX transmitter and receiver circuits relative to GND	-0.5	1.1	V
MGTA VTT	Analog supply voltage for the GTX transmitter and receiver termination circuits relative to GND	-0.5	1.32	V
MGTA VTTRCAL	Analog supply voltage for the resistor calibration circuit of the GTX transceiver column	-0.5	1.32	V
V_{IN}	Receiver (RXP/RXN) and Transmitter (TXP/TXN) absolute input voltage	-0.5	1.32	V
$V_{MGTRFCLK}$	Reference clock absolute input voltage	-0.5	1.32	V

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.

Table 26 summarizes the DC specifications of the clock input of the GTX transceiver. Consult the *Virtex-6 FPGA GTX Transceivers User Guide* for further details.

Table 26: GTX Transceiver Clock DC Input Level Specification

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{IDIFF}	Differential peak-to-peak input voltage		210	800	2000	mV
R_{IN}	Differential input resistance		90	100	130	Ω
C_{EXT}	Required external AC coupling capacitor		—	100	—	nF

GTX Transceiver Switching Characteristics

Consult *Virtex-6 FPGA GTX Transceivers User Guide* for further information.

Table 27: GTX Transceiver Performance

Symbol	Description	Speed Grade		Units
		-2	-1	
F_{GTXMAX}	Maximum GTX transceiver data rate	3.75	3.75	Gb/s
$F_{GPLLMAX}$	Maximum PLL frequency	2.5	2.5	GHz
$F_{GPLLMIN}$	Minimum PLL frequency	1.2	1.2	GHz

Table 28: GTX Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics

Symbol	Description	Speed Grade		Units
		-2	-1	
$F_{GTXDRPCLK}$	GTXDRPCLK maximum frequency	100	100	MHz

Table 29: GTX Transceiver Reference Clock Switching Characteristics

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
F_{GCLK}	Reference clock frequency range		67.5	—	375	MHz
T_{RCLK}	Reference clock rise time	20% – 80%	—	200	—	ps
T_{FCLK}	Reference clock fall time	80% – 20%	—	200	—	ps
T_{DCREF}	Reference clock duty cycle	Transceiver PLL only	45	50	55	%
T_{LOCK}	Clock recovery frequency acquisition time	Initial PLL lock	—	—	1	ms
T_{PHASE}	Clock recovery phase acquisition time	Lock to data after PLL has locked to the reference clock	—	—	200	μ s

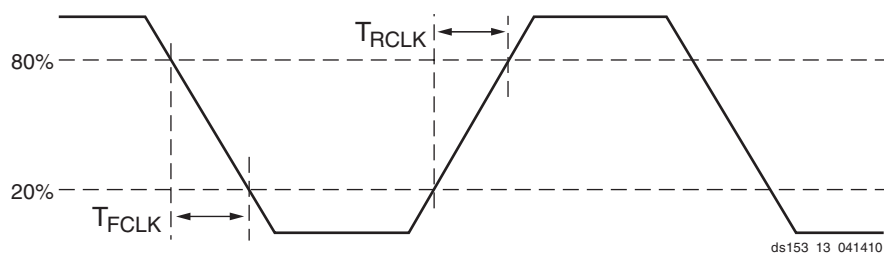


Figure 13: Reference Clock Timing Parameters

Ethernet MAC Switching Characteristics

Consult *Virtex-6 FPGA Embedded Tri-mode Ethernet MAC User Guide* for further information.

Table 33: Maximum Ethernet MAC Performance

Symbol	Description	Conditions	Speed Grade		Units
			-2	-1	
F _{TEMACCLIENT}	Client interface maximum frequency	10 Mb/s – 8-bit width	2.5 ⁽¹⁾	2.5 ⁽¹⁾	MHz
		100 Mb/s – 8-bit width	25 ⁽²⁾	25 ⁽²⁾	MHz
		1000 Mb/s – 8-bit width	125	125	MHz
		1000 Mb/s – 16-bit width	62.5	62.5	MHz
F _{TEMACPHY}	Physical interface maximum frequency	10 Mb/s – 4-bit width	2.5	2.5	MHz
		100 Mb/s – 4-bit width	25	25	MHz
		1000 Mb/s – 8-bit width	125	125	MHz

Notes:

1. When not using clock enable, the F_{MAX} is lowered to 1.25 MHz.
2. When not using clock enable, the F_{MAX} is lowered to 12.5 MHz.

Integrated Interface Block for PCI Express Designs Switching Characteristics

More information and documentation on solutions for PCI Express designs can be found at:

<http://www.xilinx.com/technology/protocols/pciexpress.htm>

Table 34: Maximum Performance for PCI Express Designs

Symbol	Description	Speed Grade		Units
		-2	-1	
F _{PIPECLK}	Pipe clock maximum frequency	125	125	MHz
F _{USERCLK}	User clock maximum frequency	250	250	MHz
F _{DRPCLK}	DRP clock maximum frequency	250	250	MHz

IOB Pad Input/Output/3-State Switching Characteristics

Table 38 summarizes the values of standard-specific data input delay adjustments, output delays terminating at pads (based on standard) and 3-state delays.

T_{IOPI} is described as the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.

T_{IOOP} is described as the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.

T_{IOTP} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer.

Table 39 summarizes the value of T_{IOTPHZ} . T_{IOTPHZ} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is enabled (i.e., a high impedance state).

Table 38: IOB Switching Characteristics

I/O Standard	T _{IOPI}		T _{IOOP}		T _{IOTP}		Units
	Speed Grade		Speed Grade		Speed Grade		
	-2	-1	-2	-1	-2	-1	
LVDS_25	1.09	1.09	1.68	1.68	1.68	1.68	ns
LVDSEXT_25	1.09	1.09	1.84	1.84	1.84	1.84	ns
HT_25	1.09	1.09	1.78	1.78	1.78	1.78	ns
BLVDS_25	1.09	1.09	1.67	1.67	1.67	1.67	ns
RSDS_25 (point to point)	1.09	1.09	1.68	1.68	1.68	1.68	ns
HSTL_I	1.06	1.06	1.73	1.73	1.73	1.73	ns
HSTL_II	1.06	1.06	1.74	1.74	1.74	1.74	ns
HSTL_III	1.06	1.06	1.71	1.71	1.71	1.71	ns
HSTL_I_18	1.06	1.06	1.75	1.75	1.75	1.75	ns
HSTL_II_18	1.06	1.06	1.81	1.81	1.81	1.81	ns
HSTL_III_18	1.06	1.06	1.71	1.71	1.71	1.71	ns
SSTL2_I	1.06	1.06	1.77	1.77	1.77	1.77	ns
SSTL2_II	1.06	1.06	1.72	1.72	1.72	1.72	ns
SSTL15	1.06	1.06	1.71	1.71	1.71	1.71	ns
LVC MOS25, Slow, 2 mA	0.66	0.66	6.01	6.01	6.01	6.01	ns
LVC MOS25, Slow, 4 mA	0.66	0.66	3.79	3.79	3.79	3.79	ns
LVC MOS25, Slow, 6 mA	0.66	0.66	3.08	3.08	3.08	3.08	ns
LVC MOS25, Slow, 8 mA	0.66	0.66	2.72	2.72	2.72	2.72	ns
LVC MOS25, Slow, 12 mA	0.66	0.66	2.17	2.17	2.17	2.17	ns
LVC MOS25, Slow, 16 mA	0.66	0.66	2.29	2.29	2.29	2.29	ns
LVC MOS25, Slow, 24 mA	0.66	0.66	2.02	2.02	2.02	2.02	ns
LVC MOS25, Fast, 2 mA	0.66	0.66	6.04	6.04	6.04	6.04	ns
LVC MOS25, Fast, 4 mA	0.66	0.66	3.82	3.82	3.82	3.82	ns
LVC MOS25, Fast, 6 mA	0.66	0.66	2.99	2.99	2.99	2.99	ns
LVC MOS25, Fast, 8 mA	0.66	0.66	2.65	2.65	2.65	2.65	ns
LVC MOS25, Fast, 12 mA	0.66	0.66	2.08	2.08	2.08	2.08	ns
LVC MOS25, Fast, 16 mA	0.66	0.66	2.13	2.13	2.13	2.13	ns
LVC MOS25, Fast, 24 mA	0.66	0.66	1.99	1.99	1.99	1.99	ns

Table 38: IOB Switching Characteristics (Cont'd)

I/O Standard	T _{IOPI}		T _{IOOP}		T _{IOTP}		Units
	Speed Grade		Speed Grade		Speed Grade		
	-2	-1	-2	-1	-2	-1	
DIFF_SSTL18_II_T_DCI	1.09	1.09	1.67	1.67	1.67	1.67	ns
DIFF_SSTL15	1.06	1.06	1.71	1.71	1.71	1.71	ns
DIFF_SSTL15_DCI	1.06	1.06	1.68	1.68	1.68	1.68	ns
DIFF_SSTL15_T_DCI	1.06	1.06	1.68	1.68	1.68	1.68	ns

Table 39: IOB 3-state ON Output Switching Characteristics (T_{IOTPHZ})

Symbol	Description	Speed Grade		Units
		-2	-1	
T_{IOTPHZ}	T input to Pad high-impedance	0.99	0.99	ns

I/O Standard Adjustment Measurement Methodology

Input Delay Measurements

Table 40 shows the test setup parameters used for measuring input delay.

Table 40: Input Delay Measurement Methodology

Description	I/O Standard Attribute	$V_L^{(1)(2)}$	$V_H^{(1)(2)}$	$V_{MEAS}^{(1,4,5)}$	$V_{REF}^{(1,3,5)}$
LVC MOS, 2.5V	LVC MOS25	0	2.5	1.25	—
LVC MOS, 1.8V	LVC MOS18	0	1.8	0.9	—
LVC MOS, 1.5V	LVC MOS15	0	1.5	0.75	—
HSTL (High-Speed Transceiver Logic), Class I & II	HSTL_I, HSTL_II	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	0.75
HSTL, Class III	HSTL_III	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	0.90
HSTL, Class I & II, 1.8V	HSTL_I_18, HSTL_II_18	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	0.90
HSTL, Class III 1.8V	HSTL_III_18	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	1.08
SSTL (Stub Terminated Transceiver Logic), Class I & II, 3.3V	SSTL3_I, SSTL3_II	$V_{REF} - 1.00$	$V_{REF} + 1.00$	V_{REF}	1.5
SSTL, Class I & II, 2.5V	SSTL2_I, SSTL2_II	$V_{REF} - 0.75$	$V_{REF} + 0.75$	V_{REF}	1.25
SSTL, Class I & II, 1.8V	SSTL18_I, SSTL18_II	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	0.90
LVDS (Low-Voltage Differential Signaling), 2.5V	LVDS_25	$1.2 - 0.125$	$1.2 + 0.125$	0 ⁽⁶⁾	—
LVDS EXT (LVDS Extended Mode), 2.5V	LVDS EXT_25	$1.2 - 0.125$	$1.2 + 0.125$	0 ⁽⁶⁾	—
HT (HyperTransport), 2.5V	LDT_25	$0.6 - 0.125$	$0.6 + 0.125$	0 ⁽⁶⁾	—

Notes:

- The input delay measurement methodology parameters for LVDCI are the same for LVC MOS standards of the same voltage. Input delay measurement methodology parameters for HSLVDCI are the same as for HSTL_II standards of the same voltage. Parameters for all other DCI standards are the same for the corresponding non-DCI standards.
- Input waveform switches between V_L and V_H .
- Measurements are made at typical, minimum, and maximum V_{REF} values. Reported delays reflect worst case of these measurements. V_{REF} values listed are typical.
- Input voltage level from which measurement starts.
- This is an input voltage reference that bears no relation to the V_{REF} / V_{MEAS} parameters found in IBIS models and/or noted in Figure 14.
- The value given is the differential output voltage.

Table 41: Output Delay Measurement Methodology (Cont'd)

Description	I/O Standard Attribute	R_{REF} (Ω)	$C_{REF}^{(1)}$ (pF)	V_{MEAS} (V)	V_{REF} (V)
HT (HyperTransport), 2.5V	LDT_25	100	0	0 ⁽²⁾	0.6
LVPECL (Low-Voltage Positive Emitter-Coupled Logic), 2.5V	LVPECL_25	100	0	0 ⁽²⁾	0
LVDCI/HSLVDCI, 2.5V	LVDCI_25, HSLVDCI_25	1M	0	1.25	0
LVDCI/HSLVDCI, 1.8V	LVDCI_18, HSLVDCI_18	1M	0	0.9	0
LVDCI/HSLVDCI, 1.5V	LVDCI_15, HSLVDCI_15	1M	0	0.75	0
HSTL (High-Speed Transceiver Logic), Class I & II, with DCI	HSTL_I_DCI, HSTL_II_DCI	50	0	V_{REF}	0.75
HSTL, Class III, with DCI	HSTL_III_DCI	50	0	0.9	1.5
HSTL, Class I & II, 1.8V, with DCI	HSTL_I_DCI_18, HSTL_II_DCI_18	50	0	V_{REF}	0.9
HSTL, Class III, 1.8V, with DCI	HSTL_III_DCI_18	50	0	1.1	1.8
SSTL (Stub Series Termini.Logic), Class I & II, 1.8V, with DCI	SSTL18_I_DCI, SSTL18_II_DCI	50	0	V_{REF}	0.9
SSTL, Class I & II, 2.5V, with DCI	SSTL2_I_DCI, SSTL2_II_DCI	50	0	V_{REF}	1.25

Notes:

1. C_{REF} is the capacitance of the probe, nominally 0 pF.
2. The value given is the differential output voltage.

Input/Output Logic Switching Characteristics

Table 42: ILOGIC Switching Characteristics

Symbol	Description	Speed Grade		Units
		-2	-1	
Setup/Hold				
T _{ICE1CK} /T _{ICKCE1}	CE1 pin Setup/Hold with respect to CLK	0.27/0.04	0.27/0.04	ns
T _{ISRCK} /T _{ICKSR}	SR pin Setup/Hold with respect to CLK	0.96/–0.10	0.96/–0.10	ns
T _{IDOCK} /T _{IOCKD}	D pin Setup/Hold with respect to CLK without Delay	0.10/0.54	0.10/0.54	ns
T _{IDOCKD} /T _{IOCKDD}	DDLY pin Setup/Hold with respect to CLK (using IODELAY)	0.14/0.42	0.14/0.40	ns
Combinatorial				
T _{IDI}	D pin to O pin propagation delay, no Delay	0.20	0.20	ns
T _{IDID}	DDLY pin to O pin propagation delay (using IODELAY)	0.25	0.25	ns
Sequential Delays				
T _{IDLO}	D pin to Q1 pin using flip-flop as a latch without Delay	0.64	0.64	ns
T _{IDLOD}	DDLY pin to Q1 pin using flip-flop as a latch (using IODELAY)	0.68	0.68	ns
T _{ICKQ}	CLK to Q outputs	0.71	0.71	ns
T _{RQ_ILOGIC}	SR pin to OQ/TQ out	1.15	1.15	ns
T _{GSRQ_ILOGIC}	Global Set/Reset to Q outputs	10.51	10.51	ns
Set/Reset				
T _{RPW_ILOGIC}	Minimum Pulse Width, SR inputs	1.20	1.20	ns, Min

Output Serializer/Deserializer Switching Characteristics

Table 45: OSERDES Switching Characteristics

Symbol	Description	Speed Grade		Units
		-2	-1	
Setup/Hold				
T _{OSDCK_D} /T _{OSCKD_D}	D input Setup/Hold with respect to CLKDIV	0.31/−0.12	0.31/−0.12	ns
T _{OSDCK_T} /T _{OSCKD_T} ⁽¹⁾	T input Setup/Hold with respect to CLK	0.56/−0.08	0.56/−0.08	ns
T _{OSDCK_T2} /T _{OSCKD_T2} ⁽¹⁾	T input Setup/Hold with respect to CLKDIV	0.31/−0.08	0.31/−0.08	ns
T _{OSCCK_OCE} /T _{OSCKC_OCE}	OCE input Setup/Hold with respect to CLK	0.22/−0.05	0.22/−0.05	ns
T _{OSCCK_S}	SR (Reset) input Setup with respect to CLKDIV	0.07	0.07	ns
T _{OSCCK_TCE} /T _{OSCKC_TCE}	TCE input Setup/Hold with respect to CLK	0.21/−0.05	0.21/−0.05	ns
Sequential Delays				
T _{OSCKO_OQ}	Clock to out from CLK to OQ	0.82	0.82	ns
T _{OSCKO_TQ}	Clock to out from CLK to TQ	0.82	0.82	ns
Combinatorial				
T _{OSDO_TTQ}	T input to TQ Out	0.97	0.97	ns

Notes:

- T_{OSDCK_T2} and T_{OSCKD_T2} are reported as T_{OSDCK_T}/T_{OSCKD_T} in the TRACE report.

CLB Distributed RAM Switching Characteristics (SLICEM Only)

Table 48: CLB Distributed RAM Switching Characteristics

Symbol	Description	Speed Grade		Units
		-2	-1	
Sequential Delays				
T _{SHCKO}	Clock to A – B outputs	1.36	1.56	ns, Max
T _{SHCKO_1}	Clock to AMUX – BMUX outputs	1.71	1.96	ns, Max
Setup and Hold Times Before/After Clock CLK				
T _{DS} /T _{DH}	A – D inputs to CLK	0.88/0.22	1.01/0.26	ns, Min
T _{AS} /T _{AH}	Address An inputs to clock	0.27/0.70	0.31/0.80	ns, Min
T _{WS} /T _{WH}	WE input to clock	0.40/–0.01	0.46/0.00	ns, Min
T _{CECK} /T _{CKCE}	CE input to CLK	0.41/–0.02	0.48/–0.01	ns, Min
Clock CLK				
T _{MPW}	Minimum pulse width	1.00	1.15	ns, Min
T _{MCP}	Minimum clock period	2.00	2.30	ns, Min

Notes:

1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values cannot be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.
2. T_{SHCKO} also represents the CLK to XMUX output. Refer to the TRACE report for the CLK to XMUX path.

CLB Shift Register Switching Characteristics (SLICEM Only)

Table 49: CLB Shift Register Switching Characteristics

Symbol	Description	Speed Grade		Units
		-2	-1	
Sequential Delays				
T _{REG}	Clock to A – D outputs	1.58	1.82	ns, Max
T _{REG_MUX}	Clock to AMUX – DMUX output	1.93	2.22	ns, Max
T _{REG_M31}	Clock to DMUX output via M31 output	1.55	1.78	ns, Max
Setup and Hold Times Before/After Clock CLK				
T _{WS} /T _{WH}	WE input	0.09/–0.01	0.10/0.00	ns, Min
T _{CECK} /T _{CKCE}	CE input to CLK	0.10/–0.02	0.11/–0.01	ns, Min
T _{DS} /T _{DH}	A – D inputs to CLK	0.94/0.24	1.08/0.28	ns, Min
Clock CLK				
T _{MPW}	Minimum pulse width	0.85	0.98	ns, Min

Notes:

1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values cannot be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

Block RAM and FIFO Switching Characteristics

Table 50: Block RAM and FIFO Switching Characteristics

Symbol	Description	Speed Grade		Units
		-2	-1	
Block RAM and FIFO Clock-to-Out Delays				
T _{RCKO_DO} and T _{RCKO_DO_REG} ⁽¹⁾	Clock CLK to DOUT output (without output register) ⁽²⁾⁽³⁾	2.08	2.39	ns, Max
	Clock CLK to DOUT output (with output register) ⁽⁴⁾⁽⁵⁾	0.75	0.86	ns, Max
T _{RCKO_DO_ECC} and T _{RCKO_DO_ECC_REG}	Clock CLK to DOUT output with ECC (without output register) ⁽²⁾⁽³⁾	3.30	3.79	ns, Max
	Clock CLK to DOUT output with ECC (with output register) ⁽⁴⁾⁽⁵⁾	0.86	0.98	ns, Max
T _{RCKO_CASC} and T _{RCKO_CASC_REG}	Clock CLK to DOUT output with Cascade (without output register) ⁽²⁾	3.18	3.65	ns, Max
	Clock CLK to DOUT output with Cascade (with output register) ⁽⁴⁾	1.58	1.81	ns, Max
T _{RCKO_FLAGS}	Clock CLK to FIFO flags outputs ⁽⁶⁾	0.91	1.05	ns, Max
T _{RCKO_POINTERS}	Clock CLK to FIFO pointers outputs ⁽⁷⁾	1.09	1.25	ns, Max
T _{RCKO_RDCOUNT}	Clock CLK to FIFO Read Counter	1.09	1.25	ns, Max
T _{RCKO_WRCOUNT}	Clock CLK to FIFO Write Counter	1.09	1.25	ns, Max
T _{RCKO_SDBIT_ECC} and T _{RCKO_SDBIT_ECC_REG}	Clock CLK to BITERR (with output register)	0.76	0.87	ns, Max
	Clock CLK to BITERR (without output register)	2.84	3.26	ns, Max
T _{RCKO_PARITY_ECC}	Clock CLK to ECCPARITY in ECC encode only mode	1.06	1.21	ns, Max
T _{RCKO_RDADDR_ECC} and T _{RCKO_RDADDR_ECC_REG}	Clock CLK to RDADDR output with ECC (without output register)	0.90	1.03	ns, Max
	Clock CLK to RDADDR output with ECC (with output register)	0.92	1.06	ns, Max
Setup and Hold Times Before/After Clock CLK				
T _{RCCK_ADDR} /T _{RCKC_ADDR}	ADDR inputs ⁽⁸⁾	0.62/0.32	0.72/0.37	ns, Min
T _{RDCK_DI} /T _{RCKD_DI}	DIN inputs ⁽⁹⁾	1.11/0.34	1.28/0.39	ns, Min
T _{RDCK_DI_ECC} /T _{RCKD_DI_ECC}	DIN inputs with block RAM ECC in standard mode ⁽⁹⁾	0.59/0.34	0.68/0.39	ns, Min
	DIN inputs with block RAM ECC encode only ⁽⁹⁾	0.85/0.34	0.97/0.39	ns, Min
	DIN inputs with FIFO ECC in standard mode ⁽⁹⁾	1.02/0.34	1.17/0.39	ns, Min
T _{RCCK_CLK} /T _{RCKC_CLK}	Inject single/double bit error in ECC mode	1.20/0.29	1.38/0.33	ns, Min
T _{RCCK_RDEN} /T _{RCKC_RDEN}	Block RAM Enable (EN) input	0.41/0.30	0.47/0.34	ns, Min
T _{RCCK_REGCE} /T _{RCKC_REGCE}	CE input of output register	0.22/0.31	0.25/0.35	ns, Min
T _{RCCK_RSTREG} /T _{RCKC_RSTREG}	Synchronous RSTREG input	0.28/0.26	0.32/0.29	ns, Min
T _{RCCK_RSTRAM} /T _{RCKC_RSTRAM}	Synchronous RSTRAM input	0.41/0.27	0.47/0.31	ns, Min
T _{RCCK_WE} /T _{RCKC_WE}	Write Enable (WE) input (block RAM only)	0.52/0.35	0.60/0.40	ns, Min
T _{RCCK_WREN} /T _{RCKC_WREN}	WREN FIFO inputs	0.55/0.30	0.64/0.34	ns, Min
T _{RCCK_RDEN} /T _{RCKC_RDEN}	RDEN FIFO inputs	0.55/0.30	0.63/0.34	ns, Min
Reset Delays				
T _{RCO_FLAGS}	Reset RST to FIFO Flags/Pointers ⁽¹⁰⁾	1.10	1.27	ns, Max
T _{RCCK_RSTREG} /T _{RCKC_RSTREG}	FIFO reset timing ⁽¹¹⁾	0.28/0.26	0.32/0.29	ns, Min

Table 51: DSP48E1 Switching Characteristics (Cont'd)

Symbol	Description	Speed Grade		Units
		-2	-1	
Combinatorial Delays from Input Pins to Cascading Output Pins				
T _{DSPDO_{A; B}_{ACOUT; BCOUT}}	{A, B} input to {ACOUT, BCOUT} output	0.65	0.75	ns
T _{DSPDO_{A, B}_{PCOUT, CARRYCASCOUT, MULTSIGNOUT}_MULT}	{A, B} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output using multiplier	5.24	6.03	ns
T _{DSPDO_D_{PCOUT, CARRYCASCOUT, MULTSIGNOUT}_MULT}	D input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output using multiplier	4.94	5.68	ns
T _{DSPDO_{A, B}_{PCOUT, CARRYCASCOUT, MULTSIGNOUT}}	{A, B} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output not using multiplier	2.19	2.52	ns
T _{DSPDO_{C, CARRYIN}_{PCOUT, CARRYCASCOUT, MULTSIGNOUT}}	{C, CARRYIN} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output	1.95	2.25	ns
Combinatorial Delays from Cascading Input Pins to All Output Pins				
T _{DSPDO_{ACIN, BCIN}_{P, CARRYOUT}_MULT}	{ACIN, BCIN} input to {P, CARRYOUT} output using multiplier	4.97	5.72	ns
T _{DSPDO_{ACIN, BCIN}_{P, CARRYOUT}}	{ACIN, BCIN} input to {P, CARRYOUT} output not using multiplier	1.92	2.21	ns
T _{DSPDO_{ACIN; BCIN}_{ACOUT; BCOUT}}	{ACIN, BCIN} input to {ACOUT, BCOUT} output	0.49	0.57	ns
T _{DSPDO_{ACIN, BCIN}_{PCOUT, CARRYCASCOUT, MULTSIGNOUT}_MULT}	{ACIN, BCIN} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output using multiplier	5.10	5.86	ns
T _{DSPDO_{ACIN, BCIN}_{PCOUT, CARRYCASCOUT, MULTSIGNOUT}}	{ACIN, BCIN} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output not using multiplier	2.05	2.35	ns
T _{DSPDO_{PCIN, CARRYCASCIN, MULTSIGNIN}_{P, CARRYOUT}}	{PCIN, CARRYCASCIN, MULTSIGNIN} input to {P, CARRYOUT} output	1.60	1.83	ns
T _{DSPDO_{PCIN, CARRYCASCIN, MULTSIGNIN}_{PCOUT, CARRYCASCOUT, MULTSIGNOUT}}	{PCIN, CARRYCASCIN, MULTSIGNIN} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output	1.72	1.98	ns
Clock to Outs from Output Register Clock to Output Pins				
T _{DSPCKO_{P, CARRYOUT}_PREG}	CLK (PREG) to {P, CARRYOUT} output	0.50	0.57	ns
T _{DSPCKO_{PCOUT, CARRYCASCOUT, MULTSIGNOUT}_PREG}	CLK (PREG) to {CARRYCASCOUT, PCOUT, MULTSIGNOUT} output	0.50	0.66	ns
Clock to Outs from Pipeline Register Clock to Output Pins				
T _{DSPCKO_{P, CARRYOUT}_MREG}	CLK (MREG) to {P, CARRYOUT} output	2.30	2.65	ns
T _{DSPCKO_{PCOUT, CARRYCASCOUT, MULTSIGNOUT}_MREG}	CLK (MREG) to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output	2.43	2.79	ns
T _{DSPCKO_{P, CARRYOUT}_ADREG_MULT}	CLK (ADREG) to {P, CARRYOUT} output	3.72	4.72	ns
T _{DSPCKO_{PCOUT, CARRYCASCOUT, MULTSIGNOUT}_ADREG_MULT}	CLK (ADREG) to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output	3.84	4.42	ns
Clock to Outs from Input Register Clock to Output Pins				
T _{DSPCKO_{P, CARRYOUT}_{AREG, BREG}_MULT}	CLK (AREG, BREG) to {P, CARRYOUT} output using multiplier	5.36	6.16	ns
T _{DSPCKO_{P, CARRYOUT}_{AREG, BREG}}	CLK (AREG, BREG) to {P, CARRYOUT} output not using multiplier	2.27	2.61	ns
T _{DSPCKO_{P, CARRYOUT}_CREG}	CLK (CREG) to {P, CARRYOUT} output	2.27	2.61	ns
T _{DSPCKO_{P, CARRYOUT}_DREG_MULT}	CLK (DREG) to {P, CARRYOUT} output	5.25	6.04	ns

Table 57: MMCM Specification (Cont'd)

Symbol	Description	Speed Grade		Units
		-2	-1	
$T_{STATPHAOFFSET}$	Static Phase Offset of the MMCM Outputs ⁽³⁾	0.12	0.12	ns
$T_{OUTJITTER}$	MMCM Output Jitter ⁽⁴⁾	Note 1		
$T_{OUTDUTY}$	MMCM Output Clock Duty Cycle Precision ⁽⁵⁾	0.20	0.20	ns
$T_{LOCKMAX}$	MMCM Maximum Lock Time	100	100	μs
F_{OUTMAX}	MMCM Maximum Output Frequency	700	700	MHz
F_{OUTMIN}	MMCM Minimum Output Frequency ⁽⁶⁾⁽⁷⁾	4.69	4.69	MHz
$T_{EXTFDVAR}$	External Clock Feedback Variation	< 20% of clock input period or 1 ns Max		
$RST_{MINPULSE}$	Minimum Reset Pulse Width	1.5	1.5	ns
F_{PFDMAX}	Maximum Frequency at the Phase Frequency Detector with Bandwidth Set to High or Optimized ⁽⁸⁾	450	450	MHz
	Maximum Frequency at the Phase Frequency Detector with Bandwidth Set to Low	300	300	MHz
F_{PFDMIN}	Minimum Frequency at the Phase Frequency Detector with Bandwidth Set to High or Optimized	135	135	MHz
	Minimum Frequency at the Phase Frequency Detector with Bandwidth Set to Low	10.00	10.00	MHz
$T_{FBDELAY}$	Maximum Delay in the Feedback Path	3 ns Max or one CLKIN cycle		
$T_{MMCMCKD_PSEN}/$ $T_{MMCMCKD_PSEN}$	Setup and Hold of Phase Shift Enable	1.04/0.00	1.04/0.00	ns
$T_{MMCMCKD_PSINCDEC}/$ $T_{MMCMCKD_PSINCDEC}$	Setup and Hold of Phase Shift Increment/Decrement	1.04/0.00	1.04/0.00	ns
$T_{MMCMCKO_PSDONE}$	Phase Shift Clock-to-Out of PSDONE	0.38	0.38	ns

Notes:

1. When $DIVCLK_DIVIDE = 3$ or 4 , F_{INMAX} is 315 MHz.
2. The MMCM does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
3. The static offset is measured between any MMCM outputs with identical phase.
4. Values for this parameter are available in the Architecture Wizard.
5. Includes global clock buffer.
6. Calculated as $F_{VCO}/128$ assuming output duty cycle is 50%.
7. When $CASCADE4_OUT = TRUE$, F_{OUTMIN} is 0.036 MHz.
8. In ISE software 12.3 (or earlier versions supporting the Virtex-6 family), the phase frequency detector Optimized bandwidth setting is equivalent to the High bandwidth setting. Starting with ISE software 12.4, the Optimized bandwidth setting is automatically adjusted to Low when the software can determine that the phase frequency detector input is less than 135 MHz.

Virtex-6 CXT Device Pin-to-Pin Output Parameter Guidelines

All devices are 100% functionally tested. The representative values for typical pin locations and normal clock loading are listed in Table 58. Values are expressed in nanoseconds unless otherwise noted.

Table 58: Global Clock Input to Output Delay Without MMCM

Symbol	Description	Device	Speed Grade		Units
			-2	-1	
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, <i>without</i> MMCM.					
T _{ICKOF}	Global Clock input and OUTFF <i>without</i> MMCM	XC6VCX75T	5.88	5.88	ns
		XC6VCX130T	6.00	6.00	ns
		XC6VCX195T	6.13	6.13	ns
		XC6VCX240T	6.13	6.13	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

Table 59: Global Clock Input to Output Delay With MMCM

Symbol	Description	Device	Speed Grade		Units
			-2	-1	
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, <i>with</i> MMCM.					
T _{ICKOFMMCMGC}	Global Clock Input and OUTFF <i>with</i> MMCM	XC6VCX75T	2.77	2.77	ns
		XC6VCX130T	2.78	2.78	ns
		XC6VCX195T	2.78	2.78	ns
		XC6VCX240T	2.79	2.79	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. MMCM output jitter is already included in the timing calculation.

Table 60: Clock-Capable Clock Input to Output Delay With MMCM

Symbol	Description	Device	Speed Grade		Units
			-2	-1	
LVCMOS25 Clock-capable Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, <i>with</i> MMCM.					
T _{ICKOFMMCMCC}	Clock-capable Clock Input and OUTFF <i>with</i> MMCM	XC6VCX75T	2.63	2.63	ns
		XC6VCX130T	2.65	2.65	ns
		XC6VCX195T	2.65	2.65	ns
		XC6VCX240T	2.65	2.65	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. MMCM output jitter is already included in the timing calculation.

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