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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	15600
Number of Logic Elements/Cells	199680
Total RAM Bits	12681216
Number of I/O	600
Number of Gates	-
Voltage - Supply	0.95V ~ 1.05V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1156-BBGA, FCBGA
Supplier Device Package	1156-FCBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc6vcx195t-1ffg1156i

FF484 Package Placement Diagrams

Figure 2 and Figure 3 show the placement diagrams for the GTX transceivers in the FF484 package.

Note: Unbonded locations in the FF484 package are:

- CX75T: X0Y8, X0Y9, X0Y10, X0Y11
- CX130T: X0Y0, X0Y1, X0Y2, X0Y3, and X0Y12, X0Y13, X0Y14, X0Y15

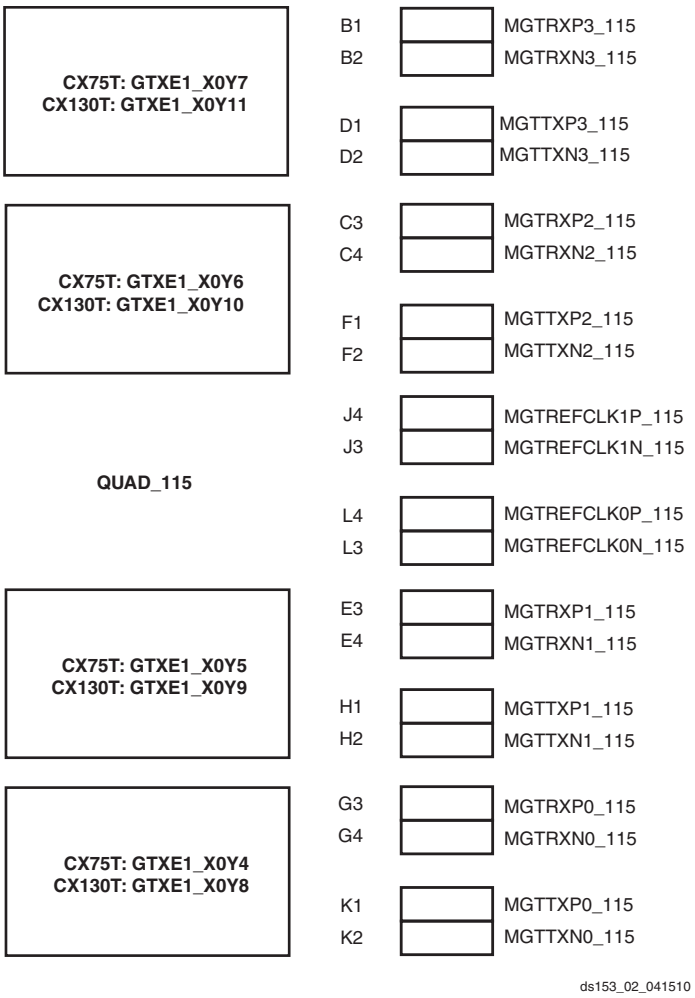

Figure 2: **Placement Diagram for the FF484 Package (1 of 2)**

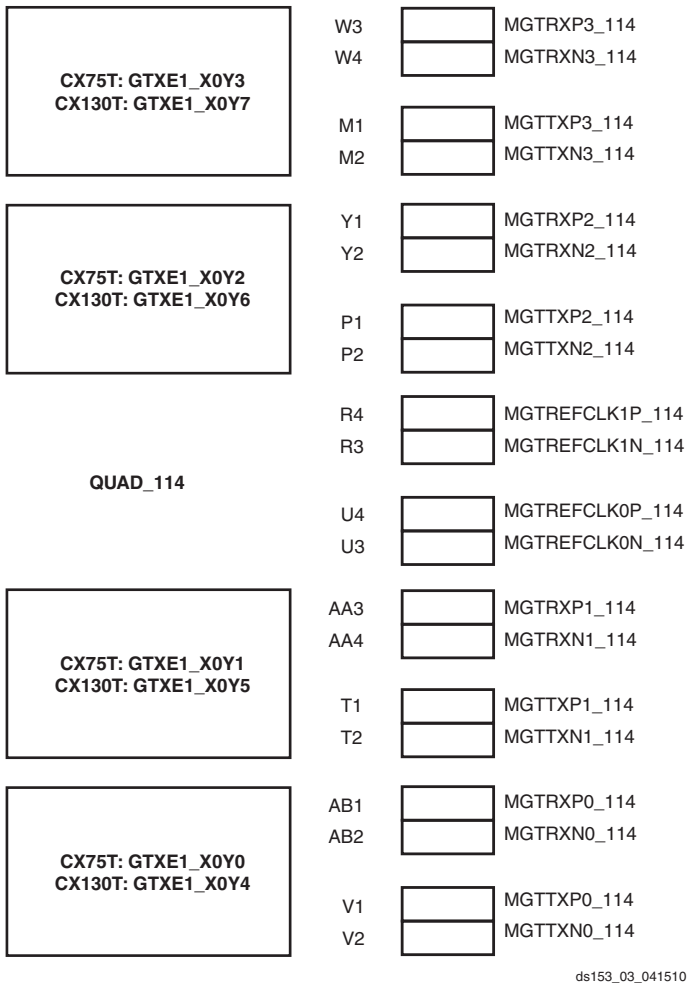

Figure 3: **Placement Diagram for the FF484 Package (2 of 2)**

FF784 Package Placement Diagrams

Figure 4 through Figure 6 show the placement diagrams for the GTX transceivers in the FF784 package.

Note: Unbonded locations in the FF784 package are:

- CX130T: X0Y0, X0Y1, X0Y2, X0Y3
- CX195T: X0Y0, X0Y1, X0Y2, X0Y3
- CX240T: X0Y0, X0Y1, X0Y2, X0Y3

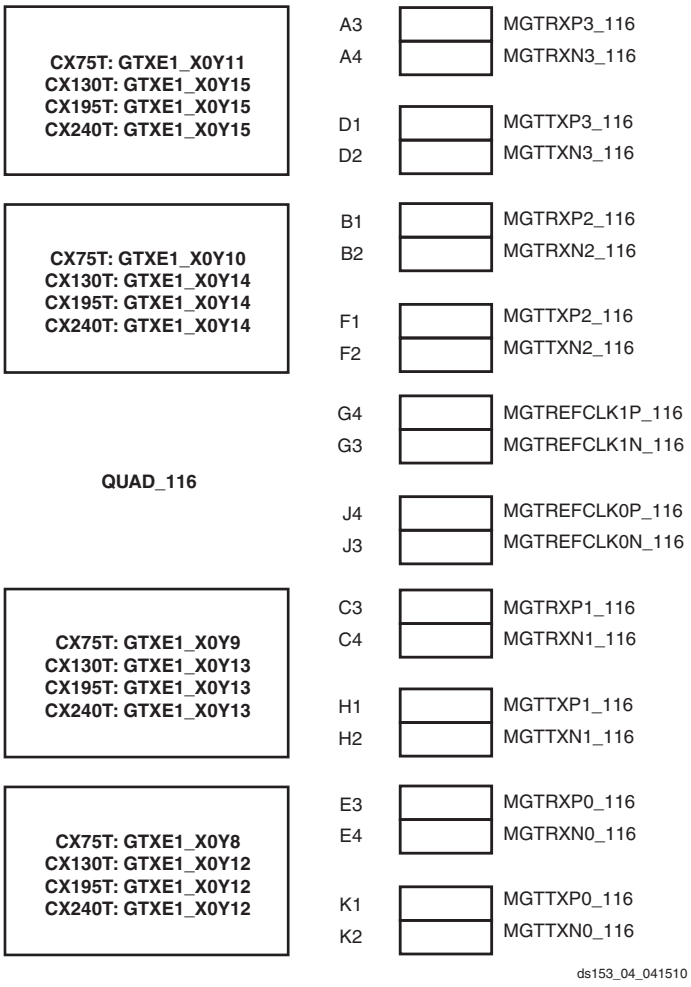

Figure 4: **Placement Diagram for the FF784 Package (1 of 3)**

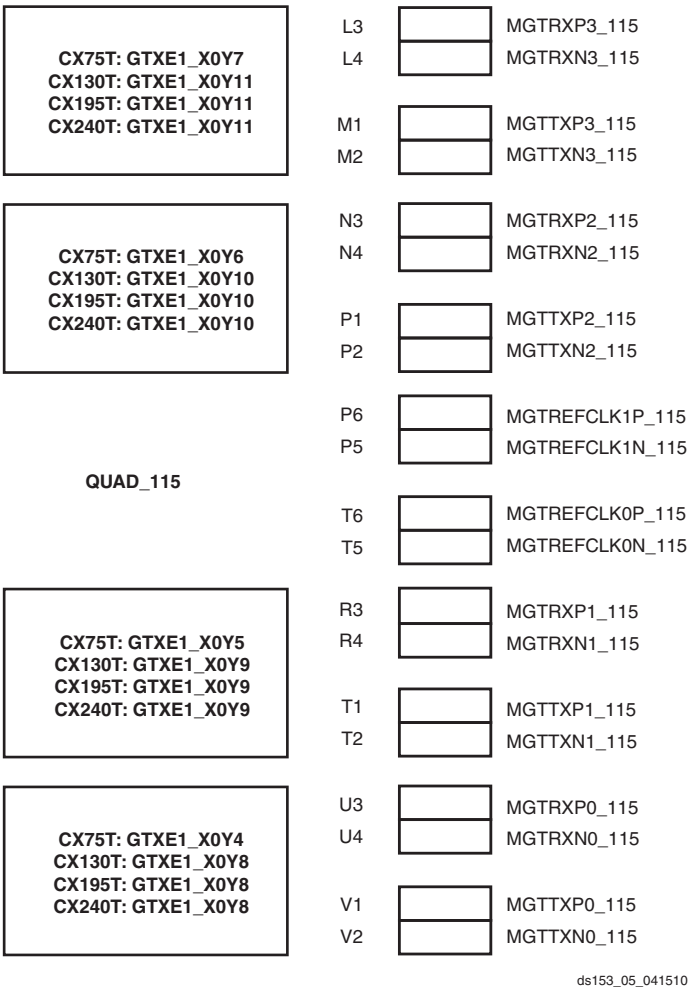

Figure 5: **Placement Diagram for the FF784 Package (2 of 3)**

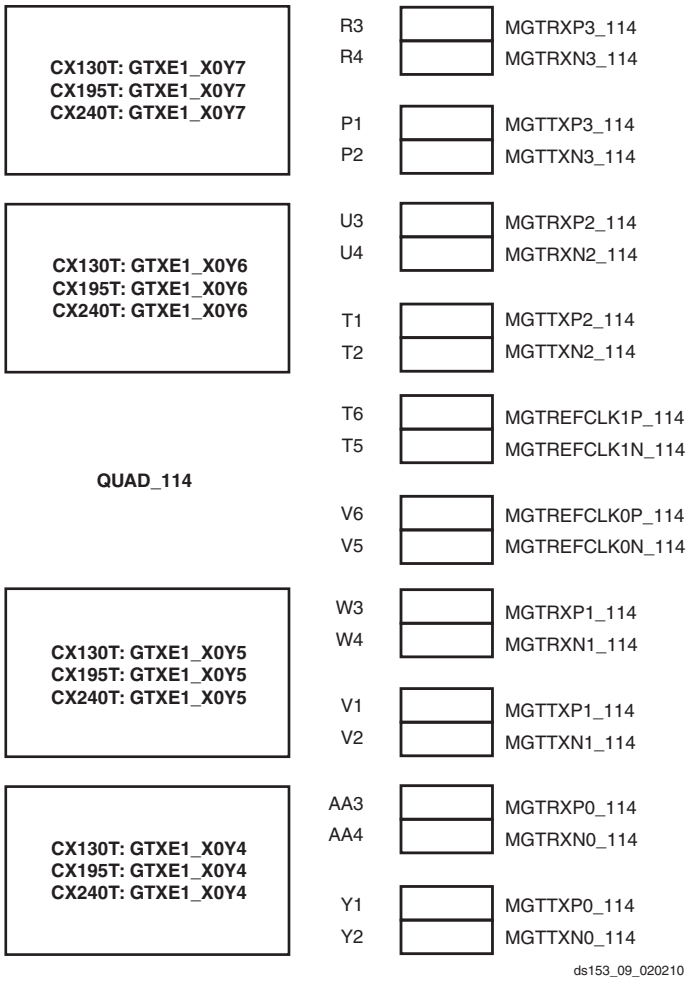

Figure 9: **Placement Diagram for the FF1156 Package (3 of 4)**

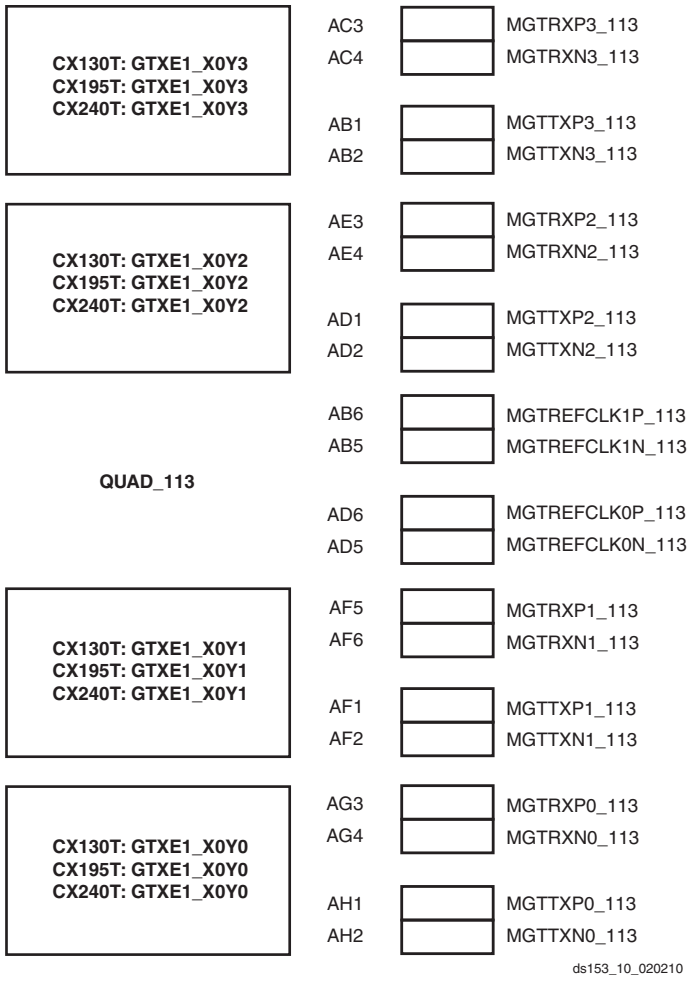

Figure 10: **Placement Diagram for the FF1156 Package (4 of 4)**

Virtex-6 CXT FPGA Electrical Characteristics Introduction

Virtex-6 CXT FPGAs are available in -2 and -1 speed grades, with -2 having the highest performance. Virtex-6 CXT FPGA DC and AC characteristics are specified for both commercial and industrial grades. Except the operating temperature range or unless otherwise noted, all the DC and AC electrical parameters are the same for a particular speed grade (that is, the timing characteristics of a -1 speed grade industrial device are the same as for a -1 speed grade commercial device). However, only selected speed grades and/or devices might be available in the industrial range.

All supply voltage and junction temperature specifications are representative of worst-case conditions. The parameters included are common to popular designs and typical applications.

All specifications are subject to change without notice.

Virtex-6 CXT FPGA DC Characteristics

Table 9: **Absolute Maximum Ratings(1)**

Symbol	Description		Units
V_{CCINT}	Internal supply voltage relative to GND	–0.5 to 1.1	V
V_{CCAUX}	Auxiliary supply voltage relative to GND	–0.5 to 3.0	V
V_{CCO}	Output drivers supply voltage relative to GND	–0.5 to 3.0	V
V_{BATT}	Key memory battery backup supply	–0.5 to 3.0	V
V_{FS}	External voltage supply for eFUSE programming(2)	–0.5 to 3.0	V
V_{REF}	Input reference voltage	–0.5 to 3.0	V
V_{IN}(3)	2.5V or below I/O input voltage relative to GND(4) (user and dedicated I/Os)	–0.5 to V_{CCO} + 0.5	V
V_{TS}	Voltage applied to 3-state 2.5V or below output(4) (user and dedicated I/Os)	–0.5 to V_{CCO} + 0.5	V
T_{STG}	Storage temperature (ambient)	–65 to 150	°C
T_{SOL}	Maximum soldering temperature(5)	+220	°C
T_j	Maximum junction temperature(5)	+125	°C

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
2. When not programming eFUSE, connect V_{FS} to GND.
3. 2.5V I/O absolute maximum limit applied to DC and AC signals.
4. For I/O operation, refer to the *Virtex-6 FPGA SelectIO Resources User Guide*.
5. For soldering guidelines and thermal considerations, see *Virtex-6 FPGA Packaging and Pinout Specification*.

LVPECL DC Specifications (LVPECL_25)

These values are valid when driving a 100Ω differential load only, i.e., a 100Ω resistor between the two receiver pins. The V_{OH} levels are 200 mV below standard LVPECL levels and are compatible with devices tolerant of lower common-mode ranges. Table 19 summarizes the DC output specifications of LVPECL. For more information on using LVPECL, see the *Virtex-6 FPGA SelectIO Resources User Guide*.

Table 19: **LVPECL DC Specifications**

Symbol	DC Parameter	Min	Typ	Max	Units
V_{OH}	Output High Voltage	V_{CC} – 1.025	1.545	V_{CC} – 0.88	V
V_{OL}	Output Low Voltage	V_{CC} – 1.81	0.795	V_{CC} – 1.62	V
V_{ICM}	Input Common-Mode Voltage	0.6	–	2.2	V
V_{IDIFF}	Differential Input Voltage(1)(2)	0.100	–	1.5	V

Notes:

1. Recommended input maximum voltage not to exceed V_{CCAUX} + 0.2V.
2. Recommended input minimum voltage not to go below –0.5V.

eFUSE Read Endurance

Table 20 lists the maximum number of read cycle operations expected. For more information, see the *Virtex-6 FPGA Configuration User Guide*.

Table 20: **eFUSE Read Endurance**

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
DNA_CYCLES	Number of DNA_PORT READ operations or JTAG ISC_DNA read command operations. Unaffected by SHIFT operations.	30,000,000				Read Cycles
AES_CYCLES	Number of JTAG FUSE_KEY or FUSE_CNTL read command operations. Unaffected by SHIFT operations.	30,000,000				Read Cycles

GTX Transceiver Specifications

GTX Transceiver DC Characteristics

Table 21: **Absolute Maximum Ratings for GTX Transceivers(1)**

Symbol	Description	Min	Max	Units
MGTAVCC	Analog supply voltage for the GTX transmitter and receiver circuits relative to GND	–0.5	1.1	V
MGTAVTT	Analog supply voltage for the GTX transmitter and receiver termination circuits relative to GND	–0.5	1.32	V
MGTAVTTRCAL	Analog supply voltage for the resistor calibration circuit of the GTX transceiver column	–0.5	1.32	V
V_{IN}	Receiver (RXP/RXN) and Transmitter (TXP/TXN) absolute input voltage	–0.5	1.32	V
$V_{MGTREFCLK}$	Reference clock absolute input voltage	–0.5	1.32	V

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.

Table 22: **Recommended Operating Conditions for GTX Transceivers(1)(2)**

Symbol	Description	Min	Typ	Max	Units
MGTAVCC	Analog supply voltage for the GTX transmitter and receiver circuits relative to GND	0.95	1.0	1.06	V
MGTAVTT	Analog supply voltage for the GTX transmitter and receiver termination circuits relative to GND	1.14	1.2	1.26	V
MGTAVTTRCAL	Analog supply voltage for the resistor calibration circuit of the GTX transceiver column	1.14	1.2	1.26	V

Notes:

1. Each voltage listed requires the filter circuit described in *Virtex-6 FPGA GTX Transceivers User Guide*.
2. Voltages are specified for the temperature range of T_j = –40°C to +100°C.

Table 23: **GTX Transceiver Supply Current (per Lane) (1)(2)**

Symbol	Description	Typ	Max	Units
$I_{MGTAVTT}$	MGTAVTT supply current for one GTX transceiver	55.9	Note 2	mA
$I_{MGTAVCC}$	MGTAVCC supply current for one GTX transceiver	56.1		mA
$MGTR_{REF}$	Precision reference resistor for internal calibration termination	100.0 ± 1% tolerance		Ω

Notes:

1. Typical values are specified at nominal voltage, 25°C, with a 3.125 Gb/s line rate.
2. Values for currents other than the values specified in this table can be obtained by using the XPOWER Estimator (XPE) or XPOWER Analyzer (XPA) tools.

Table 24: **GTX Transceiver Quiescent Supply Current (per Lane)(1)(2)(3)**

Symbol	Description	Typ(4)	Max	Units
$I_{MGTAVTTQ}$	Quiescent MGTAVTT supply current for one GTX transceiver	0.9	Note 2	mA
$I_{MGTAVCCQ}$	Quiescent MGTAVCC supply current for one GTX transceiver	3.5		mA

Notes:

1. Device powered and unconfigured.
2. Currents for conditions other than values specified in this table can be obtained by using the XPOWER Estimator (XPE) or XPOWER Analyzer (XPA) tools.
3. GTX transceiver quiescent supply current for an entire device can be calculated by multiplying the values in this table by the number of available GTX transceivers.
4. Typical values are specified at nominal voltage, 25°C.

Table 30: **GTX Transceiver User Clock Switching Characteristics(1)**

Symbol	Description	Conditions	Speed Grade		Units
			-2	-1	
F_{TXOUT}	TXOUTCLK maximum frequency	Internal 20-bit data path	187.5	187.5	MHz
		Internal 16-bit data path	234.38	234.38	MHz
F_{RXREC}	RXRECCLK maximum frequency	Internal 20-bit data path	187.5	187.5	MHz
		Internal 16-bit data path	234.38	234.38	MHz
T_{RX}	RXUSRCLK maximum frequency		234.38	234.38	MHz
T_{RX2}	RXUSRCLK2 maximum frequency	1 byte interface	376	312.5	MHz
		2 byte interface	234.38	234.38	MHz
		4 byte interface	117.19	117.19	MHz
T_{TX}	TXUSRCLK maximum frequency		234.38	234.38	MHz
T_{TX2}	TXUSRCLK2 maximum frequency	1 byte interface	376	312.5	MHz
		2 byte interface	234.38	234.38	MHz
		4 byte interface	117.19	117.19	MHz

Notes:

1. Clocking must be implemented as described in *Virtex-6 FPGA GTX Transceivers User Guide*.

Table 31: **GTX Transceiver Transmitter Switching Characteristics**

Symbol	Description	Condition	Min	Typ	Max	Units
F_{GTXTX}	Serial data rate range		0.480	–	F_{GTXMAX}	Gb/s
T_{RTX}	TX Rise time	20%–80%	–	120	–	ps
T_{FTX}	TX Fall time	80%–20%	–	120	–	ps
T_{LLSKEW}	TX lane-to-lane skew(1)		–	–	350	ps
$V_{TXOOBVDPP}$	Electrical idle amplitude		–	–	15	mV
$T_{TXOOBTRANSITION}$	Electrical idle transition time		–	–	75	ns
$T_{J3.75}$	Total Jitter(2)(3)	3.75 Gb/s	–	–	0.34	UI
$D_{J3.75}$	Deterministic Jitter(2)(3)		–	–	0.16	UI
$T_{J3.125}$	Total Jitter(2)(3)	3.125 Gb/s	–	–	0.2	UI
$D_{J3.125}$	Deterministic Jitter(2)(3)		–	–	0.1	UI
$T_{J3.125L}$	Total Jitter(2)(3)	3.125 Gb/s(4)	–	–	0.35	UI
$D_{J3.125L}$	Deterministic Jitter(2)(3)		–	–	0.16	UI
$T_{J2.5}$	Total Jitter(2)(3)	2.5 Gb/s(5)	–	–	0.20	UI
$D_{J2.5}$	Deterministic Jitter(2)(3)		–	–	0.08	UI
$T_{J1.25}$	Total Jitter(2)(3)	1.25 Gb/s(6)	–	–	0.15	UI
$D_{J1.25}$	Deterministic Jitter(2)(3)		–	–	0.06	UI
T_{J600}	Total Jitter(2)(3)	600 Mb/s	–	–	0.1	UI
D_{J600}	Deterministic Jitter(2)(3)		–	–	0.03	UI

Table 38: **IOB Switching Characteristics *(Cont'd)***

I/O Standard	T_{IOPI}		T_{IOOP}		T_{IOTP}		Units
	Speed Grade		Speed Grade		Speed Grade		
	-2	-1	-2	-1	-2	-1	
LVPECL_25	1.09	1.09	1.65	1.65	1.65	1.65	ns
HSTL_I_12	1.06	1.06	1.78	1.78	1.78	1.78	ns
HSTL_I_DCI	1.06	1.06	1.66	1.66	1.66	1.66	ns
HSTL_II_DCI	1.06	1.06	1.68	1.68	1.68	1.68	ns
HSTL_II_T_DCI	1.06	1.06	1.66	1.66	1.66	1.66	ns
HSTL_III_DCI	1.06	1.06	1.62	1.62	1.62	1.62	ns
HSTL_I_DCI_18	1.06	1.06	1.68	1.68	1.68	1.68	ns
HSTL_II_DCI_18	1.06	1.06	1.62	1.62	1.62	1.62	ns
HSTL_II _T_DCI_18	1.06	1.06	1.68	1.68	1.68	1.68	ns
HSTL_III_DCI_18	1.06	1.06	1.69	1.69	1.69	1.69	ns
DIFF_HSTL_I_18	1.09	1.09	1.75	1.75	1.75	1.75	ns
DIFF_HSTL_I_DCI_18	1.09	1.09	1.68	1.68	1.68	1.68	ns
DIFF_HSTL_I	1.09	1.09	1.73	1.73	1.73	1.73	ns
DIFF_HSTL_I_DCI	1.09	1.09	1.66	1.66	1.66	1.66	ns
DIFF_HSTL_II_18	1.09	1.09	1.81	1.81	1.81	1.81	ns
DIFF_HSTL_II_DCI_18	1.09	1.09	1.62	1.62	1.62	1.62	ns
DIFF_HSTL_II _T_DCI_18	1.09	1.09	1.68	1.68	1.68	1.68	ns
DIFF_HSTL_II	1.09	1.09	1.74	1.74	1.74	1.74	ns
DIFF_HSTL_II_DCI	1.09	1.09	1.68	1.68	1.68	1.68	ns
SSTL2_I_DCI	1.06	1.06	1.70	1.70	1.70	1.70	ns
SSTL2_II_DCI	1.06	1.06	1.67	1.67	1.67	1.67	ns
SSTL2_II_T_DCI	1.06	1.06	1.70	1.70	1.70	1.70	ns
SSTL18_I	1.06	1.06	1.75	1.75	1.75	1.75	ns
SSTL18_II	1.06	1.06	1.67	1.67	1.67	1.67	ns
SSTL18_I_DCI	1.06	1.06	1.67	1.67	1.67	1.67	ns
SSTL18_II_DCI	1.06	1.06	1.63	1.63	1.63	1.63	ns
SSTL18_II_T_DCI	1.06	1.06	1.67	1.67	1.67	1.67	ns
SSTL15_T_DCI	1.06	1.06	1.68	1.68	1.68	1.68	ns
SSTL15_DCI	1.06	1.06	1.68	1.68	1.68	1.68	ns
DIFF_SSTL2_I	1.09	1.09	1.77	1.77	1.77	1.77	ns
DIFF_SSTL2_I_DCI	1.09	1.09	1.70	1.70	1.70	1.70	ns
DIFF_SSTL2_II	1.09	1.09	1.72	1.72	1.72	1.72	ns
DIFF_SSTL2_II_DCI	1.09	1.09	1.67	1.67	1.67	1.67	ns
DIFF_SSTL2_II_T_DCI	1.09	1.09	1.70	1.70	1.70	1.70	ns
DIFF_SSTL18_I	1.09	1.09	1.75	1.75	1.75	1.75	ns
DIFF_SSTL18_I_DCI	1.09	1.09	1.67	1.67	1.67	1.67	ns
DIFF_SSTL18_II	1.09	1.09	1.67	1.67	1.67	1.67	ns
DIFF_SSTL18_II_DCI	1.09	1.09	1.63	1.63	1.63	1.63	ns

Table 43: **OLOGIC Switching Characteristics**

Symbol	Description	Speed Grade		Units
		-2	-1	
Setup/Hold				
T_{ODCK}/T_{OCKD}	D1/D2 pins Setup/Hold with respect to CLK	0.54/–0.11	0.54/–0.11	ns
T_{OOCECK}/T_{OCKOCE}	OCE pin Setup/Hold with respect to CLK	0.22/–0.05	0.22/–0.05	ns
T_{OSRCK}/T_{OCKSR}	SR pin Setup/Hold with respect to CLK	0.71/–0.29	0.71/–0.29	ns
T_{OTCK}/T_{OCKT}	T1/T2 pins Setup/Hold with respect to CLK	0.56/–0.10	0.56/–0.10	ns
T_{OTCECK}/T_{OCKTCE}	TCE pin Setup/Hold with respect to CLK	0.21/–0.05	0.21/–0.05	ns
Combinatorial				
T_{DOQ}	D1 to OQ out or T1 to TQ out	1.01	1.01	ns
Sequential Delays				
T_{OCKQ}	CLK to OQ/TQ out	0.71	0.71	ns
T_{RQ}	SR pin to OQ/TQ out	1.05	1.05	ns
T_{GSRQ}	Global Set/Reset to Q outputs	10.51	10.51	ns
Set/Reset				
T_{RPW}	Minimum Pulse Width, SR inputs	1.20	1.20	ns, Min

Input Serializer/Deserializer Switching Characteristics

Table 44: **ISERDES Switching Characteristics**

Symbol	Description	Speed Grade		Units
		-2	-1	
Setup/Hold for Control Lines				
$T_{ISCCK\_BITSLIP}/T_{ISCKC\_BITSLIP}$	BITSLIP pin Setup/Hold with respect to CLKDIV	0.09/0.17	0.09/0.17	ns
$T_{ISCCK\_CE}/T_{ISCKC\_CE}$ (2)	CE pin Setup/Hold with respect to CLK (for CE1)	0.27/0.04	0.27/0.04	ns
$T_{ISCCK\_CE2}/T_{ISCKC\_CE2}$ (2)	CE pin Setup/Hold with respect to CLKDIV (for CE2)	–0.06/0.31	–0.06/0.31	ns
Setup/Hold for Data Lines				
T_{ISDCK_D}/T_{ISCKD_D}	D pin Setup/Hold with respect to CLK	0.09/0.11	0.09/0.11	ns
$T_{ISDCK\_DDLY}/T_{ISCKD\_DDLY}$	DDLY pin Setup/Hold with respect to CLK (using IODELAY) (1)	0.14/0.07	0.14/0.07	ns
$T_{ISDCK\_D\_DDR}/T_{ISCKD\_D\_DDR}$	D pin Setup/Hold with respect to CLK at DDR mode	0.09/0.11	0.09/0.11	ns
$T_{ISDCK\_DDLY\_DDR}$ $T_{ISCKD\_DDLY\_DDR}$	D pin Setup/Hold with respect to CLK at DDR mode (using IODELAY) (1)	0.14/0.07	0.14/0.07	ns
Sequential Delays				
T_{ISCKO_Q}	CLKDIV to out at Q pin	0.75	0.75	ns
Propagation Delays				
T_{ISDO_DO}	D input to DO output pin	0.25	0.25	ns

Notes:

1. Recorded at 0 tap value.
2. T_{ISCCK_CE2} and T_{ISCKC_CE2} are reported as $T_{ISCCK\_CE}/T_{ISCKC\_CE}$ in a TRACE report.

Input/Output Delay Switching Characteristics

Table 46: **Input/Output Delay Switching Characteristics**

Symbol	Description	Speed Grade		Units
		-2	-1	
IDELAYCTRL				
T_{DLYCCO_RDY}	Reset to Ready for IDELAYCTRL	3	3	µs
$F_{IDELAYCTRL\_REF}$	REFCLK frequency	200	200	MHz
IDELAYCTRL_REF_PRECISION	REFCLK precision	±10	±10	MHz
$T_{IDELAYCTRL\_RPW}$	Minimum Reset pulse width	50	50	ns
IODELAY				
$T_{IDELAYRESOLUTION}$	IODELAY Chain Delay Resolution	1/(32 x 2 x F_{REF})		ps
$T_{IDELAYPAT\_JIT}$	Pattern dependent period jitter in delay chain for clock pattern.(1)	0	0	ps per tap
	Pattern dependent period jitter in delay chain for random data pattern.(2)	±5	±5	ps per tap
	Pattern dependent period jitter in delay chain for random data pattern.(3)	±9	±9	ps per tap
$T_{IODELAY\_CLK\_MAX}$	Maximum frequency of CLK input to IODELAY	300	300	MHz
T_{IODCCK_CE} / T_{IODCKC_CE}	CE pin Setup/Hold with respect to CK	0.65/–0.09	0.65/–0.09	ns
T_{IODCK_INC}/ T_{IODCKC_INC}	INC pin Setup/Hold with respect to CK	0.31/–0.00	0.31/–0.00	ns
T_{IODCCK_RST}/ T_{IODCKC_RST}	RST pin Setup/Hold with respect to CK	0.69/–0.08	0.69/–0.08	ns
T_{IODDO_T}	TSCONTROL delay to MUXE/MUXF switching and through IODELAY	Note 4	Note 4	ps
$T_{IODDO\_IDATAIN}$	Propagation delay through IODELAY	Note 4	Note 4	ps
$T_{IODDO\_ODATAIN}$	Propagation delay through IODELAY	Note 4	Note 4	ps

Notes:

1. When HIGH_PERFORMANCE mode is set to TRUE or FALSE.
2. When HIGH_PERFORMANCE mode is set to TRUE
3. When HIGH_PERFORMANCE mode is set to FALSE.
4. Delay depends on IODELAY tap setting. See the TRACE report for actual values.

CLB Switching Characteristics

Table 47: **CLB Switching Characteristics**

Symbol	Description	Speed Grade		Units
		-2	-1	
Combinatorial Delays				
T_{ILO}	An – Dn LUT address to A	0.08	0.08	ns, Max
	An – Dn LUT address to AMUX/CMUX	0.23	0.25	ns, Max
	An – Dn LUT address to BMUX_A	0.37	0.41	ns, Max
T_{ITO}	An – Dn inputs to A – D Q outputs	0.79	0.91	ns, Max
T_{AXA}	AX inputs to AMUX output	0.42	0.48	ns, Max
T_{AXB}	AX inputs to BMUX output	0.47	0.53	ns, Max
T_{AXC}	AX inputs to CMUX output	0.52	0.60	ns, Max
T_{AXD}	AX inputs to DMUX output	0.55	0.63	ns, Max

CLB Distributed RAM Switching Characteristics (SLICEM Only)

Table 48: **CLB Distributed RAM Switching Characteristics**

Symbol	Description	Speed Grade		Units
		-2	-1	
Sequential Delays				
T_{SHCKO}	Clock to A – B outputs	1.36	1.56	ns, Max
T_{SHCKO_1}	Clock to AMUX – BMUX outputs	1.71	1.96	ns, Max
Setup and Hold Times Before/After Clock CLK				
T_{DS}/T_{DH}	A – D inputs to CLK	0.88/0.22	1.01/0.26	ns, Min
T_{AS}/T_{AH}	Address An inputs to clock	0.27/0.70	0.31/0.80	ns, Min
T_{WS}/T_{WH}	WE input to clock	0.40/–0.01	0.46/0.00	ns, Min
T_{CECK}/T_{CKCE}	CE input to CLK	0.41/–0.02	0.48/–0.01	ns, Min
Clock CLK				
T_{MPW}	Minimum pulse width	1.00	1.15	ns, Min
T_{MCP}	Minimum clock period	2.00	2.30	ns, Min

Notes:

1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values cannot be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.
2. T_{SHCKO} also represents the CLK to XMUX output. Refer to the TRACE report for the CLK to XMUX path.

CLB Shift Register Switching Characteristics (SLICEM Only)

Table 49: **CLB Shift Register Switching Characteristics**

Symbol	Description	Speed Grade		Units
		-2	-1	
Sequential Delays				
T_{REG}	Clock to A – D outputs	1.58	1.82	ns, Max
T_{REG_MUX}	Clock to AMUX – DMUX output	1.93	2.22	ns, Max
T_{REG_M31}	Clock to DMUX output via M31 output	1.55	1.78	ns, Max
Setup and Hold Times Before/After Clock CLK				
T_{WS}/T_{WH}	WE input	0.09/–0.01	0.10/0.00	ns, Min
T_{CECK}/T_{CKCE}	CE input to CLK	0.10/–0.02	0.11/–0.01	ns, Min
T_{DS}/T_{DH}	A – D inputs to CLK	0.94/0.24	1.08/0.28	ns, Min
Clock CLK				
T_{MPW}	Minimum pulse width	0.85	0.98	ns, Min

Notes:

1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values cannot be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

Block RAM and FIFO Switching Characteristics

Table 50: **Block RAM and FIFO Switching Characteristics**

Symbol	Description	Speed Grade		Units
		-2	-1	
Block RAM and FIFO Clock-to-Out Delays				
T_{RCKO_DO} and $T_{RCKO\_DO\_REG}$[1]	Clock CLK to DOUT output (without output register)[2][3]	2.08	2.39	ns, Max
	Clock CLK to DOUT output (with output register)[4][5]	0.75	0.86	ns, Max
$T_{RCKO\_DO\_ECC}$ and $T_{RCKO\_DO\_ECC\_REG}$	Clock CLK to DOUT output with ECC (without output register)[2][3]	3.30	3.79	ns, Max
	Clock CLK to DOUT output with ECC (with output register)[4][5]	0.86	0.98	ns, Max
T_{RCKO_CASC} and $T_{RCKO\_CASC\_REG}$	Clock CLK to DOUT output with Cascade (without output register)[2]	3.18	3.65	ns, Max
	Clock CLK to DOUT output with Cascade (with output register)[4]	1.58	1.81	ns, Max
T_{RCKO_FLAGS}	Clock CLK to FIFO flags outputs[6]	0.91	1.05	ns, Max
$T_{RCKO\_POINTERS}$	Clock CLK to FIFO pointers outputs[7]	1.09	1.25	ns, Max
$T_{RCKO\_RDCOUNT}$	Clock CLK to FIFO Read Counter	1.09	1.25	ns, Max
$T_{RCKO\_WRCOUNT}$	Clock CLK to FIFO Write Counter	1.09	1.25	ns, Max
$T_{RCKO\_SDBIT\_ECC}$ and $T_{RCKO\_SDBIT\_ECC\_REG}$	Clock CLK to BITERR (with output register)	0.76	0.87	ns, Max
	Clock CLK to BITERR (without output register)	2.84	3.26	ns, Max
$T_{RCKO\_PARITY\_ECC}$	Clock CLK to ECCPARITY in ECC encode only mode	1.06	1.21	ns, Max
$T_{RCKO\_RDADDR\_ECC}$ and $T_{RCKO\_RDADDR\_ECC\_REG}$	Clock CLK to RDADDR output with ECC (without output register)	0.90	1.03	ns, Max
	Clock CLK to RDADDR output with ECC (with output register)	0.92	1.06	ns, Max
Setup and Hold Times Before/After Clock CLK				
$T_{RCCK\_ADDR}/T_{RCKC\_ADDR}$	ADDR inputs[8]	0.62/0.32	0.72/0.37	ns, Min
T_{RDCK_DI}/T_{RCKD_DI}	DIN inputs[9]	1.11/0.34	1.28/0.39	ns, Min
$T_{RDCK\_DI\_ECC}/T_{RCKD\_DI\_ECC}$	DIN inputs with block RAM ECC in standard mode[9]	0.59/0.34	0.68/0.39	ns, Min
	DIN inputs with block RAM ECC encode only[9]	0.85/0.34	0.97/0.39	ns, Min
	DIN inputs with FIFO ECC in standard mode[9]	1.02/0.34	1.17/0.39	ns, Min
$T_{RCCK\_CLK}/T_{RCKC\_CLK}$	Inject single/double bit error in ECC mode	1.20/0.29	1.38/0.33	ns, Min
$T_{RCCK\_RDEN}/T_{RCKC\_RDEN}$	Block RAM Enable (EN) input	0.41/0.30	0.47/0.34	ns, Min
$T_{RCCK\_REGCE}/T_{RCKC\_REGCE}$	CE input of output register	0.22/0.31	0.25/0.35	ns, Min
$T_{RCCK\_RSTREG}/T_{RCKC\_RSTREG}$	Synchronous RSTREG input	0.28/0.26	0.32/0.29	ns, Min
$T_{RCCK\_RSTRAM}/T_{RCKC\_RSTRAM}$	Synchronous RSTRAM input	0.41/0.27	0.47/0.31	ns, Min
T_{RCCK_WE}/T_{RCKC_WE}	Write Enable (WE) input (block RAM only)	0.52/0.35	0.60/0.40	ns, Min
$T_{RCCK\_WREN}/T_{RCKC\_WREN}$	WREN FIFO inputs	0.55/0.30	0.64/0.34	ns, Min
$T_{RCCK\_RDEN}/T_{RCKC\_RDEN}$	RDEN FIFO inputs	0.55/0.30	0.63/0.34	ns, Min
Reset Delays				
T_{RCO_FLAGS}	Reset RST to FIFO Flags/Pointers[10]	1.10	1.27	ns, Max
$T_{RCCK\_RSTREG}/T_{RCKC\_RSTREG}$	FIFO reset timing[11]	0.28/0.26	0.32/0.29	ns, Min

Table 50: **Block RAM and FIFO Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade		Units
		-2	-1	
Maximum Frequency				
F_{MAX}	Block RAM (Write First and No Change modes)	400	350	MHz
	Block RAM (Read First mode)	400	347	MHz
	Block RAM (SDP mode)(12)	400	347	MHz
$F_{MAX\_CASCADE}$	Block RAM Cascade (Write First and No Change modes)	400	347	MHz
	Block RAM Cascade (Read First mode)	350	304	MHz
F_{MAX_FIFO}	FIFO in all modes	400	350	MHz
F_{MAX_ECC}	Block RAM and FIFO in ECC configuration	325	282	MHz

Notes:

1. TRACE will report all of these parameters as T_{RCKO_DO}.
2. T_{RCKO_DOR} includes T_{RCKO_DOW}, T_{RCKO_DOPR}, and T_{RCKO_DOPW} as well as the B port equivalent timing parameters.
3. These parameters also apply to synchronous FIFO with DO_REG = 0.
4. T_{RCKO_DO} includes T_{RCKO_DOP} as well as the B port equivalent timing parameters.
5. These parameters also apply to multirate (asynchronous) and synchronous FIFO with DO_REG = 1.
6. T_{RCKO_FLAGS} includes the following parameters: T_{RCKO_AEMPTY}, T_{RCKO_AFULL}, T_{RCKO_EMPTY}, T_{RCKO_FULL}, T_{RCKO_RDERR}, T_{RCKO_WRERR}.
7. $T_{RCKO\_POINTERS}$ includes both $T_{RCKO\_RDCOUNT}$ and $T_{RCKO\_WRCOUNT}$.
8. The ADDR setup and hold must be met when EN is asserted (even when WE is deasserted). Otherwise, block RAM data corruption is possible.
9. T_{RCKO_DI} includes both A and B inputs as well as the parity inputs of A and B.
10. T_{RCO_FLAGS} includes the following flags: AEMPTY, AFULL, EMPTY, FULL, RDERR, WRERR, RDCOUNT, and WRCOUNT.
11. The FIFO reset must be asserted for at least three positive clock edges.
12. When using ISE software v12.4 or later, if the RDARRDR_COLLISION_HWCONFIG attribute is set to PERFORMANCE or the block RAM is in single-port operation, then the faster F_{MAX} for WRITE_FIRST/NO_CHANGE modes apply.

DSP48E1 Switching Characteristics

Table 51: **DSP48E1 Switching Characteristics**

Symbol	Description	Speed Grade		Units
		-2	-1	
Setup and Hold Times of Data/Control Pins to the Input Register Clock				
$T_{DSPDCK\_\{A, ACIN; B, BCIN\}\_\{AREG; BREG\}}$/ $T_{DSPCKD\_\{A, ACIN; B, BCIN\}\_\{AREG; BREG\}}$	{A, ACIN, B, BCIN} input to {A, B} register CLK	0.35/0.34	0.41/0.39	ns
$T_{DSPDCK\_C\_CREG}$/$T_{DSPCKD\_C\_CREG}$	C input to C register CLK	0.22/0.24	0.26/0.27	ns
$T_{DSPDCK\_D\_DREG}$/$T_{DSPCKD\_D\_DREG}$	D input to D register CLK	0.15/0.39	0.17/0.44	ns
Setup and Hold Times of Data Pins to the Pipeline Register Clock				
$T_{DSPDCK\_\{A, ACIN, B, BCIN\}\_PREG\_MULT}$/ $T_{DSPCKD\_\{A, ACIN, B, BCIN\}\_PREG\_MULT}$	{A, ACIN, B, BCIN} input to M register CLK	3.21/0.02	3.69/0.02	ns
$T_{DSPDCK\_\{A, D\}\_ADREG}$/ $T_{DSPCKD–\{A, D\}\_ADREG}$	{A, D} input to AD register CLK	1.69/0.13	1.94/0.15	ns
Setup and Hold Times of Data/Control Pins to the Output Register Clock				
$T_{DSPDCK\_\{A, ACIN, B, BCIN\}\_PREG\_MULT}$/ $T_{DSPCKD\_\{A, ACIN, B, BCIN\}\_PREG\_MULT}$	{A, ACIN, B, BCIN} input to P register CLK using multiplier	5.20/–0.19	5.97/–0.22	ns
$T_{DSPDCK\_D\_DREG\_MULT}$/ $T_{DSPCKD\_D\_DREG\_MULT}$	D input to P register CLK	4.90/–0.65	5.63/–0.75	ns
$T_{DSPDCK\_\{A, ACIN, B, BCIN\}\_PREG}$/ $T_{DSPCKD\_\{A, ACIN, B, BCIN\}\_PREG}$	{A, ACIN, B, BCIN} input to P register CLK not using multiplier	2.15/–0.19	2.47/–0.22	ns
$T_{DSPDCK\_C\_PREG}$/ $T_{DSPCKD\_C\_PREG}$	C input to P register CLK	1.91/–0.14	2.19/–0.17	ns
$T_{DSPDCK\_\{PCIN, CARRYCASCIN, MULTSIGNIN\}\_PREG}$/ $T_{DSPCKD\_\{PCIN, CARRYCASCIN, MULTSIGNIN\}\_PREG}$	{PCIN, CARRYCASCIN, MULTSIGNIN} input to P register CLK	1.67/–0.04	1.92/–0.05	ns
Setup and Hold Times of the CE Pins				
$T_{DSPDCK\_\{CEA; CEB\}\_\{AREG; BREG\}}$/ $T_{DSPCKD\_\{CEA; CEB\}\_\{AREG; BREG\}}$	{CEA; CEB} input to {A; B} register CLK	0.22/0.25	0.25/0.29	ns
$T_{DSPDCK\_CEC\_CREG}$/ $T_{DSPCKD\_CEC\_CREG}$	CEC input to C register CLK	0.24/0.23	0.28/0.27	ns
$T_{DSPDCK\_CED\_DREG}$/ $T_{DSPCKD\_CED\_DREG}$	CED input to D register CLK	0.31/0.14	0.35/0.16	ns
$T_{DSPDCK\_CEM\_MREG}$/ $T_{DSPCKD\_CEM\_MREG}$	CEM input to M register CLK	0.26/0.25	0.30/0.28	ns
$T_{DSPDCK\_CEP\_PREG}$/ $T_{DSPCKD\_CEP\_PREG}$	CEP input to P register CLK	0.46/0.03	0.53/0.03	ns
Setup and Hold Times of the RST Pins				
$T_{DSPDCK\_\{RSTA; RSTB\}\_\{AREG; BREG\}}$/ $T_{DSPCKD\_\{RSTA; RSTB\}\_\{AREG; BREG\}}$	{RSTA, RSTB} input to {A, B} register CLK	0.38/0.22	0.43/0.25	ns
$T_{DSPDCK\_RSTC\_CREG}$/ $T_{DSPCKD\_RSTC\_CREG}$	RSTC input to C register CLK	0.23/0.09	0.27/0.11	ns
$T_{DSPDCK\_RSTD\_DREG}$/ $T_{DSPCKD\_RSTD\_DREG}$	RSTD input to D register CLK	0.38/0.19	0.44/0.21	ns
$T_{DSPDCK\_RSTM\_MREG}$/ $T_{DSPCKD\_RSTM\_MREG}$	RSTM input to M register CLK	0.26/0.30	0.30/0.35	ns
$T_{DSPDCK\_RSTP\_PREG}$/ $T_{DSPCKD\_RSTP\_PREG}$	RSTP input to P register CLK	0.33/0.05	0.41/0.06	ns
Combinatorial Delays from Input Pins to Output Pins				
$T_{DSPDO\_\{A, B\}\_\{P, CARRYOUT\}\_MULT}$	{A, B} input to {P, CARRYOUT} output using multiplier	5.08	5.84	ns
$T_{DSPDO\_D\_\{P, CARRYOUT\}\_MULT}$	D input to {P, CARRYOUT} output using multiplier	4.82	5.54	ns
$T_{DSPDO\_\{A, B\}\_\{P, CARRYOUT\}}$	{A, B} input to {P, CARRYOUT} output not using multiplier	2.07	2.38	ns
$T_{DSPDO\_\{C, CARRYIN\}\_\{P, CARRYOUT\}}$	{C, CARRYIN} input to {P, CARRYOUT} output	1.83	2.10	ns

Configuration Switching Characteristics

Table 52: **Configuration Switching Characteristics**

Symbol	Description	Speed Grade		Units
		-2	-1	
Power-up Timing Characteristics				
T_{PL} (1)	Program Latency	3	3	ms, Max
T_{POR} (1)	Power-on-Reset	15/55	15/55	ms, Min/Max
T_{ICCK}	CCLK (output) delay	400	400	ns, Min
$T_{PROGRAM}$	Program Pulse Width	250	250	ns, Min
Master/Slave Serial Mode Programming Switching (1)				
T_{DCCK}/T_{CCKD}	DIN Setup/Hold, slave mode	4.0/0.0	4.0/0.0	ns, Min
T_{DSCCK}/T_{SCCKD}	DIN Setup/Hold, master mode	4.0/0.0	4.0/0.0	ns, Min
T_{CCO}	DOUT at 2.5V	6	6	ns, Max
	DOUT at 1.8V	6	6	ns, Max
F_{MCCK}	Maximum CCLK frequency, serial modes	100	100	MHz, Max
$F_{MCCKTOL}$	Frequency Tolerance, master mode with respect to nominal CCLK	55	55	%
F_{MSCCK}	Slave mode external CCLK	100	100	MHz
SelectMAP Mode Programming Switching				
T_{SMDCCK}/T_{SMCCKD}	SelectMAP Data Setup/Hold	4.0/0.0	4.0/0.0	ns, Min
$T_{SMCSCCK}/T_{SMCCKCS}$	CSI_B Setup/Hold	4.0/0.0	4.0/0.0	ns, Min
T_{SMCCKW}/T_{SMWCCK}	RDWR_B Setup/Hold	10.0/0.0	10.0/0.0	ns, Min
$T_{SMCKCSO}$	CSO_B clock to out (330 Ω pull-up resistor required)	7	7	ns, Min
T_{SMCO}	CCLK to DATA out in readback at 2.5V	8	8	ns, Max
	CCLK to DATA out in readback at 1.8V	8	8	ns, Max
T_{SMCKBY}	CCLK to BUSY out in readback at 2.5V	6	6	ns, Max
	CCLK to BUSY out in readback at 1.8V	6	6	ns, Max
F_{SMCCK}	Maximum Frequency with respect to nominal CCLK	100	100	MHz, Max
F_{RBCCK}	Maximum Readback Frequency with respect to nominal CCLK	100	100	MHz, Max
$F_{MCCKTOL}$	Frequency Tolerance with respect to nominal CCLK	55	55	%
Boundary-Scan Port Timing Specifications				
T_{TAPTCK}/T_{TCKTAP}	TMS and TDI Setup time before TCK/ Hold time after TCK	3.0/2.0	3.0/2.0	ns, Min
T_{TCKTDO}	TCK falling edge to TDO output valid at 2.5V	6	6	ns, Max
	TCK falling edge to TDO output valid at 1.8V	6	6	ns, Max
F_{TCK}	Maximum configuration TCK clock frequency	66	66	MHz, Max
F_{TCKB_MIN}	Minimum boundary-scan TCK clock frequency when using IEEE Std 1149.6 (AC-JTAG). Minimum operating temperature for IEEE Std 1149.6 is 0°C.	15	15	MHz, Min
F_{TCKB}	Maximum boundary-scan TCK clock frequency	66	66	MHz, Max

Table 52: **Configuration Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade		Units
		-2	-1	
BPI Master Flash Mode Programming Switching				
T_{BPICCO}(2)	ADDR[25:0], RS[1:0], FCS_B, FOE_B, FWE_B outputs valid after CCLK rising edge at 2.5V	6	6	ns
	ADDR[25:0], RS[1:0], FCS_B, FOE_B, FWE_B outputs valid after CCLK rising edge at 1.8V	6	6	ns
T_{BPIDCC}/T_{BPICCD}	Setup/Hold on D[15:0] data input pins	4.0/0.0	4.0/0.0	ns
$T_{INITADDR}$	Minimum period of initial ADDR[25:0] address cycles	3	3	CCLK cycles
SPI Master Flash Mode Programming Switching				
$T_{SPIDCC}/T_{SPIDCCD}$	DIN Setup/Hold before/after the rising CCLK edge	3.0/0.0	3.0/0.0	ns
T_{SPICCM}	MOSI clock to out at 2.5V	6	6	ns
	MOSI clock to out at 1.8V	6	6	ns
$T_{SPICCFC}$	FCS_B clock to out at 2.5V	6	6	ns
	FCS_B clock to out at 1.8V	6	6	ns
$T_{FSINIT}/T_{FSINITH}$	FS[2:0] to INIT_B rising edge Setup and Hold	2	2	µs
CCLK Output (Master Modes)				
T_{MCCKL}	Master CCLK clock Low time duty cycle	45/55	45/55	%, Min/Max
T_{MCCKH}	Master CCLK clock High time duty cycle	45/55	45/55	%, Min/Max
CCLK Input (Slave Modes)				
T_{SCCKL}	Slave CCLK clock minimum Low time	2.5	2.5	ns, Min
T_{SCCKH}	Slave CCLK clock minimum High time	2.5	2.5	ns, Min
Dynamic Reconfiguration Port (DRP) for MMCM Before and After DCLK				
F_{DCK}	Maximum frequency for DCLK	200	200	MHz
$T_{MMCMDCK\_DADDR}/T_{MMCMCKD\_DADDR}$	DADDR Setup/Hold	1.63/0.00	1.63/0.00	ns
$T_{MMCMDCK\_DI}/T_{MMCMCKD\_DI}$	DI Setup/Hold	1.63/0.00	1.63/0.00	ns
$T_{MMCMDCK\_DEN}/T_{MMCMCKD\_DEN}$	DEN Setup/Hold time	1.63/0.00	1.63/0.00	ns
$T_{MMCMDCK\_DWE}/T_{MMCMCKD\_DWE}$	DWE Setup/Hold time	1.63/0.00	1.63/0.00	ns
$T_{MMCMCKO\_DO}$	CLK to out of DO(3)	3.64	3.64	ns
$T_{MMCMCKO\_DRDY}$	CLK to out of DRDY	0.38	0.38	ns

Notes:

1. To support longer delays in configuration, use the design solutions described in *Virtex-6 FPGA Configuration Guide*.
2. Only during configuration, the last edge is determined by a weak pull-up/pull-down resistor in the I/O.
3. DO will hold until next DRP operation.

Virtex-6 CXT Device Pin-to-Pin Output Parameter Guidelines

All devices are 100% functionally tested. The representative values for typical pin locations and normal clock loading are listed in Table 58. Values are expressed in nanoseconds unless otherwise noted.

Table 58: **Global Clock Input to Output Delay Without MMCM**

Symbol	Description	Device	Speed Grade		Units
			-2	-1	
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, *without* MMCM.					
T_{ICKOF}	Global Clock input and OUTFF *without* MMCM	XC6VCX75T	5.88	5.88	ns
		XC6VCX130T	6.00	6.00	ns
		XC6VCX195T	6.13	6.13	ns
		XC6VCX240T	6.13	6.13	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

Table 59: **Global Clock Input to Output Delay With MMCM**

Symbol	Description	Device	Speed Grade		Units
			-2	-1	
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, *with* MMCM.					
$T_{ICKOFMMCMGC}$	Global Clock Input and OUTFF *with* MMCM	XC6VCX75T	2.77	2.77	ns
		XC6VCX130T	2.78	2.78	ns
		XC6VCX195T	2.78	2.78	ns
		XC6VCX240T	2.79	2.79	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. MMCM output jitter is already included in the timing calculation.

Table 60: **Clock-Capable Clock Input to Output Delay With MMCM**

Symbol	Description	Device	Speed Grade		Units
			-2	-1	
LVCMOS25 Clock-capable Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, *with* MMCM.					
$T_{ICKOFMMCMCC}$	Clock-capable Clock Input and OUTFF *with* MMCM	XC6VCX75T	2.63	2.63	ns
		XC6VCX130T	2.65	2.65	ns
		XC6VCX195T	2.65	2.65	ns
		XC6VCX240T	2.65	2.65	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. MMCM output jitter is already included in the timing calculation.

Table 66: **Sample Window**

Symbol	Description	Device	Speed Grade		Units
			-2	-1	
T_{SAMP}	Sampling Error at Receiver Pins(1)	All	610	610	ps
T_{SAMP_BUFIO}	Sampling Error at Receiver Pins using BUFIO(2)	All	400	400	ps

Notes:

1. This parameter indicates the total sampling error of Virtex-6 CXT FPGA DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the MMCM to capture the DDR input registers' edges of operation. These measurements include:
   - CLK0 MMCM jitter
   - MMCM accuracy (phase offset)
   - MMCM phase shift resolution

   These measurements do not include package or clock tree skew.
2. This parameter indicates the total sampling error of Virtex-6 CXT FPGA DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the BUFIO clock network and IODELAY to capture the DDR input registers' edges of operation. These measurements do not include package or clock tree skew.

Table 67: **Pin-to-Pin Setup/Hold and Clock-to-Out**

Symbol	Description	Speed Grade		Units
		-2	-1	
Data Input Setup and Hold Times Relative to a Forwarded Clock Input Pin Using BUFIO				
T_{PSCS}/T_{PHCS}	Setup/Hold of I/O clock	–0.33/1.31	–0.33/1.31	ns
Pin-to-Pin Clock-to-Out Using BUFIO				
$T_{ICKOFCS}$	Clock-to-Out of I/O clock	5.19	5.19	ns

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
07/08/09	1.0	Initial Xilinx release.
02/05/10	1.1	Removed Figure 11: Placement Diagram for the FF1156 Package (5 of 5) from page 11 as there are only 16 GTX transceivers in the FF1156 package. Corrected the placement diagrams in Figure 2 through Figure 10.

Date	Version	Description of Revisions
06/08/10	1.2	Revised GTX Transceivers in CXT Devices, page 5. Added V_{FS} and revised the V_{IN} and V_{TS} values in Table 9, page 11. Added V_{FS} and note 6 to Table 10. Revised description of C_{IN} in Table 11, including adding note 3. Updated Table 13 including adding note 2. Removed DIFF SSTL15 and added values to SSTL15 in Table 15. Updated Table 16 through Table 19. Added eFUSE Read Endurance section. Updated entire GTX Transceivers in CXT Devices section. Changed specifications of PCI Express in Table 34. In Table 35, removed RLDRAM II and revised and added values to other interface performance specifications. Updated speed specification to v1.04 with appropriate changes to Table 36. Revised the IOB switching characteristics in Table 38. Updated values in Table 39 and note 4 in Table 41. ILOGIC (Table 42), OLOGIC (Table 43), ISERDES (Table 44), and OSERDES (Table 45) switching characteristics changes. Revised $T_{IODELAY\_CLK\_MAX}$ and $T_{IDELAYPAT\_JIT}$ in Table 46. Revised CLB switching characteristics and added T_{SHCKO} to Table 47and revised CLB switching characteristics in Table 48 and Table 49. In Table 50, removed $T_{RCKO\_RDCOUNT}$ and $T_{RCKO\_WRCOUNT}$, removed $T_{RCKO\_PARITY\_ECC}$: Clock CLK to ECCPARITY in standard ECC mode, revised $T_{RDCK\_DI\_ECC}$/$T_{RCKD\_DI\_ECC}$, $T_{RCKO\_POINTERS}$, and revised F_{MAX} and $F_{MAX\_CASCADE}$ switching characteristics. Multiple changes to configuration specifications in Table 52. Revised switching characteristics and global clock tree (BUFG) F_{MAX} in Table 53. Revised switching characteristics and I/O clock tree (BUFIO) F_{MAX} in Table 54. Added note 1 to Table 55. Revised the F_{MAX} horizontal clock tree (BUFH) in Table 56. Multiple changes to MMCM specifications in Table 57 including F_{INMAX} and F_{OUTMAX}. Updated switching characteristics in Table 58 through Table 63. Removed T_{DCD_BUFH} and $T_{BUFHSKEW}$ from Table 64.
06/30/10	1.3	Production release of XC6VCX130T and XC6VCX240T in Table 36 and Table 37. Updated -1 speed grade SDR values in Table 35. Updated BUFIO F_{MAX} specification in Table 54. Added Note 6 to Table 57.
07/28/10	1.4	Production release of XC6VCX75T and XC6VCX195T in Table 36 and Table 37 using ISE 12.2 software with speed file v1.06 using the *Speed File Patch*. Updated PCI compliance on page 1. Added values to Table 13. In Table 25, update $V_{CMOUTDC}$ equation to MGTAVTT – DV_{PPOUT}/4. Updated F_{MAX} in Table 53, Table 54, and Table 56. Updated F_{INMAX} and F_{OUTMAX} in Table 57. Updated values in Table 61, Table 62, and Table 63.
10/14/10	1.5	Moved data sheet to Production status on the first page. Updated speed file with ISE 12.3 software with speed file v1.08 using the *Speed File Patch.* In Table 51, updated values for $T_{DSPCKO\_\{PCOUT,}$ CARRYCASCOUT, MULTSIGNOUT}_PREG.
02/11/11	1.6	Updated Table 10 to include the industrial range specifications. Added Note 12 to Table 50. Revised T_{BPICCO} values in Table 52. Updated range description for F_{INDUTY} in Table 57 and added note 8. The following revisions are due to specification changes as described in XCN11009, *Virtex-6 FPGA: Data Sheet, User Guides, and JTAG ID Updates*. In Table 52, updated the values for T_{SMCCKW}, T_{SPIDCC}, T_{SPICCM}, and $T_{SPICCFC}$. In Table 57: MMCM Specification, added bandwidth settings to F_{PFDMIN} and added note 1.

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