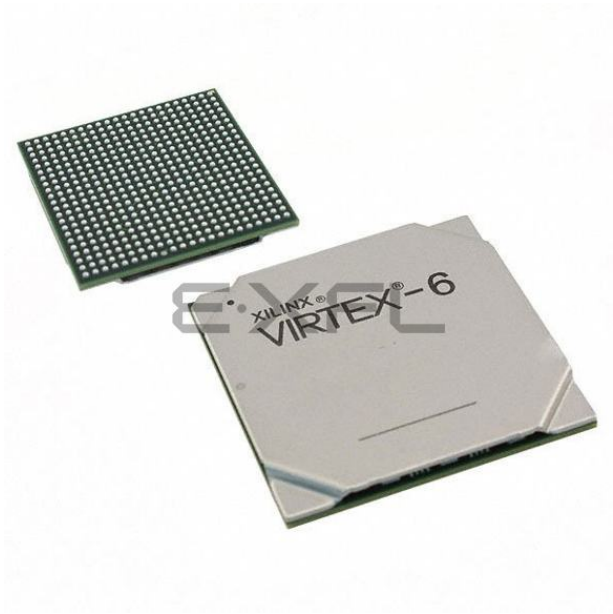
AMD Xilinx - XC6VCX195T-2FF784I Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

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The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	15600
Number of Logic Elements/Cells	199680
Total RAM Bits	12681216
Number of I/O	400
Number of Gates	-
Voltage - Supply	0.95V ~ 1.05V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	784-BBGA, FCBGA
Supplier Device Package	784-FCBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc6vcx195t-2ff784i

Virtex-6 CXT FPGA Documentation

In addition to the data sheet information found herein, complete and up-to-date documentation of the Virtex-6 family of FPGAs is available on the Xilinx website and available for download:

Virtex-6 FPGA Configuration Guide **(UG360)**

This all-encompassing configuration guide includes chapters on configuration interfaces (serial and parallel), multi-bitstream management, bitstream encryption, boundary-scan and JTAG configuration, and reconfiguration techniques.

Virtex-6 FPGA SelectIO Resources User Guide **(UG361)**

This guide describes the SelectIO™ resources available in all the Virtex-6 CXT devices.

Virtex-6 FPGA Clocking Resources User Guide **(UG362)**

This guide describes the clocking resources available in all the Virtex-6 CXT devices, including the MMCM and clock buffers.

Virtex-6 FPGA Memory Resources User Guide **(UG363)**

This guide describes the Virtex-6 CXT device block RAM and FIFO capabilities.

Virtex-6 FPGA CLB User Guide **(UG364)**

This guide describes the capabilities of the configurable logic blocks (CLB) available in all Virtex-6 CXT devices.

Virtex-6 FPGA DSP48E1 Slice User Guide **(UG369)**

This guide describes the architecture of the DSP48E1 slice in Virtex-6 CXT FPGAs and provides configuration examples.

Virtex-6 FPGA GTX Transceivers User Guide **(UG366)**

This guide describes the GTX transceivers available in all the Virtex-6 CXT FPGAs.

Virtex-6 FPGA Tri-Mode Ethernet MAC User Guide **(UG368)**

This guide describes the dedicated tri-mode Ethernet media access controller (TEMAC) available in all the Virtex-6 CXT FPGAs.

Virtex-6 FPGA Data Sheet: DC and Switching Characteristics **(DS152)**

Reference this data sheet when considering device migration to the Virtex-6 LXT and SXT families. It contains the DC and Switching Characteristic specifications specifically for the Virtex-6 LXT and SXT families.

Virtex-6 FPGA Packaging and Pinout Specifications **(UG365)**

These specifications includes the tables for device/package combinations and maximum I/Os, pin definitions, pinout tables, pinout diagrams, mechanical drawings, and thermal specifications of the Virtex-6 LXT and SXT families. Reference these specifications when considering device migration to the Virtex-6 LXT and SXT families.

Configuration Bitstream Overview for CXT Devices

This section contains two tables similar to those in the *Virtex-6 FPGA Configuration Guide* only updated for the CXT family. The Virtex-6 CXT FPGA bitstream contains commands to the FPGA configuration logic as well as configuration data. Table 3 gives a typical bitstream length and Table 4 gives the specific device ID codes for the Virtex-6 CXT devices.

Table 3: **Virtex-6 CXT FPGA Bitstream Length**

Device	Total Number of Configuration Bits
XC6VCX75T	26,239,328
XC6VCX130T	43,719,776
XC6VCX195T	61,552,736
XC6VCX240T	73,859,552

Table 4: **Virtex-6 CXT FPGA Device ID Codes**

Device	ID Code (Hex)
XC6VCX75T	0x042C4093
XC6VCX130T	0x042CA093
XC6VCX195T	0x042CC093
XC6VCX240T	0x042D0093

FF484 Package Placement Diagrams

Figure 2 and Figure 3 show the placement diagrams for the GTX transceivers in the FF484 package.

Note: Unbonded locations in the FF484 package are:

- CX75T: X0Y8, X0Y9, X0Y10, X0Y11
- CX130T: X0Y0, X0Y1, X0Y2, X0Y3, and X0Y12, X0Y13, X0Y14, X0Y15

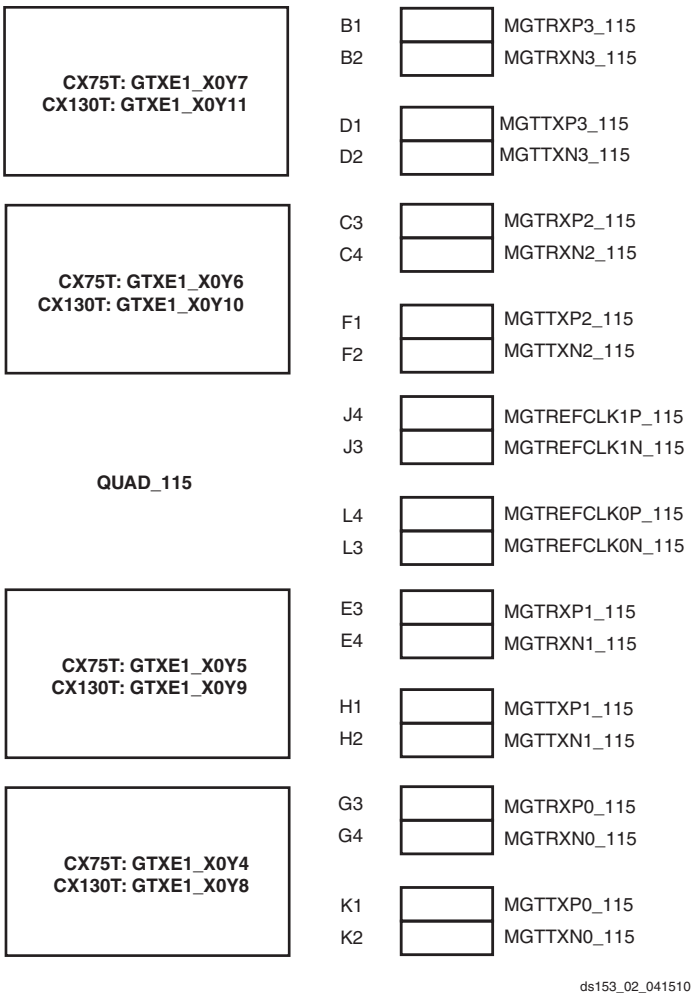

Figure 2: **Placement Diagram for the FF484 Package (1 of 2)**

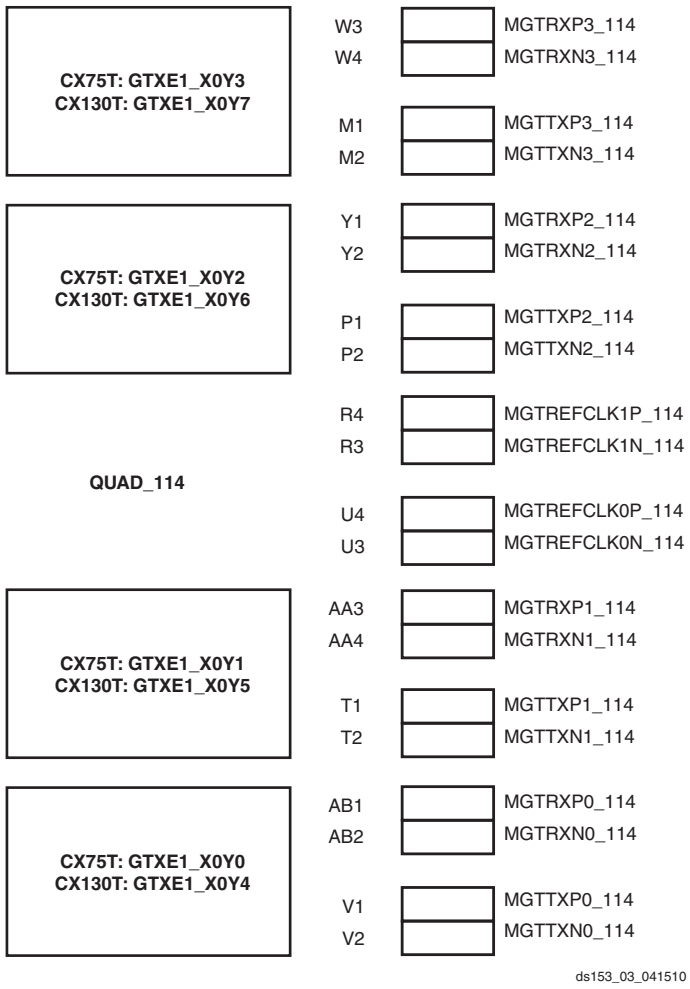

Figure 3: **Placement Diagram for the FF484 Package (2 of 2)**

FF784 Package Placement Diagrams

Figure 4 through Figure 6 show the placement diagrams for the GTX transceivers in the FF784 package.

Note: Unbonded locations in the FF784 package are:

- CX130T: X0Y0, X0Y1, X0Y2, X0Y3
- CX195T: X0Y0, X0Y1, X0Y2, X0Y3
- CX240T: X0Y0, X0Y1, X0Y2, X0Y3

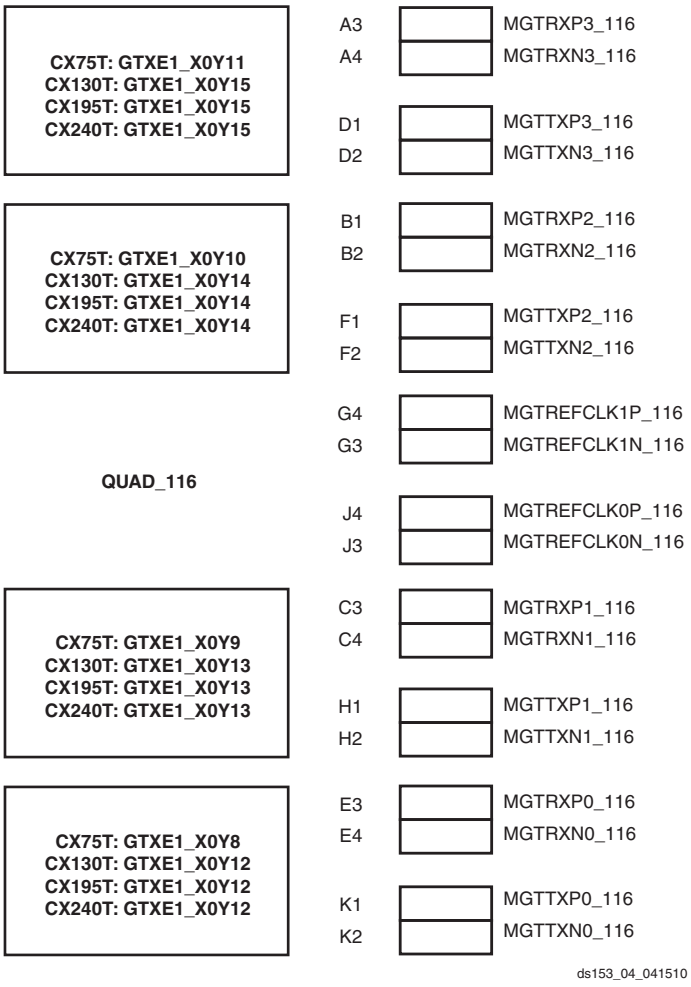

Figure 4: **Placement Diagram for the FF784 Package (1 of 3)**

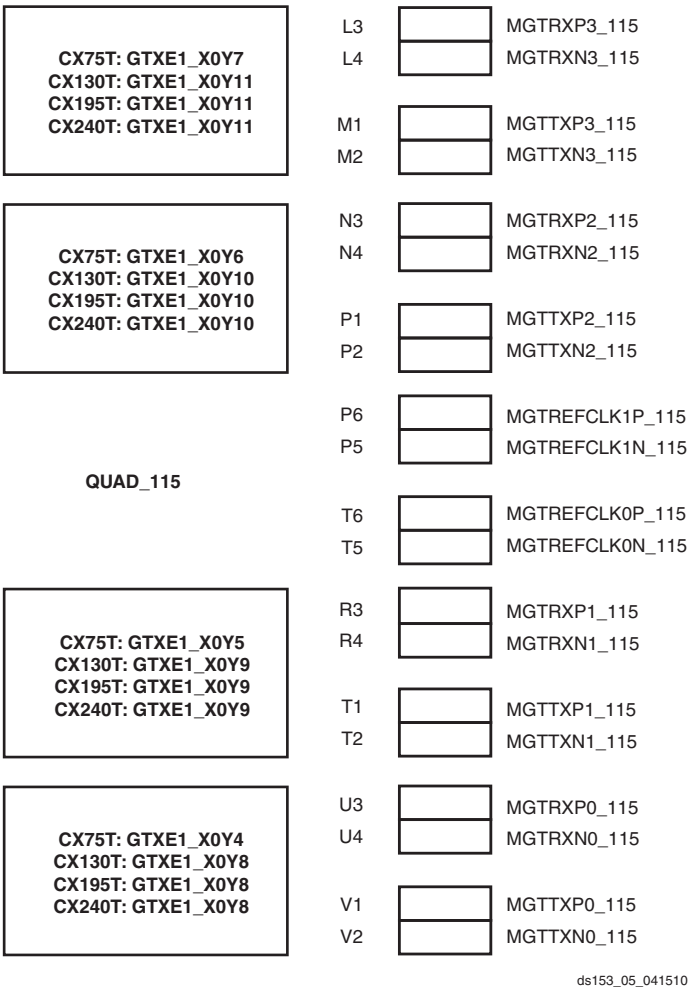

Figure 5: **Placement Diagram for the FF784 Package (2 of 3)**

Power-On Power Supply Requirements

Xilinx FPGAs require a certain amount of supply current during power-on to insure proper device initialization. The actual current consumed depends on the power-on ramp rate of the power supply.

Virtex-6 CXT devices require a power-on sequence of V_{CCINT}, V_{CCAUX}, and V_{CCO}. If the requirement can not be met, then V_{CCAUX} must always be powered prior to V_{CCO}. V_{CCAUX} and V_{CCO} can be powered by the same supply, therefore, both V_{CCAUX} and V_{CCO} are permitted to ramp simultaneously. Similarly, for the power-down sequence, V_{CCO} must be powered down prior to V_{CCAUX} or if powered by the same supply, V_{CCAUX} and V_{CCO} power-down simultaneously.

Table 13 shows the minimum current, in addition to I_{CCQ}, that are required by Virtex-6 CXT devices for proper power-on and configuration. If the current minimums shown in Table 12 and Table 13 are met, the device powers on after all three supplies have passed through their power-on reset threshold voltages. The FPGA must be configured after V_{CCINT} is applied.

Once initialized and configured, use the XPOWER tools to estimate current drain on these supplies.

Table 13: **Power-On Current for Virtex-6 CXT Devices**

Device	$I_{CCINTMIN}$	$I_{CCAUXMIN}$	I_{CCOMIN}	Units
	Typ(1)	Typ(1)	Typ(1)	
XC6VCX75T	See I_{CCINTQ} in Table 12	I_{CCAUXQ} + 10	I_{CCOQ} + 30 mA per bank	mA
XC6VCX130T	See I_{CCINTQ} in Table 12	I_{CCAUXQ} + 10	I_{CCOQ} + 30 mA per bank	mA
XC6VCX195T	See I_{CCINTQ} in Table 12	I_{CCAUXQ} + 40	I_{CCOQ} + 30 mA per bank	mA
XC6VCX240T	See I_{CCINTQ} in Table 12	I_{CCAUXQ} + 40	I_{CCOQ} + 30 mA per bank	mA

Notes:

1. Typical values are specified at nominal voltage, 25°C.
2. Use the XPOWER™ Estimator (XPE) spreadsheet tool (download at http://www.xilinx.com/power) to calculate maximum power-on currents.

Table 14: **Power Supply Ramp Time**

Symbol	Description	Ramp Time	Units
V_{CCINT}	Internal supply voltage relative to GND	0.20 to 50.0	ms
V_{CCO}	Output drivers supply voltage relative to GND	0.20 to 50.0	ms
V_{CCAUX}	Auxiliary supply voltage relative to GND	0.20 to 50.0	ms

SelectIO™ DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

Table 15: **SelectIO DC Input and Output Levels**

I/O Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
LVCMOS25, LVDCI25	–0.3	0.7	1.7	V_{CCO} + 0.3	0.4	V_{CCO} – 0.4	Note(3)	Note(3)
LVCMOS18, LVDCI18	–0.3	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.3	0.45	V_{CCO} – 0.45	Note(4)	Note(4)
LVCMOS15, LVDCI15	–0.3	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.3	25% V_{CCO}	75% V_{CCO}	Note(4)	Note(4)
LVCMOS12	–0.3	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.3	25% V_{CCO}	75% V_{CCO}	Note(5)	Note(5)
HSTL I_12	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.3	25% V_{CCO}	75% V_{CCO}	6.3	6.3
HSTL I(2)	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.3	0.4	V_{CCO} – 0.4	8	–8
HSTL II(2)	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.3	0.4	V_{CCO} – 0.4	16	–16
HSTL III(2)	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.3	0.4	V_{CCO} – 0.4	24	–8
DIFF HSTL I(2)	–0.3	50% V_{CCO} – 0.1	50% V_{CCO} + 0.1	V_{CCO} + 0.3	–	–	–	–
DIFF HSTL II(2)	–0.3	50% V_{CCO} – 0.1	50% V_{CCO} + 0.1	V_{CCO} + 0.3	–	–	–	–
SSTL2 I	–0.3	V_{REF} – 0.15	V_{REF} + 0.15	V_{CCO} + 0.3	V_{TT} – 0.61	V_{TT} + 0.61	8.1	–8.1
SSTL2 II	–0.3	V_{REF} – 0.15	V_{REF} + 0.15	V_{CCO} + 0.3	V_{TT} – 0.81	V_{TT} + 0.81	16.2	–16.2
DIFF SSTL2 I	–0.3	50% V_{CCO} – 0.15	50% V_{CCO} + 0.15	V_{CCO} + 0.3	–	–	–	–
DIFF SSTL2 II	–0.3	50% V_{CCO} – 0.15	50% V_{CCO} + 0.15	V_{CCO} + 0.3	–	–	–	–
SSTL18 I	–0.3	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.3	V_{TT} – 0.47	V_{TT} + 0.47	6.7	–6.7
SSTL18 II	–0.3	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.3	V_{TT} – 0.60	V_{TT} + 0.60	13.4	–13.4
DIFF SSTL18 I	–0.3	50% V_{CCO} – 0.125	50% V_{CCO} + 0.125	V_{CCO} + 0.3	–	–	–	–
DIFF SSTL18 II	–0.3	50% V_{CCO} – 0.125	50% V_{CCO} + 0.125	V_{CCO} + 0.3	–	–	–	–
SSTL15	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.3	V_{TT} – 0.175	V_{TT} + 0.175	14.3	14.3

Notes:

1. Tested according to relevant specifications.
2. Applies to both 1.5V and 1.8V HSTL.
3. Using drive strengths of 2, 4, 6, 8, 12, 16, or 24 mA.
4. Using drive strengths of 2, 4, 6, 8, 12, or 16 mA.
5. Supported drive strengths of 2, 4, 6, or 8 mA.
6. For detailed interface specific DC voltage levels, see the *Virtex-6 FPGA SelectIO Resources User Guide*.

LVPECL DC Specifications (LVPECL_25)

These values are valid when driving a 100Ω differential load only, i.e., a 100Ω resistor between the two receiver pins. The V_{OH} levels are 200 mV below standard LVPECL levels and are compatible with devices tolerant of lower common-mode ranges. Table 19 summarizes the DC output specifications of LVPECL. For more information on using LVPECL, see the *Virtex-6 FPGA SelectIO Resources User Guide*.

Table 19: **LVPECL DC Specifications**

Symbol	DC Parameter	Min	Typ	Max	Units
V_{OH}	Output High Voltage	V_{CC} – 1.025	1.545	V_{CC} – 0.88	V
V_{OL}	Output Low Voltage	V_{CC} – 1.81	0.795	V_{CC} – 1.62	V
V_{ICM}	Input Common-Mode Voltage	0.6	–	2.2	V
V_{IDIFF}	Differential Input Voltage(1)(2)	0.100	–	1.5	V

Notes:

1. Recommended input maximum voltage not to exceed V_{CCAUX} + 0.2V.
2. Recommended input minimum voltage not to go below –0.5V.

eFUSE Read Endurance

Table 20 lists the maximum number of read cycle operations expected. For more information, see the *Virtex-6 FPGA Configuration User Guide*.

Table 20: **eFUSE Read Endurance**

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
DNA_CYCLES	Number of DNA_PORT READ operations or JTAG ISC_DNA read command operations. Unaffected by SHIFT operations.	30,000,000				Read Cycles
AES_CYCLES	Number of JTAG FUSE_KEY or FUSE_CNTL read command operations. Unaffected by SHIFT operations.	30,000,000				Read Cycles

GTX Transceiver Specifications

GTX Transceiver DC Characteristics

Table 21: **Absolute Maximum Ratings for GTX Transceivers(1)**

Symbol	Description	Min	Max	Units
MGTAVCC	Analog supply voltage for the GTX transmitter and receiver circuits relative to GND	–0.5	1.1	V
MGTAVTT	Analog supply voltage for the GTX transmitter and receiver termination circuits relative to GND	–0.5	1.32	V
MGTAVTTRCAL	Analog supply voltage for the resistor calibration circuit of the GTX transceiver column	–0.5	1.32	V
V_{IN}	Receiver (RXP/RXN) and Transmitter (TXP/TXN) absolute input voltage	–0.5	1.32	V
$V_{MGTREFCLK}$	Reference clock absolute input voltage	–0.5	1.32	V

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.

Table 22: **Recommended Operating Conditions for GTX Transceivers(1)(2)**

Symbol	Description	Min	Typ	Max	Units
MGTAVCC	Analog supply voltage for the GTX transmitter and receiver circuits relative to GND	0.95	1.0	1.06	V
MGTAVTT	Analog supply voltage for the GTX transmitter and receiver termination circuits relative to GND	1.14	1.2	1.26	V
MGTAVTTRCAL	Analog supply voltage for the resistor calibration circuit of the GTX transceiver column	1.14	1.2	1.26	V

Notes:

1. Each voltage listed requires the filter circuit described in *Virtex-6 FPGA GTX Transceivers User Guide*.
2. Voltages are specified for the temperature range of T_j = –40°C to +100°C.

Table 23: **GTX Transceiver Supply Current (per Lane) (1)(2)**

Symbol	Description	Typ	Max	Units
$I_{MGTAVTT}$	MGTAVTT supply current for one GTX transceiver	55.9	Note 2	mA
$I_{MGTAVCC}$	MGTAVCC supply current for one GTX transceiver	56.1		mA
$MGTR_{REF}$	Precision reference resistor for internal calibration termination	100.0 ± 1% tolerance		Ω

Notes:

1. Typical values are specified at nominal voltage, 25°C, with a 3.125 Gb/s line rate.
2. Values for currents other than the values specified in this table can be obtained by using the XPOWER Estimator (XPE) or XPOWER Analyzer (XPA) tools.

Table 24: **GTX Transceiver Quiescent Supply Current (per Lane)(1)(2)(3)**

Symbol	Description	Typ(4)	Max	Units
$I_{MGTAVTTQ}$	Quiescent MGTAVTT supply current for one GTX transceiver	0.9	Note 2	mA
$I_{MGTAVCCQ}$	Quiescent MGTAVCC supply current for one GTX transceiver	3.5		mA

Notes:

1. Device powered and unconfigured.
2. Currents for conditions other than values specified in this table can be obtained by using the XPOWER Estimator (XPE) or XPOWER Analyzer (XPA) tools.
3. GTX transceiver quiescent supply current for an entire device can be calculated by multiplying the values in this table by the number of available GTX transceivers.
4. Typical values are specified at nominal voltage, 25°C.

Table 26 summarizes the DC specifications of the clock input of the GTX transceiver. Consult the *Virtex-6 FPGA GTX Transceivers User Guide* for further details.

Table 26: **GTX Transceiver Clock DC Input Level Specification**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{IDIFF}	Differential peak-to-peak input voltage		210	800	2000	mV
R_{IN}	Differential input resistance		90	100	130	Ω
C_{EXT}	Required external AC coupling capacitor		–	100	–	nF

GTX Transceiver Switching Characteristics

Consult *Virtex-6 FPGA GTX Transceivers User Guide* for further information.

Table 27: **GTX Transceiver Performance**

Symbol	Description	Speed Grade		Units
		-2	-1	
F_{GTXMAX}	Maximum GTX transceiver data rate	3.75	3.75	Gb/s
$F_{GPLLMAX}$	Maximum PLL frequency	2.5	2.5	GHz
$F_{GPLLMIN}$	Minimum PLL frequency	1.2	1.2	GHz

Table 28: **GTX Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics**

Symbol	Description	Speed Grade		Units
		-2	-1	
$F_{GTXDRPCLK}$	GTXDRPCLK maximum frequency	100	100	MHz

Table 29: **GTX Transceiver Reference Clock Switching Characteristics**

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
F_{GCLK}	Reference clock frequency range		67.5	–	375	MHz
T_{RCLK}	Reference clock rise time	20% – 80%	–	200	–	ps
T_{FCLK}	Reference clock fall time	80% – 20%	–	200	–	ps
T_{DCREF}	Reference clock duty cycle	Transceiver PLL only	45	50	55	%
T_{LOCK}	Clock recovery frequency acquisition time	Initial PLL lock	–	–	1	ms
T_{PHASE}	Clock recovery phase acquisition time	Lock to data after PLL has locked to the reference clock	–	–	200	µs

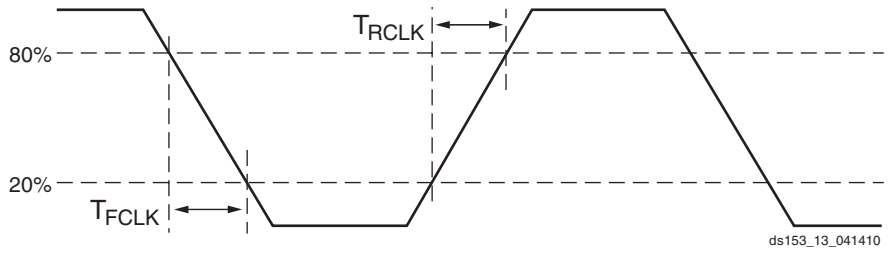

Figure 13: **Reference Clock Timing Parameters**

Table 30: **GTX Transceiver User Clock Switching Characteristics(1)**

Symbol	Description	Conditions	Speed Grade		Units
			-2	-1	
F_{TXOUT}	TXOUTCLK maximum frequency	Internal 20-bit data path	187.5	187.5	MHz
		Internal 16-bit data path	234.38	234.38	MHz
F_{RXREC}	RXRECCLK maximum frequency	Internal 20-bit data path	187.5	187.5	MHz
		Internal 16-bit data path	234.38	234.38	MHz
T_{RX}	RXUSRCLK maximum frequency		234.38	234.38	MHz
T_{RX2}	RXUSRCLK2 maximum frequency	1 byte interface	376	312.5	MHz
		2 byte interface	234.38	234.38	MHz
		4 byte interface	117.19	117.19	MHz
T_{TX}	TXUSRCLK maximum frequency		234.38	234.38	MHz
T_{TX2}	TXUSRCLK2 maximum frequency	1 byte interface	376	312.5	MHz
		2 byte interface	234.38	234.38	MHz
		4 byte interface	117.19	117.19	MHz

Notes:

1. Clocking must be implemented as described in *Virtex-6 FPGA GTX Transceivers User Guide*.

Table 31: **GTX Transceiver Transmitter Switching Characteristics**

Symbol	Description	Condition	Min	Typ	Max	Units
F_{GTXTX}	Serial data rate range		0.480	–	F_{GTXMAX}	Gb/s
T_{RTX}	TX Rise time	20%–80%	–	120	–	ps
T_{FTX}	TX Fall time	80%–20%	–	120	–	ps
T_{LLSKEW}	TX lane-to-lane skew(1)		–	–	350	ps
$V_{TXOOBVDPP}$	Electrical idle amplitude		–	–	15	mV
$T_{TXOOBTRANSITION}$	Electrical idle transition time		–	–	75	ns
$T_{J3.75}$	Total Jitter(2)(3)	3.75 Gb/s	–	–	0.34	UI
$D_{J3.75}$	Deterministic Jitter(2)(3)		–	–	0.16	UI
$T_{J3.125}$	Total Jitter(2)(3)	3.125 Gb/s	–	–	0.2	UI
$D_{J3.125}$	Deterministic Jitter(2)(3)		–	–	0.1	UI
$T_{J3.125L}$	Total Jitter(2)(3)	3.125 Gb/s(4)	–	–	0.35	UI
$D_{J3.125L}$	Deterministic Jitter(2)(3)		–	–	0.16	UI
$T_{J2.5}$	Total Jitter(2)(3)	2.5 Gb/s(5)	–	–	0.20	UI
$D_{J2.5}$	Deterministic Jitter(2)(3)		–	–	0.08	UI
$T_{J1.25}$	Total Jitter(2)(3)	1.25 Gb/s(6)	–	–	0.15	UI
$D_{J1.25}$	Deterministic Jitter(2)(3)		–	–	0.06	UI
T_{J600}	Total Jitter(2)(3)	600 Mb/s	–	–	0.1	UI
D_{J600}	Deterministic Jitter(2)(3)		–	–	0.03	UI

Switching Characteristics

All values represented in this data sheet are based on the speed specification (version 1.08). Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

Advance

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary

These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

Production

These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

All specifications are always representative of worst-case supply voltage and junction temperature conditions.

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device.

Table 36 correlates the current status of each Virtex-6 CXT device on a per speed grade basis.

Table 36: **Virtex-6 CXT Device/Speed Grade Designations**

Device	Speed Grade Designations		
	Advance	Preliminary	Production
XC6VCX75T			-2, -1
XC6VCX130T			-2, -1
XC6VCX195T			-2, -1
XC6VCX240T			-2, -1

Testing of Switching Characteristics

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Virtex-6 CXT devices.

Production Silicon and ISE Software Status

In some cases, a particular family member (and speed grade) is released to production before a speed specification is released with the correct label (Advance, Preliminary, Production). Any labeling discrepancies are corrected in subsequent speed specification releases. Table 37 lists the production released Virtex-6 family member, speed grade, and the minimum corresponding supported speed specification version and ISE software revisions. The ISE® software and speed specifications listed are the minimum releases required for production. All subsequent releases of software and speed specifications are valid.

Table 37: **Virtex-6 CXT Device/Production Software and Speed Specification Release**

Device	Speed Grade Designations	
	-2	-1
XC6VCX75T	ISE 12.2 (with speed file patch) v1.06	
XC6VCX130T	ISE 12.1 v1.04	
XC6VCX195T	ISE 12.2 (with speed file patch) v1.06	
XC6VCX240T	ISE 12.1 v1.04	

Notes:

1. Blank entries indicate a device and/or speed grade in advance or preliminary status.

Table 38: **IOB Switching Characteristics *(Cont'd)***

I/O Standard	T_{IOPI}		T_{IOOP}		T_{IOTP}		Units
	Speed Grade		Speed Grade		Speed Grade		
	-2	-1	-2	-1	-2	-1	
DIFF_SSTL18_II_T_DCI	1.09	1.09	1.67	1.67	1.67	1.67	ns
DIFF_SSTL15	1.06	1.06	1.71	1.71	1.71	1.71	ns
DIFF_SSTL15_DCI	1.06	1.06	1.68	1.68	1.68	1.68	ns
DIFF_SSTL15_T_DCI	1.06	1.06	1.68	1.68	1.68	1.68	ns

Table 39: **IOB 3-state ON Output Switching Characteristics (T_{IOTPHZ})**

Symbol	Description	Speed Grade		Units
		-2	-1	
T_{IOTPHZ}	T input to Pad high-impedance	0.99	0.99	ns

I/O Standard Adjustment Measurement Methodology

Input Delay Measurements

Table 40 shows the test setup parameters used for measuring input delay.

Table 40: **Input Delay Measurement Methodology**

Description	I/O Standard Attribute	V_L (1)(2)	V_H (1)(2)	V_{MEAS} (1,4,5)	V_{REF} (1,3,5)
LVCMOS, 2.5V	LVCMOS25	0	2.5	1.25	–
LVCMOS, 1.8V	LVCMOS18	0	1.8	0.9	–
LVCMOS, 1.5V	LVCMOS15	0	1.5	0.75	–
HSTL (High-Speed Transceiver Logic), Class I & II	HSTL_I, HSTL_II	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.75
HSTL, Class III	HSTL_III	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.90
HSTL, Class I & II, 1.8V	HSTL_I_18, HSTL_II_18	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.90
HSTL, Class III 1.8V	HSTL_III_18	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	1.08
SSTL (Stub Terminated Transceiver Logic), Class I & II, 3.3V	SSTL3_I, SSTL3_II	V_{REF} – 1.00	V_{REF} + 1.00	V_{REF}	1.5
SSTL, Class I & II, 2.5V	SSTL2_I, SSTL2_II	V_{REF} – 0.75	V_{REF} + 0.75	V_{REF}	1.25
SSTL, Class I & II, 1.8V	SSTL18_I, SSTL18_II	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.90
LVDS (Low-Voltage Differential Signaling), 2.5V	LVDS_25	1.2 – 0.125	1.2 + 0.125	0(6)	–
LVDSEXT (LVDS Extended Mode), 2.5V	LVDSEXT_25	1.2 – 0.125	1.2 + 0.125	0(6)	–
HT (HyperTransport), 2.5V	LDT_25	0.6 – 0.125	0.6 + 0.125	0(6)	–

Notes:

1. The input delay measurement methodology parameters for LVDCI are the same for LVCMOS standards of the same voltage. Input delay measurement methodology parameters for HSLVDCI are the same as for HSTL_II standards of the same voltage. Parameters for all other DCI standards are the same for the corresponding non-DCI standards.
2. Input waveform switches between V_L and V_H.
3. Measurements are made at typical, minimum, and maximum V_{REF} values. Reported delays reflect worst case of these measurements. V_{REF} values listed are typical.
4. Input voltage level from which measurement starts.
5. This is an input voltage reference that bears no relation to the V_{REF} / V_{MEAS} parameters found in IBIS models and/or noted in Figure 14.
6. The value given is the differential output voltage.

Output Delay Measurements

Output delays are measured using a Tektronix P6245 TDS500/600 probe (< 1 pF) across approximately 4" of FR4 microstrip trace. Standard termination was used for all testing. The propagation delay of the 4" trace is characterized separately and subtracted from the final measurement, and is therefore not included in the generalized test setups shown in Figure 14 and Figure 15.

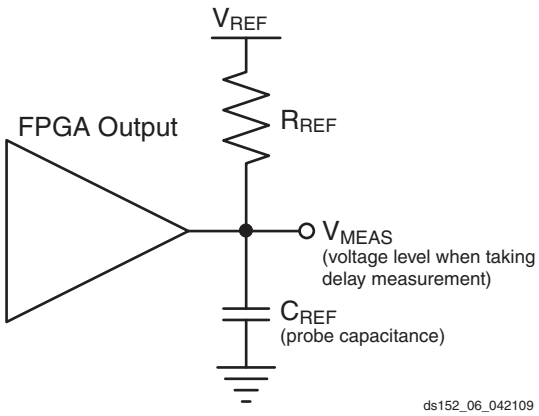

Figure 14: **Single Ended Test Setup**

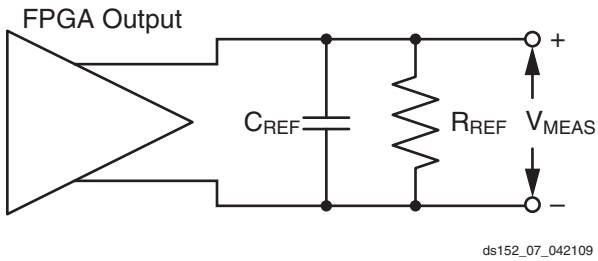

Figure 15: **Differential Test Setup**

Measurements and test conditions are reflected in the IBIS models except where the IBIS format precludes it. Parameters V_{REF}, R_{REF}, C_{REF}, and V_{MEAS} fully describe the test conditions for each I/O standard. The most accurate prediction of propagation delay in any given application can be obtained through IBIS simulation, using the following method:

1. Simulate the output driver of choice into the generalized test setup, using values from Table 41.
2. Record the time to V_{MEAS}.
3. Simulate the output driver of choice into the actual PCB trace and load, using the appropriate IBIS model or capacitance value to represent the load.
4. Record the time to V_{MEAS}.
5. Compare the results of steps 2 and 4. The increase or decrease in delay yields the actual propagation delay of the PCB trace.

Table 41: **Output Delay Measurement Methodology**

Description	I/O Standard Attribute	R_{REF} (Ω)	C_{REF} (1) (pF)	V_{MEAS} (V)	V_{REF} (V)
LVCMOS, 2.5V	LVCMOS25	1M	0	1.25	0
LVCMOS, 1.8V	LVCMOS18	1M	0	0.9	0
LVCMOS, 1.5V	LVCMOS15	1M	0	0.75	0
LVCMOS, 1.2V	LVCMOS12	1M	0	0.75	0
HSTL (High-Speed Transceiver Logic), Class I	HSTL_I	50	0	V_{REF}	0.75
HSTL, Class II	HSTL_II	25	0	V_{REF}	0.75
HSTL, Class III	HSTL_III	50	0	0.9	1.5
HSTL, Class I, 1.8V	HSTL_I_18	50	0	V_{REF}	0.9
HSTL, Class II, 1.8V	HSTL_II_18	25	0	V_{REF}	0.9
HSTL, Class III, 1.8V	HSTL_III_18	50	0	1.1	1.8
SSTL (Stub Series Terminated Logic), Class I, 1.8V	SSTL18_I	50	0	V_{REF}	0.9
SSTL, Class II, 1.8V	SSTL18_II	25	0	V_{REF}	0.9
SSTL, Class I, 2.5V	SSTL2_I	50	0	V_{REF}	1.25
SSTL, Class II, 2.5V	SSTL2_II	25	0	V_{REF}	1.25
LVDS (Low-Voltage Differential Signaling), 2.5V	LVDS_25	100	0	0 (2)	1.2
LVDSEXT (LVDS Extended Mode), 2.5V	LVDS_25	100	0	0 (2)	1.2
BLVDS (Bus LVDS), 2.5V	BLVDS_25	100	0	0 (2)	0

Table 41: **Output Delay Measurement Methodology *(Cont'd)***

Description	I/O Standard Attribute	R_{REF} (Ω)	C_{REF}[1] (pF)	V_{MEAS} (V)	V_{REF} (V)
HT (HyperTransport), 2.5V	LDT_25	100	0	0[2]	0.6
LVPECL (Low-Voltage Positive Emitter-Coupled Logic), 2.5V	LVPECL_25	100	0	0[2]	0
LVDCI/HSLVDCI, 2.5V	LVDCI_25, HSLVDCI_25	1M	0	1.25	0
LVDCI/HSLVDCI, 1.8V	LVDCI_18, HSLVDCI_18	1M	0	0.9	0
LVDCI/HSLVDCI, 1.5V	LVDCI_15, HSLVDCI_15	1M	0	0.75	0
HSTL (High-Speed Transceiver Logic), Class I & II, with DCI	HSTL_I_DCI, HSTL_II_DCI	50	0	V_{REF}	0.75
HSTL, Class III, with DCI	HSTL_III_DCI	50	0	0.9	1.5
HSTL, Class I & II, 1.8V, with DCI	HSTL_I_DCI_18, HSTL_II_DCI_18	50	0	V_{REF}	0.9
HSTL, Class III, 1.8V, with DCI	HSTL_III_DCI_18	50	0	1.1	1.8
SSTL (Stub Series Termi.Logic), Class I & II, 1.8V, with DCI	SSTL18_I_DCI, SSTL18_II_DCI	50	0	V_{REF}	0.9
SSTL, Class I & II, 2.5V, with DCI	SSTL2_I_DCI, SSTL2_II_DCI	50	0	V_{REF}	1.25

Notes:

1. C_{REF} is the capacitance of the probe, nominally 0 pF.
2. The value given is the differential output voltage.

Input/Output Logic Switching Characteristics

Table 42: **ILOGIC Switching Characteristics**

Symbol	Description	Speed Grade		Units
		-2	-1	
Setup/Hold				
T_{ICE1CK}/T_{ICKCE1}	CE1 pin Setup/Hold with respect to CLK	0.27/0.04	0.27/0.04	ns
T_{ISRCK}/T_{ICKSR}	SR pin Setup/Hold with respect to CLK	0.96/–0.10	0.96/–0.10	ns
T_{IDOCK}/T_{IOCKD}	D pin Setup/Hold with respect to CLK without Delay	0.10/0.54	0.10/0.54	ns
T_{IDOCKD}/T_{IOCKDD}	DDLY pin Setup/Hold with respect to CLK (using IODELAY)	0.14/0.42	0.14/0.40	ns
Combinatorial				
T_{IDI}	D pin to O pin propagation delay, no Delay	0.20	0.20	ns
T_{IDID}	DDLY pin to O pin propagation delay (using IODELAY)	0.25	0.25	ns
Sequential Delays				
T_{IDLO}	D pin to Q1 pin using flip-flop as a latch without Delay	0.64	0.64	ns
T_{IDLOD}	DDLY pin to Q1 pin using flip-flop as a latch (using IODELAY)	0.68	0.68	ns
T_{ICKQ}	CLK to Q outputs	0.71	0.71	ns
T_{RQ_ILOGIC}	SR pin to OQ/TQ out	1.15	1.15	ns
T_{GSRQ_ILOGIC}	Global Set/Reset to Q outputs	10.51	10.51	ns
Set/Reset				
T_{RPW_ILOGIC}	Minimum Pulse Width, SR inputs	1.20	1.20	ns, Min

CLB Distributed RAM Switching Characteristics (SLICEM Only)

Table 48: **CLB Distributed RAM Switching Characteristics**

Symbol	Description	Speed Grade		Units
		-2	-1	
Sequential Delays				
T_{SHCKO}	Clock to A – B outputs	1.36	1.56	ns, Max
T_{SHCKO_1}	Clock to AMUX – BMUX outputs	1.71	1.96	ns, Max
Setup and Hold Times Before/After Clock CLK				
T_{DS}/T_{DH}	A – D inputs to CLK	0.88/0.22	1.01/0.26	ns, Min
T_{AS}/T_{AH}	Address An inputs to clock	0.27/0.70	0.31/0.80	ns, Min
T_{WS}/T_{WH}	WE input to clock	0.40/–0.01	0.46/0.00	ns, Min
T_{CECK}/T_{CKCE}	CE input to CLK	0.41/–0.02	0.48/–0.01	ns, Min
Clock CLK				
T_{MPW}	Minimum pulse width	1.00	1.15	ns, Min
T_{MCP}	Minimum clock period	2.00	2.30	ns, Min

Notes:

1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values cannot be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.
2. T_{SHCKO} also represents the CLK to XMUX output. Refer to the TRACE report for the CLK to XMUX path.

CLB Shift Register Switching Characteristics (SLICEM Only)

Table 49: **CLB Shift Register Switching Characteristics**

Symbol	Description	Speed Grade		Units
		-2	-1	
Sequential Delays				
T_{REG}	Clock to A – D outputs	1.58	1.82	ns, Max
T_{REG_MUX}	Clock to AMUX – DMUX output	1.93	2.22	ns, Max
T_{REG_M31}	Clock to DMUX output via M31 output	1.55	1.78	ns, Max
Setup and Hold Times Before/After Clock CLK				
T_{WS}/T_{WH}	WE input	0.09/–0.01	0.10/0.00	ns, Min
T_{CECK}/T_{CKCE}	CE input to CLK	0.10/–0.02	0.11/–0.01	ns, Min
T_{DS}/T_{DH}	A – D inputs to CLK	0.94/0.24	1.08/0.28	ns, Min
Clock CLK				
T_{MPW}	Minimum pulse width	0.85	0.98	ns, Min

Notes:

1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values cannot be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

DSP48E1 Switching Characteristics

Table 51: **DSP48E1 Switching Characteristics**

Symbol	Description	Speed Grade		Units
		-2	-1	
Setup and Hold Times of Data/Control Pins to the Input Register Clock				
$T_{DSPDCK\_\{A, ACIN; B, BCIN\}\_\{AREG; BREG\}}$/ $T_{DSPCKD\_\{A, ACIN; B, BCIN\}\_\{AREG; BREG\}}$	{A, ACIN, B, BCIN} input to {A, B} register CLK	0.35/0.34	0.41/0.39	ns
$T_{DSPDCK\_C\_CREG}$/$T_{DSPCKD\_C\_CREG}$	C input to C register CLK	0.22/0.24	0.26/0.27	ns
$T_{DSPDCK\_D\_DREG}$/$T_{DSPCKD\_D\_DREG}$	D input to D register CLK	0.15/0.39	0.17/0.44	ns
Setup and Hold Times of Data Pins to the Pipeline Register Clock				
$T_{DSPDCK\_\{A, ACIN, B, BCIN\}\_PREG\_MULT}$/ $T_{DSPCKD\_\{A, ACIN, B, BCIN\}\_PREG\_MULT}$	{A, ACIN, B, BCIN} input to M register CLK	3.21/0.02	3.69/0.02	ns
$T_{DSPDCK\_\{A, D\}\_ADREG}$/ $T_{DSPCKD–\{A, D\}\_ADREG}$	{A, D} input to AD register CLK	1.69/0.13	1.94/0.15	ns
Setup and Hold Times of Data/Control Pins to the Output Register Clock				
$T_{DSPDCK\_\{A, ACIN, B, BCIN\}\_PREG\_MULT}$/ $T_{DSPCKD\_\{A, ACIN, B, BCIN\}\_PREG\_MULT}$	{A, ACIN, B, BCIN} input to P register CLK using multiplier	5.20/–0.19	5.97/–0.22	ns
$T_{DSPDCK\_D\_DREG\_MULT}$/ $T_{DSPCKD\_D\_DREG\_MULT}$	D input to P register CLK	4.90/–0.65	5.63/–0.75	ns
$T_{DSPDCK\_\{A, ACIN, B, BCIN\}\_PREG}$/ $T_{DSPCKD\_\{A, ACIN, B, BCIN\}\_PREG}$	{A, ACIN, B, BCIN} input to P register CLK not using multiplier	2.15/–0.19	2.47/–0.22	ns
$T_{DSPDCK\_C\_PREG}$/ $T_{DSPCKD\_C\_PREG}$	C input to P register CLK	1.91/–0.14	2.19/–0.17	ns
$T_{DSPDCK\_\{PCIN, CARRYCASCIN, MULTSIGNIN\}\_PREG}$/ $T_{DSPCKD\_\{PCIN, CARRYCASCIN, MULTSIGNIN\}\_PREG}$	{PCIN, CARRYCASCIN, MULTSIGNIN} input to P register CLK	1.67/–0.04	1.92/–0.05	ns
Setup and Hold Times of the CE Pins				
$T_{DSPDCK\_\{CEA; CEB\}\_\{AREG; BREG\}}$/ $T_{DSPCKD\_\{CEA; CEB\}\_\{AREG; BREG\}}$	{CEA; CEB} input to {A; B} register CLK	0.22/0.25	0.25/0.29	ns
$T_{DSPDCK\_CEC\_CREG}$/ $T_{DSPCKD\_CEC\_CREG}$	CEC input to C register CLK	0.24/0.23	0.28/0.27	ns
$T_{DSPDCK\_CED\_DREG}$/ $T_{DSPCKD\_CED\_DREG}$	CED input to D register CLK	0.31/0.14	0.35/0.16	ns
$T_{DSPDCK\_CEM\_MREG}$/ $T_{DSPCKD\_CEM\_MREG}$	CEM input to M register CLK	0.26/0.25	0.30/0.28	ns
$T_{DSPDCK\_CEP\_PREG}$/ $T_{DSPCKD\_CEP\_PREG}$	CEP input to P register CLK	0.46/0.03	0.53/0.03	ns
Setup and Hold Times of the RST Pins				
$T_{DSPDCK\_\{RSTA; RSTB\}\_\{AREG; BREG\}}$/ $T_{DSPCKD\_\{RSTA; RSTB\}\_\{AREG; BREG\}}$	{RSTA, RSTB} input to {A, B} register CLK	0.38/0.22	0.43/0.25	ns
$T_{DSPDCK\_RSTC\_CREG}$/ $T_{DSPCKD\_RSTC\_CREG}$	RSTC input to C register CLK	0.23/0.09	0.27/0.11	ns
$T_{DSPDCK\_RSTD\_DREG}$/ $T_{DSPCKD\_RSTD\_DREG}$	RSTD input to D register CLK	0.38/0.19	0.44/0.21	ns
$T_{DSPDCK\_RSTM\_MREG}$/ $T_{DSPCKD\_RSTM\_MREG}$	RSTM input to M register CLK	0.26/0.30	0.30/0.35	ns
$T_{DSPDCK\_RSTP\_PREG}$/ $T_{DSPCKD\_RSTP\_PREG}$	RSTP input to P register CLK	0.33/0.05	0.41/0.06	ns
Combinatorial Delays from Input Pins to Output Pins				
$T_{DSPDO\_\{A, B\}\_\{P, CARRYOUT\}\_MULT}$	{A, B} input to {P, CARRYOUT} output using multiplier	5.08	5.84	ns
$T_{DSPDO\_D\_\{P, CARRYOUT\}\_MULT}$	D input to {P, CARRYOUT} output using multiplier	4.82	5.54	ns
$T_{DSPDO\_\{A, B\}\_\{P, CARRYOUT\}}$	{A, B} input to {P, CARRYOUT} output not using multiplier	2.07	2.38	ns
$T_{DSPDO\_\{C, CARRYIN\}\_\{P, CARRYOUT\}}$	{C, CARRYIN} input to {P, CARRYOUT} output	1.83	2.10	ns

Table 51: **DSP48E1 Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade		Units
		-2	-1	
Clock to Outs from Input Register Clock to Cascading Output Pins				
$T_{DSPCKO\_\{ACOUT;\ BCOUT\}\_\{AREG;\ BREG\}}$	CLK (AREG, BREG) to {P, CARRYOUT} output	0.89	1.02	ns
$T_{DSPCKO\_\{PCOUT,\ CARRYCASCOUT,\ MULTSIGNOUT\}\_\{AREG,\ BREG\}\_MULT}$	CLK (AREG, BREG) to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output using multiplier	5.49	6.31	ns
$T_{DSPCKO\_\{PCOUT,\ CARRYCASCOUT,\ MULTSIGNOUT\}\_\{AREG,\ BREG\}}$	CLK (AREG, BREG) to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output not using multiplier	2.40	2.76	ns
$T_{DSPCKO\_\{PCOUT,\ CARRYCASCOUT,\ MULTSIGNOUT\}\_DREG\_MULT}$	CLK (DREG) to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output using multiplier	5.38	6.18	ns
$T_{DSPCKO\_\{PCOUT,\ CARRYCASCOUT,\ MULTSIGNOUT\}\_CREG}$	CLK (CREG) to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output	2.40	2.76	ns
Maximum Frequency				
F_{MAX}	With all registers used	350	275	MHz
F_{MAX_PATDET}	With pattern detector	350	275	MHz
$F_{MAX\_MULT\_NOMREG}$	Two register multiply without MREG	262	227	MHz
$F_{MAX\_MULT\_NOMREG\_PATDET}$	Two register multiply without MREG with pattern detect	241	209	MHz
$F_{MAX\_PREADD\_MULT\_NOADREG}$	Without ADREG	292	253	MHz
$F_{MAX\_PREADD\_MULT\_NOADREG\_PATDET}$	Without ADREG with pattern detect	292	253	MHz
$F_{MAX\_NOPIPELINEREG}$	Without pipeline registers (MREG, ADREG)	196	170	MHz
$F_{MAX\_NOPIPELINEREG\_PATDET}$	Without pipeline registers (MREG, ADREG) with pattern detect	184	160	MHz

Table 55: **Regional Clock Switching Characteristics (BUFR)**

Symbol	Description	Speed Grade		Units
		-2	-1	
T_{BRCKO_O}	Clock to out delay from I to O	0.75	0.75	ns
		0.75	0.75	ns
		0.75	0.75	ns
		0.75	0.75	ns
$T_{BRCKO\_O\_BYP}$	Clock to out delay from I to O with Divide Bypass attribute set	0.37	0.37	ns
		0.37	0.37	ns
		0.37	0.37	ns
		0.37	0.37	ns
T_{BRDO_O}	Propagation delay from CLR to O	0.83	0.83	ns
Maximum Frequency				
F_{MAX}	Regional clock tree (BUFR)	300	300	MHz

Table 56: **Horizontal Clock Buffer Switching Characteristics (BUFH)**

Symbol	Description	Speed Grade		Units
		-2	-1	
T_{BHCKO_O}	BUFH delay from I to O	0.13	0.13	ns
$T_{BHCCK\_CE}/T_{BHCKC\_CE}$	CE pin Setup and Hold	0.05/0.05	0.05/0.05	ns
Maximum Frequency				
F_{MAX}	Horizontal clock buffer (BUFH)	700	700	MHz

MMCM Switching Characteristics

Table 57: **MMCM Specification**

Symbol	Description	Speed Grade		Units
		-2	-1	
F_{INMAX}	Maximum Input Clock Frequency(1)	700	700	MHz
F_{INMIN}	Minimum Input Clock Frequency	10	10	MHz
$F_{INJITTER}$	Maximum Input Clock Period Jitter	< 20% of clock input period or 1 ns Max		
F_{INDUTY}	Allowable Input Duty Cycle: 10—49 MHz	25/75		%
	Allowable Input Duty Cycle: 50—199 MHz	30/70		%
	Allowable Input Duty Cycle: 200—399 MHz	35/65		%
	Allowable Input Duty Cycle: 400—499 MHz	40/60		%
	Allowable Input Duty Cycle: >500 MHz	45/55		%
F_{MIN_PSCLK}	Minimum Dynamic Phase Shift Clock Frequency	0.01	0.01	MHz
F_{MAX_PSCLK}	Maximum Dynamic Phase Shift Clock Frequency	450	450	MHz
F_{VCOMIN}	Minimum MMCM VCO Frequency	600	600	MHz
F_{VCOMAX}	Maximum MMCM VCO Frequency	1200	1200	MHz
$F_{BANDWIDTH}$	Low MMCM Bandwidth at Typical(2)	1.00	1.00	MHz
	High MMCM Bandwidth at Typical(2)	4.00	4.00	MHz

Virtex-6 CXT Device Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. The representative values for typical pin locations and normal clock loading are listed in Table 61. Values are expressed in nanoseconds unless otherwise noted.

Table 61: **Global Clock Input Setup and Hold Without MMCM**

Symbol	Description	Device	Speed Grade		Units
			-2	-1	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard.(1)					
T_{PSFD}/ T_{PHFD}	Full Delay (Legacy Delay or Default Delay) Global Clock Input and IFF(2) without MMCM	XC6VCX75T	1.75/–0.01	1.75/–0.01	ns
		XC6VCX130T	1.88/–0.11	1.88/–0.11	ns
		XC6VCX195T	1.97/–0.14	1.97/–0.14	ns
		XC6VCX240T	1.97/–0.14	1.97/–0.14	ns

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input Flip-Flop or Latch.
3. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.

Table 62: **Global Clock Input Setup and Hold With MMCM**

Symbol	Description	Device	Speed Grade		Units
			-2	-1	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard.(1)					
$T_{PSMMCMGC}$/ $T_{PHMMCMGC}$	No Delay Global Clock Input and IFF(2) with MMCM	XC6VCX75T	1.72/–0.22	1.72/–0.22	ns
		XC6VCX130T	1.81/–0.21	1.81/–0.21	ns
		XC6VCX195T	1.82/–0.20	1.82/–0.20	ns
		XC6VCX240T	1.82/–0.20	1.82/–0.20	ns

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input Flip-Flop or Latch.
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 63: **Clock-Capable Clock Input Setup and Hold With MMCM**

Symbol	Description	Device	Speed Grade		Units
			-2	-1	
Input Setup and Hold Time Relative to Clock-capable Clock Input Signal for LVCMOS25 Standard.(1)					
$T_{PSMMCMCC}$/ $T_{PHMMCMCC}$	No Delay Clock-capable Clock Input and IFF(2) with MMCM	XC6VCX75T	1.86/–0.28	1.86/–0.28	ns
		XC6VCX130T	1.93/–0.28	1.93/–0.28	ns
		XC6VCX195T	1.96/–0.27	1.96/–0.27	ns
		XC6VCX240T	1.96/–0.27	1.96/–0.27	ns

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input Flip-Flop or Latch.
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Clock Switching Characteristics

The parameters in this section provide the necessary values for calculating timing budgets for Virtex-6 CXT FPGA clock transmitter and receiver data-valid windows.

Table 64: **Duty Cycle Distortion and Clock-Tree Skew**

Symbol	Description	Device	Speed Grade		Units
			-2	-1	
T_{DCD_CLK}	Global Clock Tree Duty Cycle Distortion(1)	All	0.12	0.12	ns
T_{CKSKEW}	Global Clock Tree Skew(2)	XC6VCX75T	0.18	0.18	ns
		XC6VCX130T	0.29	0.29	ns
		XC6VCX195T	0.31	0.31	ns
		XC6VCX240T	0.31	0.31	ns
T_{DCD_BUFIO}	I/O clock tree duty cycle distortion	All	0.08	0.08	ns
$T_{BUFIOSKEW}$	I/O clock tree skew across one clock region	All	0.03	0.03	ns
$T_{BUFIOSKEW2}$	I/O clock tree skew across three clock regions	All	0.22	0.22	ns
T_{DCD_BUFR}	Regional clock tree duty cycle distortion	All	0.15	0.15	ns

Notes:

1. These parameters represent the worst-case duty cycle distortion observable at the pins of the device using LVDS output buffers. For cases where other I/O standards are used, IBIS can be used to calculate any additional duty cycle distortion that might be caused by asymmetrical rise/fall times.
2. The T_{CKSKEW} value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx FPGA_Editor and Timing Analyzer tools to evaluate clock skew specific to your application.

Table 65: **Package Skew**

Symbol	Description	Device	Package	Value	Units
$T_{PKGSKEW}$	Package Skew(1)	XC6VCX75T	FF484		ps
			FF784		ps
		XC6VCX130T	FF484	95	ps
			FF784	146	ps
			FF1156	165	ps
		XC6VCX195T	FF784		ps
			FF1156		ps
		XC6VCX240T	FF784	146	ps
			FF1156	182	ps

Notes:

1. These values represent the worst-case skew between any two SelectIO resources in the package: shortest flight time to longest flight time from Pad to Ball (7.0 ps per mm).
2. Package trace length information is available for these device/package combinations. This information can be used to deskew the package.

Table 66: **Sample Window**

Symbol	Description	Device	Speed Grade		Units
			-2	-1	
T_{SAMP}	Sampling Error at Receiver Pins(1)	All	610	610	ps
T_{SAMP_BUFIO}	Sampling Error at Receiver Pins using BUFIO(2)	All	400	400	ps

Notes:

1. This parameter indicates the total sampling error of Virtex-6 CXT FPGA DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the MMCM to capture the DDR input registers' edges of operation. These measurements include:
   - CLK0 MMCM jitter
   - MMCM accuracy (phase offset)
   - MMCM phase shift resolution

   These measurements do not include package or clock tree skew.
2. This parameter indicates the total sampling error of Virtex-6 CXT FPGA DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the BUFIO clock network and IODELAY to capture the DDR input registers' edges of operation. These measurements do not include package or clock tree skew.

Table 67: **Pin-to-Pin Setup/Hold and Clock-to-Out**

Symbol	Description	Speed Grade		Units
		-2	-1	
Data Input Setup and Hold Times Relative to a Forwarded Clock Input Pin Using BUFIO				
T_{PSCS}/T_{PHCS}	Setup/Hold of I/O clock	–0.33/1.31	–0.33/1.31	ns
Pin-to-Pin Clock-to-Out Using BUFIO				
$T_{ICKOFCS}$	Clock-to-Out of I/O clock	5.19	5.19	ns

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
07/08/09	1.0	Initial Xilinx release.
02/05/10	1.1	Removed Figure 11: Placement Diagram for the FF1156 Package (5 of 5) from page 11 as there are only 16 GTX transceivers in the FF1156 package. Corrected the placement diagrams in Figure 2 through Figure 10.