AMD Xilinx - XC6VCX195T-2FFG1156C Datasheet

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Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	15600
Number of Logic Elements/Cells	199680
Total RAM Bits	12681216
Number of I/O	600
Number of Gates	-
Voltage - Supply	0.95V ~ 1.05V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1156-BBGA, FCBGA
Supplier Device Package	1156-FCBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc6vcx195t-2ffg1156c

Virtex-6 CXT FPGA Feature Summary

Table 1: **Virtex-6 CXT FPGA Feature Summary by Device**

Device	Logic Cells	Configurable Logic Blocks (CLBs)		DSP48E1 Slices(2)	Block RAM Blocks			MMCMs(4)	Interface Blocks for PCI Express	Ethernet MACs(5)	Maximum GTX Transceivers	Total I/O Banks(6)	Max User I/O(7)
		Slices(1)	Max Distributed RAM (Kb)		18 Kb(3)	36 Kb	Max (Kb)						
XC6VCX75T	74,496	11,640	1,045	288	312	156	5,616	6	1	1	12	9	360
XC6VCX130T	128,000	20,000	1,740	480	528	264	9,504	10	2	1	16	15	600
XC6VCX195T	199,680	31,200	3,040	640	688	344	12,384	10	2	1	16	15	600
XC6VCX240T	241,152	37,680	3,650	768	832	416	14,976	12	2	1	16	18	600

Notes:

1. Each Virtex-6 CXT FPGA slice contains four LUTs and eight flip-flops, only some slices can use their LUTs as distributed RAM or SRLs.
2. Each DSP48E1 slice contains a 25 x 18 multiplier, an adder, and an accumulator.
3. Block RAMs are fundamentally 36 Kbits in size. Each block can also be used as two independent 18 Kb blocks.
4. Each CMT contains two mixed-mode clock managers (MMCM).
5. This table lists individual Ethernet MACs per device.
6. Does not include configuration Bank 0.
7. This number does not include GTX transceivers.

Virtex-6 CXT FPGA Device-Package Combinations and Maximum I/Os

Virtex-6 CXT FPGA package combinations with the maximum available I/Os per package are shown in Table 2.

Table 2: **Virtex-6 CXT FPGA Device-Package Combinations and Maximum Available I/Os**

Package	FF484 FFG484		FF784 FFG784		FF1156 FFG1156	
Size (mm)	23 x 23		29 x 29		35 x 35	
Device	GTs	I/O	GTs	I/O	GTs	I/O
XC6VCX75T	8 GTXs	240	12 GTXs	360		
XC6VCX130T	8 GTXs	240	12 GTXs	400	16 GTXs	600
XC6VCX195T			12 GTXs	400	16 GTXs	600
XC6VCX240T			12 GTXs	400	16 GTXs	600

Notes:

1. Flip-chip packages are also available in Pb-Free versions (FFG).

Virtex-6 CXT FPGA Ordering Information

The Virtex-6 CXT FPGA ordering information shown in Figure 1 applies to all packages including Pb-Free.

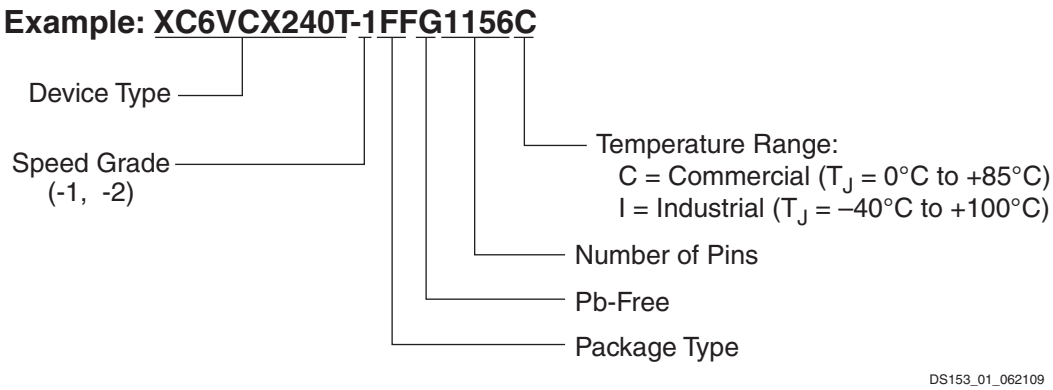

Figure 1: **Virtex-6 CXT FPGA Ordering Information**

Virtex-6 CXT FPGA Documentation

In addition to the data sheet information found herein, complete and up-to-date documentation of the Virtex-6 family of FPGAs is available on the Xilinx website and available for download:

Virtex-6 FPGA Configuration Guide **(UG360)**

This all-encompassing configuration guide includes chapters on configuration interfaces (serial and parallel), multi-bitstream management, bitstream encryption, boundary-scan and JTAG configuration, and reconfiguration techniques.

Virtex-6 FPGA SelectIO Resources User Guide **(UG361)**

This guide describes the SelectIO™ resources available in all the Virtex-6 CXT devices.

Virtex-6 FPGA Clocking Resources User Guide **(UG362)**

This guide describes the clocking resources available in all the Virtex-6 CXT devices, including the MMCM and clock buffers.

Virtex-6 FPGA Memory Resources User Guide **(UG363)**

This guide describes the Virtex-6 CXT device block RAM and FIFO capabilities.

Virtex-6 FPGA CLB User Guide **(UG364)**

This guide describes the capabilities of the configurable logic blocks (CLB) available in all Virtex-6 CXT devices.

Virtex-6 FPGA DSP48E1 Slice User Guide **(UG369)**

This guide describes the architecture of the DSP48E1 slice in Virtex-6 CXT FPGAs and provides configuration examples.

Virtex-6 FPGA GTX Transceivers User Guide **(UG366)**

This guide describes the GTX transceivers available in all the Virtex-6 CXT FPGAs.

Virtex-6 FPGA Tri-Mode Ethernet MAC User Guide **(UG368)**

This guide describes the dedicated tri-mode Ethernet media access controller (TEMAC) available in all the Virtex-6 CXT FPGAs.

Virtex-6 FPGA Data Sheet: DC and Switching Characteristics **(DS152)**

Reference this data sheet when considering device migration to the Virtex-6 LXT and SXT families. It contains the DC and Switching Characteristic specifications specifically for the Virtex-6 LXT and SXT families.

Virtex-6 FPGA Packaging and Pinout Specifications **(UG365)**

These specifications includes the tables for device/package combinations and maximum I/Os, pin definitions, pinout tables, pinout diagrams, mechanical drawings, and thermal specifications of the Virtex-6 LXT and SXT families. Reference these specifications when considering device migration to the Virtex-6 LXT and SXT families.

Configuration Bitstream Overview for CXT Devices

This section contains two tables similar to those in the *Virtex-6 FPGA Configuration Guide* only updated for the CXT family. The Virtex-6 CXT FPGA bitstream contains commands to the FPGA configuration logic as well as configuration data. Table 3 gives a typical bitstream length and Table 4 gives the specific device ID codes for the Virtex-6 CXT devices.

Table 3: **Virtex-6 CXT FPGA Bitstream Length**

Device	Total Number of Configuration Bits
XC6VCX75T	26,239,328
XC6VCX130T	43,719,776
XC6VCX195T	61,552,736
XC6VCX240T	73,859,552

Table 4: **Virtex-6 CXT FPGA Device ID Codes**

Device	ID Code (Hex)
XC6VCX75T	0x042C4093
XC6VCX130T	0x042CA093
XC6VCX195T	0x042CC093
XC6VCX240T	0x042D0093

Table 8: **Available I/O Pin/Device/Package Combinations**

Virtex-6 CXT Device	User I/O Pins	Virtex-6 CXT FPGA Package		
		FF484	FF784	FF1156
XC6VCX75T	Available User I/Os	240	360	–
	Differential I/O Pairs	120	180	–
XC6VCX130T	Available User I/Os	240	400	600
	Differential I/O Pairs	120	200	300
XC6VCX195T	Available User I/Os	–	400	600
	Differential I/O Pairs	–	200	300
XC6VCX240T	Available User I/Os	–	400	600
	Differential I/O Pairs	–	200	300

GTX Transceivers in CXT Devices

CXT devices have between 8 to 16 gigabit transceiver circuits. Each GTX transceiver is a combined transmitter and receiver capable of operating at a data rate between 480 Mb/s and 3.75 Gb/s. Lower data rates can be achieved using FPGA logic-based oversampling. The transmitter and receiver are independent circuits that use separate PLLs to multiply the reference frequency input by certain programmable numbers between 2 and 25, to become the bit-serial data clock. Each GTX transceiver has a large number of user-definable features and parameters. All of these can be defined during device configuration, and many can also be modified during operation.

FF784 Package Placement Diagrams

Figure 4 through Figure 6 show the placement diagrams for the GTX transceivers in the FF784 package.

Note: Unbonded locations in the FF784 package are:

- CX130T: X0Y0, X0Y1, X0Y2, X0Y3
- CX195T: X0Y0, X0Y1, X0Y2, X0Y3
- CX240T: X0Y0, X0Y1, X0Y2, X0Y3

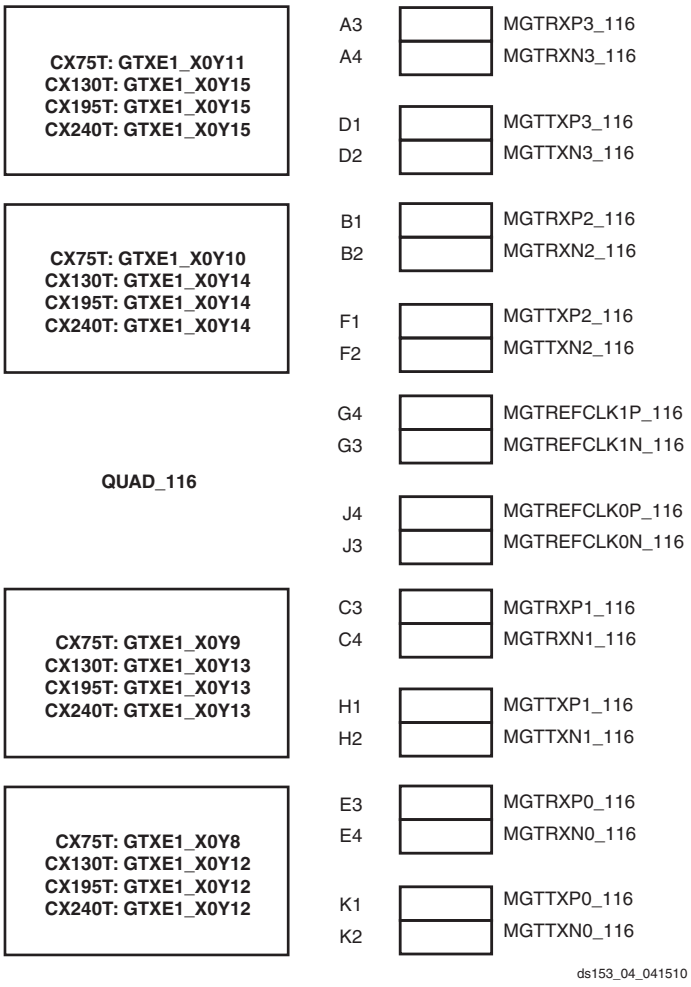

Figure 4: **Placement Diagram for the FF784 Package (1 of 3)**

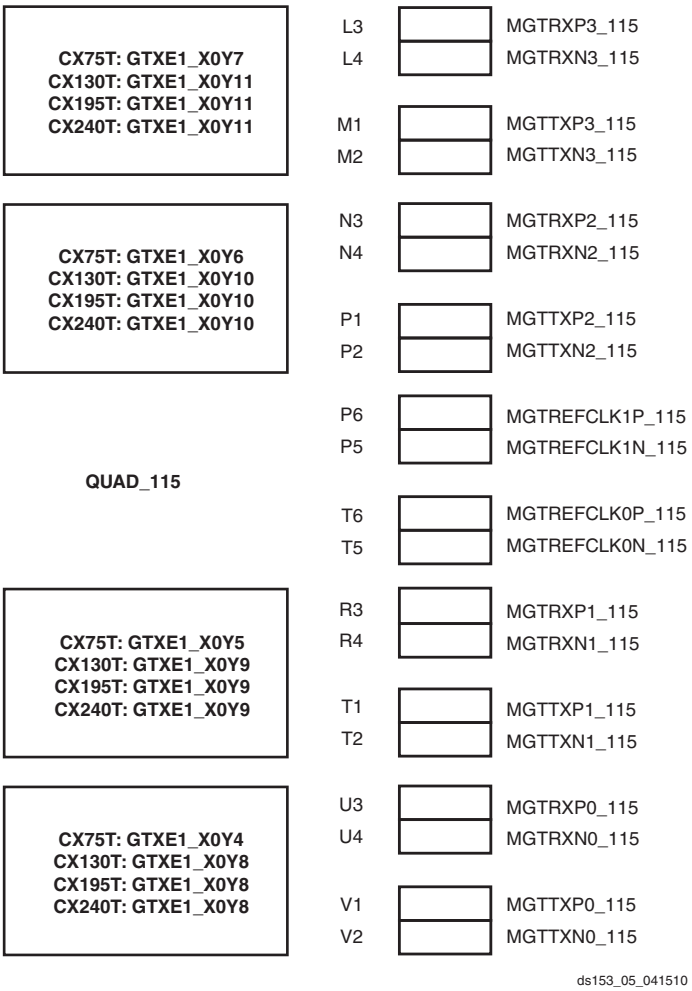

Figure 5: **Placement Diagram for the FF784 Package (2 of 3)**

FF1156 Package Placement Diagrams

Figure 7 through Figure 10 show the placement diagrams for the GTX transceivers in the FF1156 package.

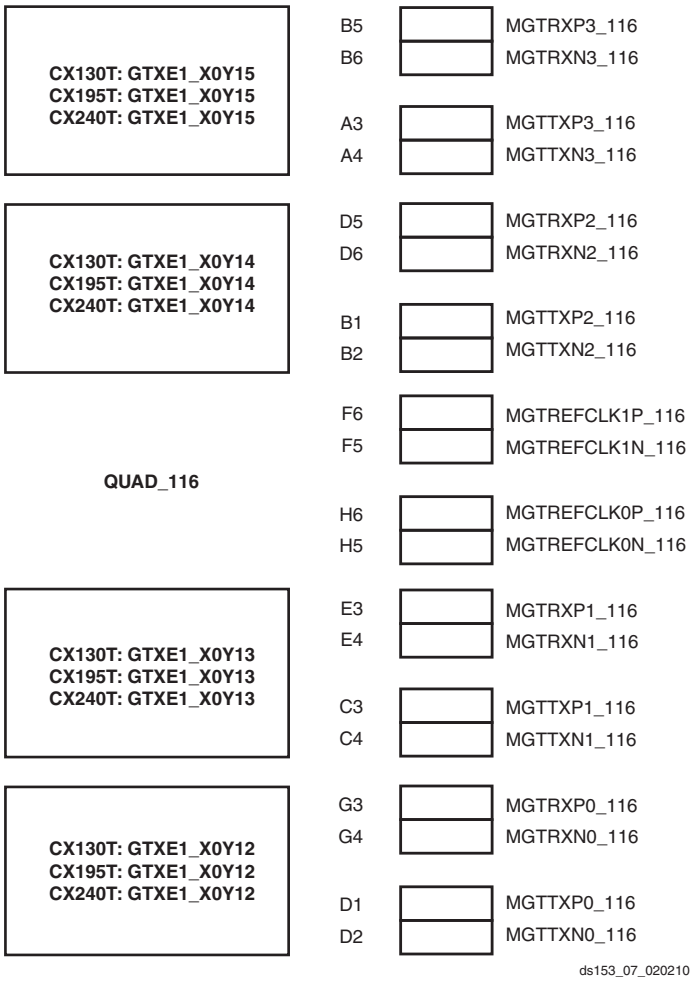

Figure 7: **Placement Diagram for the FF1156 Package (1 of 4)**

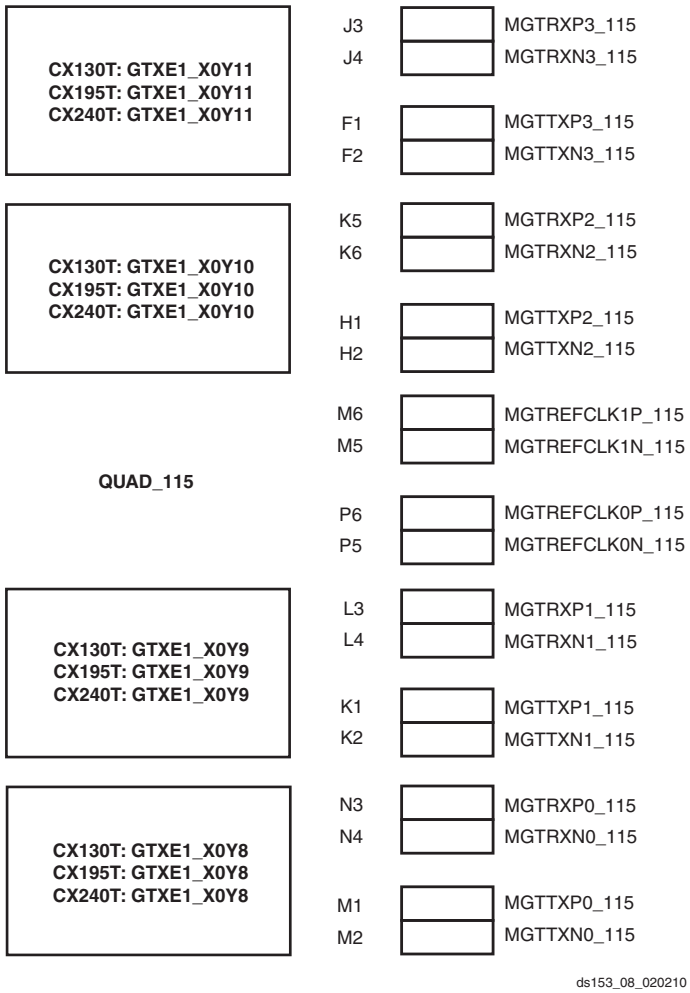

Figure 8: **Placement Diagram for the FF1156 Package (2 of 4)**

Virtex-6 CXT FPGA Electrical Characteristics Introduction

Virtex-6 CXT FPGAs are available in -2 and -1 speed grades, with -2 having the highest performance. Virtex-6 CXT FPGA DC and AC characteristics are specified for both commercial and industrial grades. Except the operating temperature range or unless otherwise noted, all the DC and AC electrical parameters are the same for a particular speed grade (that is, the timing characteristics of a -1 speed grade industrial device are the same as for a -1 speed grade commercial device). However, only selected speed grades and/or devices might be available in the industrial range.

All supply voltage and junction temperature specifications are representative of worst-case conditions. The parameters included are common to popular designs and typical applications.

All specifications are subject to change without notice.

Virtex-6 CXT FPGA DC Characteristics

Table 9: **Absolute Maximum Ratings(1)**

Symbol	Description		Units
V_{CCINT}	Internal supply voltage relative to GND	–0.5 to 1.1	V
V_{CCAUX}	Auxiliary supply voltage relative to GND	–0.5 to 3.0	V
V_{CCO}	Output drivers supply voltage relative to GND	–0.5 to 3.0	V
V_{BATT}	Key memory battery backup supply	–0.5 to 3.0	V
V_{FS}	External voltage supply for eFUSE programming(2)	–0.5 to 3.0	V
V_{REF}	Input reference voltage	–0.5 to 3.0	V
V_{IN}(3)	2.5V or below I/O input voltage relative to GND(4) (user and dedicated I/Os)	–0.5 to V_{CCO} + 0.5	V
V_{TS}	Voltage applied to 3-state 2.5V or below output(4) (user and dedicated I/Os)	–0.5 to V_{CCO} + 0.5	V
T_{STG}	Storage temperature (ambient)	–65 to 150	°C
T_{SOL}	Maximum soldering temperature(5)	+220	°C
T_j	Maximum junction temperature(5)	+125	°C

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
2. When not programming eFUSE, connect V_{FS} to GND.
3. 2.5V I/O absolute maximum limit applied to DC and AC signals.
4. For I/O operation, refer to the *Virtex-6 FPGA SelectIO Resources User Guide*.
5. For soldering guidelines and thermal considerations, see *Virtex-6 FPGA Packaging and Pinout Specification*.

SelectIO™ DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

Table 15: **SelectIO DC Input and Output Levels**

I/O Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
LVCMOS25, LVDCI25	–0.3	0.7	1.7	V_{CCO} + 0.3	0.4	V_{CCO} – 0.4	Note(3)	Note(3)
LVCMOS18, LVDCI18	–0.3	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.3	0.45	V_{CCO} – 0.45	Note(4)	Note(4)
LVCMOS15, LVDCI15	–0.3	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.3	25% V_{CCO}	75% V_{CCO}	Note(4)	Note(4)
LVCMOS12	–0.3	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.3	25% V_{CCO}	75% V_{CCO}	Note(5)	Note(5)
HSTL I_12	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.3	25% V_{CCO}	75% V_{CCO}	6.3	6.3
HSTL I(2)	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.3	0.4	V_{CCO} – 0.4	8	–8
HSTL II(2)	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.3	0.4	V_{CCO} – 0.4	16	–16
HSTL III(2)	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.3	0.4	V_{CCO} – 0.4	24	–8
DIFF HSTL I(2)	–0.3	50% V_{CCO} – 0.1	50% V_{CCO} + 0.1	V_{CCO} + 0.3	–	–	–	–
DIFF HSTL II(2)	–0.3	50% V_{CCO} – 0.1	50% V_{CCO} + 0.1	V_{CCO} + 0.3	–	–	–	–
SSTL2 I	–0.3	V_{REF} – 0.15	V_{REF} + 0.15	V_{CCO} + 0.3	V_{TT} – 0.61	V_{TT} + 0.61	8.1	–8.1
SSTL2 II	–0.3	V_{REF} – 0.15	V_{REF} + 0.15	V_{CCO} + 0.3	V_{TT} – 0.81	V_{TT} + 0.81	16.2	–16.2
DIFF SSTL2 I	–0.3	50% V_{CCO} – 0.15	50% V_{CCO} + 0.15	V_{CCO} + 0.3	–	–	–	–
DIFF SSTL2 II	–0.3	50% V_{CCO} – 0.15	50% V_{CCO} + 0.15	V_{CCO} + 0.3	–	–	–	–
SSTL18 I	–0.3	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.3	V_{TT} – 0.47	V_{TT} + 0.47	6.7	–6.7
SSTL18 II	–0.3	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.3	V_{TT} – 0.60	V_{TT} + 0.60	13.4	–13.4
DIFF SSTL18 I	–0.3	50% V_{CCO} – 0.125	50% V_{CCO} + 0.125	V_{CCO} + 0.3	–	–	–	–
DIFF SSTL18 II	–0.3	50% V_{CCO} – 0.125	50% V_{CCO} + 0.125	V_{CCO} + 0.3	–	–	–	–
SSTL15	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.3	V_{TT} – 0.175	V_{TT} + 0.175	14.3	14.3

Notes:

1. Tested according to relevant specifications.
2. Applies to both 1.5V and 1.8V HSTL.
3. Using drive strengths of 2, 4, 6, 8, 12, 16, or 24 mA.
4. Using drive strengths of 2, 4, 6, 8, 12, or 16 mA.
5. Supported drive strengths of 2, 4, 6, or 8 mA.
6. For detailed interface specific DC voltage levels, see the *Virtex-6 FPGA SelectIO Resources User Guide*.

LVPECL DC Specifications (LVPECL_25)

These values are valid when driving a 100Ω differential load only, i.e., a 100Ω resistor between the two receiver pins. The V_{OH} levels are 200 mV below standard LVPECL levels and are compatible with devices tolerant of lower common-mode ranges. Table 19 summarizes the DC output specifications of LVPECL. For more information on using LVPECL, see the *Virtex-6 FPGA SelectIO Resources User Guide*.

Table 19: **LVPECL DC Specifications**

Symbol	DC Parameter	Min	Typ	Max	Units
V_{OH}	Output High Voltage	V_{CC} – 1.025	1.545	V_{CC} – 0.88	V
V_{OL}	Output Low Voltage	V_{CC} – 1.81	0.795	V_{CC} – 1.62	V
V_{ICM}	Input Common-Mode Voltage	0.6	–	2.2	V
V_{IDIFF}	Differential Input Voltage(1)(2)	0.100	–	1.5	V

Notes:

1. Recommended input maximum voltage not to exceed V_{CCAUX} + 0.2V.
2. Recommended input minimum voltage not to go below –0.5V.

eFUSE Read Endurance

Table 20 lists the maximum number of read cycle operations expected. For more information, see the *Virtex-6 FPGA Configuration User Guide*.

Table 20: **eFUSE Read Endurance**

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
DNA_CYCLES	Number of DNA_PORT READ operations or JTAG ISC_DNA read command operations. Unaffected by SHIFT operations.	30,000,000				Read Cycles
AES_CYCLES	Number of JTAG FUSE_KEY or FUSE_CNTL read command operations. Unaffected by SHIFT operations.	30,000,000				Read Cycles

GTX Transceiver Specifications

GTX Transceiver DC Characteristics

Table 21: **Absolute Maximum Ratings for GTX Transceivers(1)**

Symbol	Description	Min	Max	Units
MGTAVCC	Analog supply voltage for the GTX transmitter and receiver circuits relative to GND	–0.5	1.1	V
MGTAVTT	Analog supply voltage for the GTX transmitter and receiver termination circuits relative to GND	–0.5	1.32	V
MGTAVTTRCAL	Analog supply voltage for the resistor calibration circuit of the GTX transceiver column	–0.5	1.32	V
V_{IN}	Receiver (RXP/RXN) and Transmitter (TXP/TXN) absolute input voltage	–0.5	1.32	V
$V_{MGTREFCLK}$	Reference clock absolute input voltage	–0.5	1.32	V

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.

Table 26 summarizes the DC specifications of the clock input of the GTX transceiver. Consult the *Virtex-6 FPGA GTX Transceivers User Guide* for further details.

Table 26: **GTX Transceiver Clock DC Input Level Specification**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{IDIFF}	Differential peak-to-peak input voltage		210	800	2000	mV
R_{IN}	Differential input resistance		90	100	130	Ω
C_{EXT}	Required external AC coupling capacitor		–	100	–	nF

GTX Transceiver Switching Characteristics

Consult *Virtex-6 FPGA GTX Transceivers User Guide* for further information.

Table 27: **GTX Transceiver Performance**

Symbol	Description	Speed Grade		Units
		-2	-1	
F_{GTXMAX}	Maximum GTX transceiver data rate	3.75	3.75	Gb/s
$F_{GPLLMAX}$	Maximum PLL frequency	2.5	2.5	GHz
$F_{GPLLMIN}$	Minimum PLL frequency	1.2	1.2	GHz

Table 28: **GTX Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics**

Symbol	Description	Speed Grade		Units
		-2	-1	
$F_{GTXDRPCLK}$	GTXDRPCLK maximum frequency	100	100	MHz

Table 29: **GTX Transceiver Reference Clock Switching Characteristics**

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
F_{GCLK}	Reference clock frequency range		67.5	–	375	MHz
T_{RCLK}	Reference clock rise time	20% – 80%	–	200	–	ps
T_{FCLK}	Reference clock fall time	80% – 20%	–	200	–	ps
T_{DCREF}	Reference clock duty cycle	Transceiver PLL only	45	50	55	%
T_{LOCK}	Clock recovery frequency acquisition time	Initial PLL lock	–	–	1	ms
T_{PHASE}	Clock recovery phase acquisition time	Lock to data after PLL has locked to the reference clock	–	–	200	µs

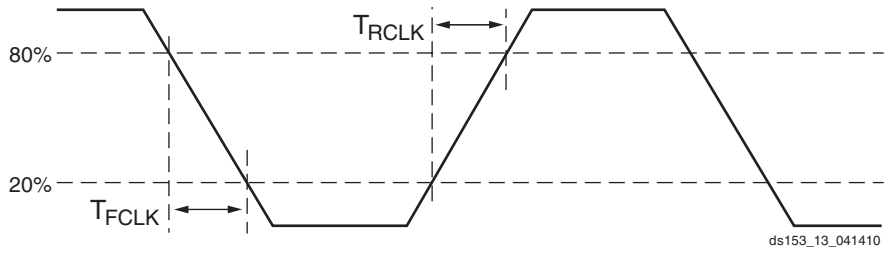

Figure 13: **Reference Clock Timing Parameters**

Table 30: **GTX Transceiver User Clock Switching Characteristics(1)**

Symbol	Description	Conditions	Speed Grade		Units
			-2	-1	
F_{TXOUT}	TXOUTCLK maximum frequency	Internal 20-bit data path	187.5	187.5	MHz
		Internal 16-bit data path	234.38	234.38	MHz
F_{RXREC}	RXRECCLK maximum frequency	Internal 20-bit data path	187.5	187.5	MHz
		Internal 16-bit data path	234.38	234.38	MHz
T_{RX}	RXUSRCLK maximum frequency		234.38	234.38	MHz
T_{RX2}	RXUSRCLK2 maximum frequency	1 byte interface	376	312.5	MHz
		2 byte interface	234.38	234.38	MHz
		4 byte interface	117.19	117.19	MHz
T_{TX}	TXUSRCLK maximum frequency		234.38	234.38	MHz
T_{TX2}	TXUSRCLK2 maximum frequency	1 byte interface	376	312.5	MHz
		2 byte interface	234.38	234.38	MHz
		4 byte interface	117.19	117.19	MHz

Notes:

1. Clocking must be implemented as described in *Virtex-6 FPGA GTX Transceivers User Guide*.

Table 31: **GTX Transceiver Transmitter Switching Characteristics**

Symbol	Description	Condition	Min	Typ	Max	Units
F_{GTXTX}	Serial data rate range		0.480	–	F_{GTXMAX}	Gb/s
T_{RTX}	TX Rise time	20%–80%	–	120	–	ps
T_{FTX}	TX Fall time	80%–20%	–	120	–	ps
T_{LLSKEW}	TX lane-to-lane skew(1)		–	–	350	ps
$V_{TXOOBVDPP}$	Electrical idle amplitude		–	–	15	mV
$T_{TXOOBTRANSITION}$	Electrical idle transition time		–	–	75	ns
$T_{J3.75}$	Total Jitter(2)(3)	3.75 Gb/s	–	–	0.34	UI
$D_{J3.75}$	Deterministic Jitter(2)(3)		–	–	0.16	UI
$T_{J3.125}$	Total Jitter(2)(3)	3.125 Gb/s	–	–	0.2	UI
$D_{J3.125}$	Deterministic Jitter(2)(3)		–	–	0.1	UI
$T_{J3.125L}$	Total Jitter(2)(3)	3.125 Gb/s(4)	–	–	0.35	UI
$D_{J3.125L}$	Deterministic Jitter(2)(3)		–	–	0.16	UI
$T_{J2.5}$	Total Jitter(2)(3)	2.5 Gb/s(5)	–	–	0.20	UI
$D_{J2.5}$	Deterministic Jitter(2)(3)		–	–	0.08	UI
$T_{J1.25}$	Total Jitter(2)(3)	1.25 Gb/s(6)	–	–	0.15	UI
$D_{J1.25}$	Deterministic Jitter(2)(3)		–	–	0.06	UI
T_{J600}	Total Jitter(2)(3)	600 Mb/s	–	–	0.1	UI
D_{J600}	Deterministic Jitter(2)(3)		–	–	0.03	UI

Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Virtex-6 CXT devices. The numbers reported here are worst-case values; they have all been fully characterized. These values are subject to the same guidelines as the Switching Characteristics, page 25.

Table 35: **Interface Performances**

Description	Speed Grade	
	-2	-1
Networking Applications		
SDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 8)	650 Mb/s	625 Mb/s
DDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 10)	1.25 Gb/s	1.0 Gb/s
SDR LVDS receiver (SFI-4.1)(1)	650 Mb/s	625 Mb/s
DDR LVDS receiver (SFI-4.2)(1)	1.0 Gb/s	0.9 Gb/s
Maximum Physical Interface (PHY) Rate for Memory Interfaces(2)(3)		
DDR2	666 Mb/s	666 Mb/s
DDR3	800 Mb/s	666 Mb/s
QDR II + SRAM	250 MHz	250 MHz

Notes:

1. LVDS receivers are typically bounded with certain applications where specific DPA algorithms dominate deterministic performance.
2. Based on Xilinx memory characterization platforms designed according to the guidelines in the *Virtex-6 FPGA Memory Interface Solutions User Guide*.
3. Consult the *Virtex-6 FPGA Memory Interface Solutions Data Sheet* for performance and feature information on memory interface cores (controller plus PHY).

Output Delay Measurements

Output delays are measured using a Tektronix P6245 TDS500/600 probe (< 1 pF) across approximately 4" of FR4 microstrip trace. Standard termination was used for all testing. The propagation delay of the 4" trace is characterized separately and subtracted from the final measurement, and is therefore not included in the generalized test setups shown in Figure 14 and Figure 15.

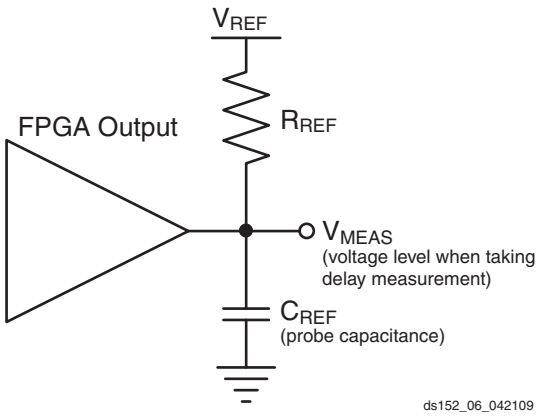

Figure 14: **Single Ended Test Setup**

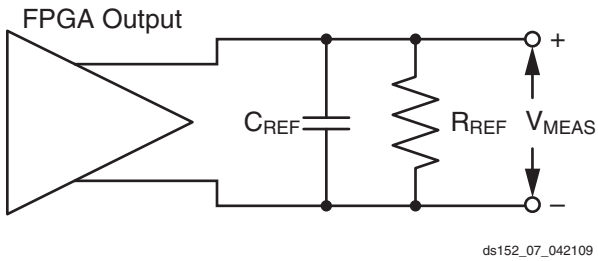

Figure 15: **Differential Test Setup**

Measurements and test conditions are reflected in the IBIS models except where the IBIS format precludes it. Parameters V_{REF}, R_{REF}, C_{REF}, and V_{MEAS} fully describe the test conditions for each I/O standard. The most accurate prediction of propagation delay in any given application can be obtained through IBIS simulation, using the following method:

1. Simulate the output driver of choice into the generalized test setup, using values from Table 41.
2. Record the time to V_{MEAS}.
3. Simulate the output driver of choice into the actual PCB trace and load, using the appropriate IBIS model or capacitance value to represent the load.
4. Record the time to V_{MEAS}.
5. Compare the results of steps 2 and 4. The increase or decrease in delay yields the actual propagation delay of the PCB trace.

Table 41: **Output Delay Measurement Methodology**

Description	I/O Standard Attribute	R_{REF} (Ω)	C_{REF} (1) (pF)	V_{MEAS} (V)	V_{REF} (V)
LVCMOS, 2.5V	LVCMOS25	1M	0	1.25	0
LVCMOS, 1.8V	LVCMOS18	1M	0	0.9	0
LVCMOS, 1.5V	LVCMOS15	1M	0	0.75	0
LVCMOS, 1.2V	LVCMOS12	1M	0	0.75	0
HSTL (High-Speed Transceiver Logic), Class I	HSTL_I	50	0	V_{REF}	0.75
HSTL, Class II	HSTL_II	25	0	V_{REF}	0.75
HSTL, Class III	HSTL_III	50	0	0.9	1.5
HSTL, Class I, 1.8V	HSTL_I_18	50	0	V_{REF}	0.9
HSTL, Class II, 1.8V	HSTL_II_18	25	0	V_{REF}	0.9
HSTL, Class III, 1.8V	HSTL_III_18	50	0	1.1	1.8
SSTL (Stub Series Terminated Logic), Class I, 1.8V	SSTL18_I	50	0	V_{REF}	0.9
SSTL, Class II, 1.8V	SSTL18_II	25	0	V_{REF}	0.9
SSTL, Class I, 2.5V	SSTL2_I	50	0	V_{REF}	1.25
SSTL, Class II, 2.5V	SSTL2_II	25	0	V_{REF}	1.25
LVDS (Low-Voltage Differential Signaling), 2.5V	LVDS_25	100	0	0 (2)	1.2
LVDSEXT (LVDS Extended Mode), 2.5V	LVDS_25	100	0	0 (2)	1.2
BLVDS (Bus LVDS), 2.5V	BLVDS_25	100	0	0 (2)	0

Table 41: **Output Delay Measurement Methodology *(Cont'd)***

Description	I/O Standard Attribute	R_{REF} (Ω)	C_{REF}[1] (pF)	V_{MEAS} (V)	V_{REF} (V)
HT (HyperTransport), 2.5V	LDT_25	100	0	0[2]	0.6
LVPECL (Low-Voltage Positive Emitter-Coupled Logic), 2.5V	LVPECL_25	100	0	0[2]	0
LVDCI/HSLVDCI, 2.5V	LVDCI_25, HSLVDCI_25	1M	0	1.25	0
LVDCI/HSLVDCI, 1.8V	LVDCI_18, HSLVDCI_18	1M	0	0.9	0
LVDCI/HSLVDCI, 1.5V	LVDCI_15, HSLVDCI_15	1M	0	0.75	0
HSTL (High-Speed Transceiver Logic), Class I & II, with DCI	HSTL_I_DCI, HSTL_II_DCI	50	0	V_{REF}	0.75
HSTL, Class III, with DCI	HSTL_III_DCI	50	0	0.9	1.5
HSTL, Class I & II, 1.8V, with DCI	HSTL_I_DCI_18, HSTL_II_DCI_18	50	0	V_{REF}	0.9
HSTL, Class III, 1.8V, with DCI	HSTL_III_DCI_18	50	0	1.1	1.8
SSTL (Stub Series Termi.Logic), Class I & II, 1.8V, with DCI	SSTL18_I_DCI, SSTL18_II_DCI	50	0	V_{REF}	0.9
SSTL, Class I & II, 2.5V, with DCI	SSTL2_I_DCI, SSTL2_II_DCI	50	0	V_{REF}	1.25

Notes:

1. C_{REF} is the capacitance of the probe, nominally 0 pF.
2. The value given is the differential output voltage.

Input/Output Logic Switching Characteristics

Table 42: **ILOGIC Switching Characteristics**

Symbol	Description	Speed Grade		Units
		-2	-1	
Setup/Hold				
T_{ICE1CK}/T_{ICKCE1}	CE1 pin Setup/Hold with respect to CLK	0.27/0.04	0.27/0.04	ns
T_{ISRCK}/T_{ICKSR}	SR pin Setup/Hold with respect to CLK	0.96/–0.10	0.96/–0.10	ns
T_{IDOCK}/T_{IOCKD}	D pin Setup/Hold with respect to CLK without Delay	0.10/0.54	0.10/0.54	ns
T_{IDOCKD}/T_{IOCKDD}	DDLY pin Setup/Hold with respect to CLK (using IODELAY)	0.14/0.42	0.14/0.40	ns
Combinatorial				
T_{IDI}	D pin to O pin propagation delay, no Delay	0.20	0.20	ns
T_{IDID}	DDLY pin to O pin propagation delay (using IODELAY)	0.25	0.25	ns
Sequential Delays				
T_{IDLO}	D pin to Q1 pin using flip-flop as a latch without Delay	0.64	0.64	ns
T_{IDLOD}	DDLY pin to Q1 pin using flip-flop as a latch (using IODELAY)	0.68	0.68	ns
T_{ICKQ}	CLK to Q outputs	0.71	0.71	ns
T_{RQ_ILOGIC}	SR pin to OQ/TQ out	1.15	1.15	ns
T_{GSRQ_ILOGIC}	Global Set/Reset to Q outputs	10.51	10.51	ns
Set/Reset				
T_{RPW_ILOGIC}	Minimum Pulse Width, SR inputs	1.20	1.20	ns, Min

Block RAM and FIFO Switching Characteristics

Table 50: **Block RAM and FIFO Switching Characteristics**

Symbol	Description	Speed Grade		Units
		-2	-1	
Block RAM and FIFO Clock-to-Out Delays				
T_{RCKO_DO} and $T_{RCKO\_DO\_REG}$[1]	Clock CLK to DOUT output (without output register)[2][3]	2.08	2.39	ns, Max
	Clock CLK to DOUT output (with output register)[4][5]	0.75	0.86	ns, Max
$T_{RCKO\_DO\_ECC}$ and $T_{RCKO\_DO\_ECC\_REG}$	Clock CLK to DOUT output with ECC (without output register)[2][3]	3.30	3.79	ns, Max
	Clock CLK to DOUT output with ECC (with output register)[4][5]	0.86	0.98	ns, Max
T_{RCKO_CASC} and $T_{RCKO\_CASC\_REG}$	Clock CLK to DOUT output with Cascade (without output register)[2]	3.18	3.65	ns, Max
	Clock CLK to DOUT output with Cascade (with output register)[4]	1.58	1.81	ns, Max
T_{RCKO_FLAGS}	Clock CLK to FIFO flags outputs[6]	0.91	1.05	ns, Max
$T_{RCKO\_POINTERS}$	Clock CLK to FIFO pointers outputs[7]	1.09	1.25	ns, Max
$T_{RCKO\_RDCOUNT}$	Clock CLK to FIFO Read Counter	1.09	1.25	ns, Max
$T_{RCKO\_WRCOUNT}$	Clock CLK to FIFO Write Counter	1.09	1.25	ns, Max
$T_{RCKO\_SDBIT\_ECC}$ and $T_{RCKO\_SDBIT\_ECC\_REG}$	Clock CLK to BITERR (with output register)	0.76	0.87	ns, Max
	Clock CLK to BITERR (without output register)	2.84	3.26	ns, Max
$T_{RCKO\_PARITY\_ECC}$	Clock CLK to ECCPARITY in ECC encode only mode	1.06	1.21	ns, Max
$T_{RCKO\_RDADDR\_ECC}$ and $T_{RCKO\_RDADDR\_ECC\_REG}$	Clock CLK to RDADDR output with ECC (without output register)	0.90	1.03	ns, Max
	Clock CLK to RDADDR output with ECC (with output register)	0.92	1.06	ns, Max
Setup and Hold Times Before/After Clock CLK				
$T_{RCCK\_ADDR}/T_{RCKC\_ADDR}$	ADDR inputs[8]	0.62/0.32	0.72/0.37	ns, Min
T_{RDCK_DI}/T_{RCKD_DI}	DIN inputs[9]	1.11/0.34	1.28/0.39	ns, Min
$T_{RDCK\_DI\_ECC}/T_{RCKD\_DI\_ECC}$	DIN inputs with block RAM ECC in standard mode[9]	0.59/0.34	0.68/0.39	ns, Min
	DIN inputs with block RAM ECC encode only[9]	0.85/0.34	0.97/0.39	ns, Min
	DIN inputs with FIFO ECC in standard mode[9]	1.02/0.34	1.17/0.39	ns, Min
$T_{RCCK\_CLK}/T_{RCKC\_CLK}$	Inject single/double bit error in ECC mode	1.20/0.29	1.38/0.33	ns, Min
$T_{RCCK\_RDEN}/T_{RCKC\_RDEN}$	Block RAM Enable (EN) input	0.41/0.30	0.47/0.34	ns, Min
$T_{RCCK\_REGCE}/T_{RCKC\_REGCE}$	CE input of output register	0.22/0.31	0.25/0.35	ns, Min
$T_{RCCK\_RSTREG}/T_{RCKC\_RSTREG}$	Synchronous RSTREG input	0.28/0.26	0.32/0.29	ns, Min
$T_{RCCK\_RSTRAM}/T_{RCKC\_RSTRAM}$	Synchronous RSTRAM input	0.41/0.27	0.47/0.31	ns, Min
T_{RCCK_WE}/T_{RCKC_WE}	Write Enable (WE) input (block RAM only)	0.52/0.35	0.60/0.40	ns, Min
$T_{RCCK\_WREN}/T_{RCKC\_WREN}$	WREN FIFO inputs	0.55/0.30	0.64/0.34	ns, Min
$T_{RCCK\_RDEN}/T_{RCKC\_RDEN}$	RDEN FIFO inputs	0.55/0.30	0.63/0.34	ns, Min
Reset Delays				
T_{RCO_FLAGS}	Reset RST to FIFO Flags/Pointers[10]	1.10	1.27	ns, Max
$T_{RCCK\_RSTREG}/T_{RCKC\_RSTREG}$	FIFO reset timing[11]	0.28/0.26	0.32/0.29	ns, Min

Table 51: **DSP48E1 Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade		Units
		-2	-1	
Clock to Outs from Input Register Clock to Cascading Output Pins				
$T_{DSPCKO\_\{ACOUT;\ BCOUT\}\_\{AREG;\ BREG\}}$	CLK (AREG, BREG) to {P, CARRYOUT} output	0.89	1.02	ns
$T_{DSPCKO\_\{PCOUT,\ CARRYCASCOUT,\ MULTSIGNOUT\}\_\{AREG,\ BREG\}\_MULT}$	CLK (AREG, BREG) to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output using multiplier	5.49	6.31	ns
$T_{DSPCKO\_\{PCOUT,\ CARRYCASCOUT,\ MULTSIGNOUT\}\_\{AREG,\ BREG\}}$	CLK (AREG, BREG) to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output not using multiplier	2.40	2.76	ns
$T_{DSPCKO\_\{PCOUT,\ CARRYCASCOUT,\ MULTSIGNOUT\}\_DREG\_MULT}$	CLK (DREG) to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output using multiplier	5.38	6.18	ns
$T_{DSPCKO\_\{PCOUT,\ CARRYCASCOUT,\ MULTSIGNOUT\}\_CREG}$	CLK (CREG) to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output	2.40	2.76	ns
Maximum Frequency				
F_{MAX}	With all registers used	350	275	MHz
F_{MAX_PATDET}	With pattern detector	350	275	MHz
$F_{MAX\_MULT\_NOMREG}$	Two register multiply without MREG	262	227	MHz
$F_{MAX\_MULT\_NOMREG\_PATDET}$	Two register multiply without MREG with pattern detect	241	209	MHz
$F_{MAX\_PREADD\_MULT\_NOADREG}$	Without ADREG	292	253	MHz
$F_{MAX\_PREADD\_MULT\_NOADREG\_PATDET}$	Without ADREG with pattern detect	292	253	MHz
$F_{MAX\_NOPIPELINEREG}$	Without pipeline registers (MREG, ADREG)	196	170	MHz
$F_{MAX\_NOPIPELINEREG\_PATDET}$	Without pipeline registers (MREG, ADREG) with pattern detect	184	160	MHz

Configuration Switching Characteristics

Table 52: **Configuration Switching Characteristics**

Symbol	Description	Speed Grade		Units
		-2	-1	
Power-up Timing Characteristics				
T_{PL} (1)	Program Latency	3	3	ms, Max
T_{POR} (1)	Power-on-Reset	15/55	15/55	ms, Min/Max
T_{ICCK}	CCLK (output) delay	400	400	ns, Min
$T_{PROGRAM}$	Program Pulse Width	250	250	ns, Min
Master/Slave Serial Mode Programming Switching (1)				
T_{DCCK}/T_{CCKD}	DIN Setup/Hold, slave mode	4.0/0.0	4.0/0.0	ns, Min
T_{DSCCK}/T_{SCCKD}	DIN Setup/Hold, master mode	4.0/0.0	4.0/0.0	ns, Min
T_{CCO}	DOUT at 2.5V	6	6	ns, Max
	DOUT at 1.8V	6	6	ns, Max
F_{MCCK}	Maximum CCLK frequency, serial modes	100	100	MHz, Max
$F_{MCCKTOL}$	Frequency Tolerance, master mode with respect to nominal CCLK	55	55	%
F_{MSCCK}	Slave mode external CCLK	100	100	MHz
SelectMAP Mode Programming Switching				
T_{SMDCCK}/T_{SMCCKD}	SelectMAP Data Setup/Hold	4.0/0.0	4.0/0.0	ns, Min
$T_{SMCSCCK}/T_{SMCCKCS}$	CSI_B Setup/Hold	4.0/0.0	4.0/0.0	ns, Min
T_{SMCCKW}/T_{SMWCCK}	RDWR_B Setup/Hold	10.0/0.0	10.0/0.0	ns, Min
$T_{SMCKCSO}$	CSO_B clock to out (330 Ω pull-up resistor required)	7	7	ns, Min
T_{SMCO}	CCLK to DATA out in readback at 2.5V	8	8	ns, Max
	CCLK to DATA out in readback at 1.8V	8	8	ns, Max
T_{SMCKBY}	CCLK to BUSY out in readback at 2.5V	6	6	ns, Max
	CCLK to BUSY out in readback at 1.8V	6	6	ns, Max
F_{SMCCK}	Maximum Frequency with respect to nominal CCLK	100	100	MHz, Max
F_{RBCCK}	Maximum Readback Frequency with respect to nominal CCLK	100	100	MHz, Max
$F_{MCCKTOL}$	Frequency Tolerance with respect to nominal CCLK	55	55	%
Boundary-Scan Port Timing Specifications				
T_{TAPTCK}/T_{TCKTAP}	TMS and TDI Setup time before TCK/ Hold time after TCK	3.0/2.0	3.0/2.0	ns, Min
T_{TCKTDO}	TCK falling edge to TDO output valid at 2.5V	6	6	ns, Max
	TCK falling edge to TDO output valid at 1.8V	6	6	ns, Max
F_{TCK}	Maximum configuration TCK clock frequency	66	66	MHz, Max
F_{TCKB_MIN}	Minimum boundary-scan TCK clock frequency when using IEEE Std 1149.6 (AC-JTAG). Minimum operating temperature for IEEE Std 1149.6 is 0°C.	15	15	MHz, Min
F_{TCKB}	Maximum boundary-scan TCK clock frequency	66	66	MHz, Max

Clock Buffers and Networks

Table 53: **Global Clock Switching Characteristics (Including BUFGCTRL)**

Symbol	Description	Speed Grade		Units
		-2	-1	
$T_{BCCCK\_CE}/T_{BCCKC\_CE}$(1)	CE pins Setup/Hold	0.16/0.00	0.16/0.00	ns
T_{BCCCK_S}/T_{BCCKC_S}(1)	S pins Setup/Hold	0.16/0.00	0.16/0.00	ns
T_{BCCKO_O}(2)	BUFGCTRL delay from I0/I1 to O	0.10	0.10	ns
Maximum Frequency				
F_{MAX}	Global clock tree (BUFG)	700	700	MHz

Notes:

1. T_{BCCCK_CE} and T_{BCCKC_CE} must be satisfied to assure glitch-free operation of the global clock when switching between clocks. These parameters do not apply to the BUFGMUX_VIRTEX4 primitive that assures glitch-free operation. The other global clock setup and hold times are optional; only needing to be satisfied if device operation requires simulation matches on a cycle-for-cycle basis when switching between clocks.
2. T_{BGCKO_O} (BUFG delay from I0 to O) values are the same as T_{BCCKO_O} values.

Table 54: **Input/Output Clock Switching Characteristics (BUFIO)**

Symbol	Description	Speed Grade		Units
		-2	-1	
T_{BIOCKO_O}	Clock to out delay from I to O	0.18	0.18	ns
Maximum Frequency				
F_{MAX}	I/O clock tree (BUFIO)	710	710	MHz

Table 55: **Regional Clock Switching Characteristics (BUFR)**

Symbol	Description	Speed Grade		Units
		-2	-1	
T_{BRCKO_O}	Clock to out delay from I to O	0.75	0.75	ns
		0.75	0.75	ns
		0.75	0.75	ns
		0.75	0.75	ns
$T_{BRCKO\_O\_BYP}$	Clock to out delay from I to O with Divide Bypass attribute set	0.37	0.37	ns
		0.37	0.37	ns
		0.37	0.37	ns
		0.37	0.37	ns
T_{BRDO_O}	Propagation delay from CLR to O	0.83	0.83	ns
Maximum Frequency				
F_{MAX}	Regional clock tree (BUFR)	300	300	MHz

Table 56: **Horizontal Clock Buffer Switching Characteristics (BUFH)**

Symbol	Description	Speed Grade		Units
		-2	-1	
T_{BHCKO_O}	BUFH delay from I to O	0.13	0.13	ns
$T_{BHCCK\_CE}/T_{BHCKC\_CE}$	CE pin Setup and Hold	0.05/0.05	0.05/0.05	ns
Maximum Frequency				
F_{MAX}	Horizontal clock buffer (BUFH)	700	700	MHz

MMCM Switching Characteristics

Table 57: **MMCM Specification**

Symbol	Description	Speed Grade		Units
		-2	-1	
F_{INMAX}	Maximum Input Clock Frequency(1)	700	700	MHz
F_{INMIN}	Minimum Input Clock Frequency	10	10	MHz
$F_{INJITTER}$	Maximum Input Clock Period Jitter	< 20% of clock input period or 1 ns Max		
F_{INDUTY}	Allowable Input Duty Cycle: 10—49 MHz	25/75		%
	Allowable Input Duty Cycle: 50—199 MHz	30/70		%
	Allowable Input Duty Cycle: 200—399 MHz	35/65		%
	Allowable Input Duty Cycle: 400—499 MHz	40/60		%
	Allowable Input Duty Cycle: >500 MHz	45/55		%
F_{MIN_PSCLK}	Minimum Dynamic Phase Shift Clock Frequency	0.01	0.01	MHz
F_{MAX_PSCLK}	Maximum Dynamic Phase Shift Clock Frequency	450	450	MHz
F_{VCOMIN}	Minimum MMCM VCO Frequency	600	600	MHz
F_{VCOMAX}	Maximum MMCM VCO Frequency	1200	1200	MHz
$F_{BANDWIDTH}$	Low MMCM Bandwidth at Typical(2)	1.00	1.00	MHz
	High MMCM Bandwidth at Typical(2)	4.00	4.00	MHz

Virtex-6 CXT Device Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. The representative values for typical pin locations and normal clock loading are listed in Table 61. Values are expressed in nanoseconds unless otherwise noted.

Table 61: **Global Clock Input Setup and Hold Without MMCM**

Symbol	Description	Device	Speed Grade		Units
			-2	-1	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard.(1)					
T_{PSFD}/ T_{PHFD}	Full Delay (Legacy Delay or Default Delay) Global Clock Input and IFF(2) without MMCM	XC6VCX75T	1.75/–0.01	1.75/–0.01	ns
		XC6VCX130T	1.88/–0.11	1.88/–0.11	ns
		XC6VCX195T	1.97/–0.14	1.97/–0.14	ns
		XC6VCX240T	1.97/–0.14	1.97/–0.14	ns

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input Flip-Flop or Latch.
3. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.

Table 62: **Global Clock Input Setup and Hold With MMCM**

Symbol	Description	Device	Speed Grade		Units
			-2	-1	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard.(1)					
$T_{PSMMCMGC}$/ $T_{PHMMCMGC}$	No Delay Global Clock Input and IFF(2) with MMCM	XC6VCX75T	1.72/–0.22	1.72/–0.22	ns
		XC6VCX130T	1.81/–0.21	1.81/–0.21	ns
		XC6VCX195T	1.82/–0.20	1.82/–0.20	ns
		XC6VCX240T	1.82/–0.20	1.82/–0.20	ns

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input Flip-Flop or Latch.
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 63: **Clock-Capable Clock Input Setup and Hold With MMCM**

Symbol	Description	Device	Speed Grade		Units
			-2	-1	
Input Setup and Hold Time Relative to Clock-capable Clock Input Signal for LVCMOS25 Standard.(1)					
$T_{PSMMCMCC}$/ $T_{PHMMCMCC}$	No Delay Clock-capable Clock Input and IFF(2) with MMCM	XC6VCX75T	1.86/–0.28	1.86/–0.28	ns
		XC6VCX130T	1.93/–0.28	1.93/–0.28	ns
		XC6VCX195T	1.96/–0.27	1.96/–0.27	ns
		XC6VCX240T	1.96/–0.27	1.96/–0.27	ns

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input Flip-Flop or Latch.
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Date	Version	Description of Revisions
06/08/10	1.2	Revised GTX Transceivers in CXT Devices, page 5. Added V_{FS} and revised the V_{IN} and V_{TS} values in Table 9, page 11. Added V_{FS} and note 6 to Table 10. Revised description of C_{IN} in Table 11, including adding note 3. Updated Table 13 including adding note 2. Removed DIFF SSTL15 and added values to SSTL15 in Table 15. Updated Table 16 through Table 19. Added eFUSE Read Endurance section. Updated entire GTX Transceivers in CXT Devices section. Changed specifications of PCI Express in Table 34. In Table 35, removed RLDRAM II and revised and added values to other interface performance specifications. Updated speed specification to v1.04 with appropriate changes to Table 36. Revised the IOB switching characteristics in Table 38. Updated values in Table 39 and note 4 in Table 41. ILOGIC (Table 42), OLOGIC (Table 43), ISERDES (Table 44), and OSERDES (Table 45) switching characteristics changes. Revised $T_{IODELAY\_CLK\_MAX}$ and $T_{IDELAYPAT\_JIT}$ in Table 46. Revised CLB switching characteristics and added T_{SHCKO} to Table 47and revised CLB switching characteristics in Table 48 and Table 49. In Table 50, removed $T_{RCKO\_RDCOUNT}$ and $T_{RCKO\_WRCOUNT}$, removed $T_{RCKO\_PARITY\_ECC}$: Clock CLK to ECCPARITY in standard ECC mode, revised $T_{RDCK\_DI\_ECC}$/$T_{RCKD\_DI\_ECC}$, $T_{RCKO\_POINTERS}$, and revised F_{MAX} and $F_{MAX\_CASCADE}$ switching characteristics. Multiple changes to configuration specifications in Table 52. Revised switching characteristics and global clock tree (BUFG) F_{MAX} in Table 53. Revised switching characteristics and I/O clock tree (BUFIO) F_{MAX} in Table 54. Added note 1 to Table 55. Revised the F_{MAX} horizontal clock tree (BUFH) in Table 56. Multiple changes to MMCM specifications in Table 57 including F_{INMAX} and F_{OUTMAX}. Updated switching characteristics in Table 58 through Table 63. Removed T_{DCD_BUFH} and $T_{BUFHSKEW}$ from Table 64.
06/30/10	1.3	Production release of XC6VCX130T and XC6VCX240T in Table 36 and Table 37. Updated -1 speed grade SDR values in Table 35. Updated BUFIO F_{MAX} specification in Table 54. Added Note 6 to Table 57.
07/28/10	1.4	Production release of XC6VCX75T and XC6VCX195T in Table 36 and Table 37 using ISE 12.2 software with speed file v1.06 using the *Speed File Patch*. Updated PCI compliance on page 1. Added values to Table 13. In Table 25, update $V_{CMOUTDC}$ equation to MGTAVTT – DV_{PPOUT}/4. Updated F_{MAX} in Table 53, Table 54, and Table 56. Updated F_{INMAX} and F_{OUTMAX} in Table 57. Updated values in Table 61, Table 62, and Table 63.
10/14/10	1.5	Moved data sheet to Production status on the first page. Updated speed file with ISE 12.3 software with speed file v1.08 using the *Speed File Patch.* In Table 51, updated values for $T_{DSPCKO\_\{PCOUT,}$ CARRYCASCOUT, MULTSIGNOUT}_PREG.
02/11/11	1.6	Updated Table 10 to include the industrial range specifications. Added Note 12 to Table 50. Revised T_{BPICCO} values in Table 52. Updated range description for F_{INDUTY} in Table 57 and added note 8. The following revisions are due to specification changes as described in XCN11009, *Virtex-6 FPGA: Data Sheet, User Guides, and JTAG ID Updates*. In Table 52, updated the values for T_{SMCCKW}, T_{SPIDCC}, T_{SPICCM}, and $T_{SPICCFC}$. In Table 57: MMCM Specification, added bandwidth settings to F_{PFDMIN} and added note 1.