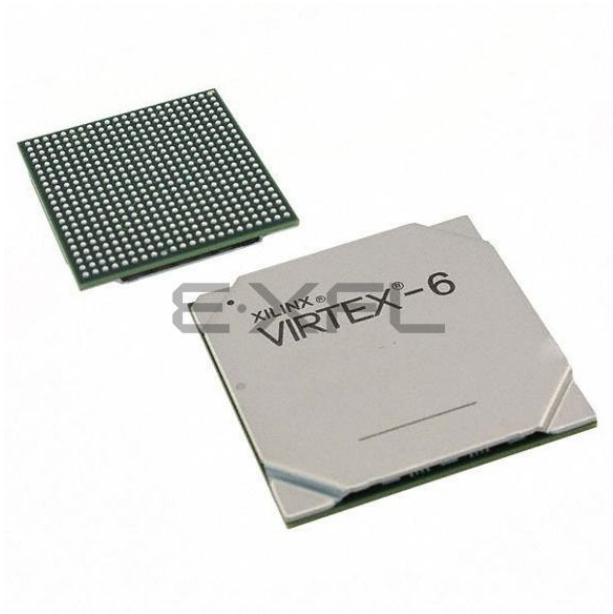
# AMD Xilinx - XC6VCX240T-1FFG784I Datasheet

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 18840 |
| Number of Logic Elements/Cells | 241152 |
| Total RAM Bits | 15335424 |
| Number of I/O | 400 |
| Number of Gates | - |
| Voltage - Supply | 0.95V ~ 1.05V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 784-BBGA, FCBGA |
| Supplier Device Package | 784-FCBGA (29x29) |
| Purchase URL | https://www.e-xfl.com/product-detail/xilinx/xc6vcx240t-1ffg784i |

## Virtex-6 CXT FPGA Documentation

In addition to the data sheet information found herein, complete and up-to-date documentation of the Virtex-6 family of FPGAs is available on the Xilinx website and available for download:

***Virtex-6 FPGA Configuration Guide*** **(UG360)**

This all-encompassing configuration guide includes chapters on configuration interfaces (serial and parallel), multi-bitstream management, bitstream encryption, boundary-scan and JTAG configuration, and reconfiguration techniques.

***Virtex-6 FPGA SelectIO Resources User Guide*** **(UG361)**

This guide describes the SelectIO™ resources available in all the Virtex-6 CXT devices.

***Virtex-6 FPGA Clocking Resources User Guide*** **(UG362)**

This guide describes the clocking resources available in all the Virtex-6 CXT devices, including the MMCM and clock buffers.

***Virtex-6 FPGA Memory Resources User Guide*** **(UG363)**

This guide describes the Virtex-6 CXT device block RAM and FIFO capabilities.

***Virtex-6 FPGA CLB User Guide*** **(UG364)**

This guide describes the capabilities of the configurable logic blocks (CLB) available in all Virtex-6 CXT devices.

***Virtex-6 FPGA DSP48E1 Slice User Guide*** **(UG369)**

This guide describes the architecture of the DSP48E1 slice in Virtex-6 CXT FPGAs and provides configuration examples.

***Virtex-6 FPGA GTX Transceivers User Guide*** **(UG366)**

This guide describes the GTX transceivers available in all the Virtex-6 CXT FPGAs.

***Virtex-6 FPGA Tri-Mode Ethernet MAC User Guide*** **(UG368)**

This guide describes the dedicated tri-mode Ethernet media access controller (TEMAC) available in all the Virtex-6 CXT FPGAs.

***Virtex-6 FPGA Data Sheet: DC and Switching Characteristics*** **(DS152)**

Reference this data sheet when considering device migration to the Virtex-6 LXT and SXT families. It contains the DC and Switching Characteristic specifications specifically for the Virtex-6 LXT and SXT families.

***Virtex-6 FPGA Packaging and Pinout Specifications*** **(UG365)**

These specifications includes the tables for device/package combinations and maximum I/Os, pin definitions, pinout tables, pinout diagrams, mechanical drawings, and thermal specifications of the Virtex-6 LXT and SXT families. Reference these specifications when considering device migration to the Virtex-6 LXT and SXT families.

## Configuration Bitstream Overview for CXT Devices

This section contains two tables similar to those in the *Virtex-6 FPGA Configuration Guide* only updated for the CXT family. The Virtex-6 CXT FPGA bitstream contains commands to the FPGA configuration logic as well as configuration data. Table 3 gives a typical bitstream length and Table 4 gives the specific device ID codes for the Virtex-6 CXT devices.

*Table 3:* **Virtex-6 CXT FPGA Bitstream Length**

| Device | Total Number of Configuration Bits |
|---|---|
| XC6VCX75T | 26,239,328 |
| XC6VCX130T | 43,719,776 |
| XC6VCX195T | 61,552,736 |
| XC6VCX240T | 73,859,552 |

*Table 4:* **Virtex-6 CXT FPGA Device ID Codes**

| Device | ID Code (Hex) |
|---|---|
| XC6VCX75T | 0x042C4093 |
| XC6VCX130T | 0x042CA093 |
| XC6VCX195T | 0x042CC093 |
| XC6VCX240T | 0x042D0093 |

## CLB Overview for CXT Devices

Table 5, updated specifically for the CXT family from a similar table in the *Virtex-6 FPGA CLB User Guide*, shows the available resources in all Virtex-6 CXT FPGA CLBs.

*Table 5:* **Virtex-6 CXT FPGA Logic Resources Available in All CLBs**

| Device | Total Slices | SLICELs | SLICEMs | Number of 6-Input LUTs | Maximum Distributed RAM (Kb) | Shift Register (Kb) | Number of Flip-Flops |
|---|---|---|---|---|---|---|---|
| XC6VCX75T | 11,640 | 7,460 | 4,180 | 46,560 | 1045 | 522.5 | 93,120 |
| XC6VCX130T | 20,000 | 13,040 | 6,960 | 80,000 | 1740 | 870 | 160,000 |
| XC6VCX195T | 31,200 | 19,040 | 12,160 | 124,800 | 3140 | 1570 | 249,600 |
| XC6VCX240T | 37,680 | 23,080 | 14,600 | 150,720 | 3770 | 1885 | 301,440 |

## Regional Clock Management for CXT Devices

Table 6, updated from the *Virtex-6 FPGA Clocking Resources User Guide* specifically for the CXT family, shows the number of clock regions in all Virtex-6 CXT FPGA CLBs.

*Table 6:* **Virtex-6 CXT FPGA Clock Regions**

| Device | Number of Clock Regions |
|---|---|
| XC6VCX75T | 6 |
| XC6VCX130T | 10 |
| XC6VCX195T | 10 |
| XC6VCX240T | 12 |

## CXT Packaging Specifications

Table 7, updated from the *Virtex-6 FPGA Packaging and Pinout Specifications* specifically for the CXT family, shows the number of GTX transceiver I/O channels. Table 8 shows the number of available I/Os and the number of differential I/O pairs for each Virtex-6 device/package combination.

*Table 7:* **Number of Serial Transceivers (GTs) I/O Channels/Device**

| I/O Channels | Device | | | |
|---|---|---|---|---|
| | CX75T(1) | CX130T(2) | CX195T(3) | CX240T(4) |
| MGTRXP | 8 or 12 | 8, 12, or 16 | 12 or 16 | 12 or 16 |
| MGTRXN | 8 or 12 | 8, 12, or 16 | 12 or 16 | 12 or 16 |
| MGTTXP | 8 or 12 | 8, 12, or 16 | 12 or 16 | 12 or 16 |
| MGTTXN | 8 or 12 | 8, 12, or 16 | 12 or 16 | 12 or 16 |

**Notes:**

1. The XC6VCX75T has 8 GTX I/O channels in the FF484/FFG484 package and 12 GTX I/O channels in the FF784/FFG784 package.
2. The XC6VCX130T has 8 GTX I/O channels in the FF484/FFG484 package, 12 GTX I/O channels in the FF784/FFG784 package, and 16 GTX I/O channels in the FF1156/FFG1156 package.
3. The XC6VCX195T has 12 GTX I/O channels in the FF784/FFG784 package and 16 GTX I/O channels in the FF1156/FFG1156 package.
4. The XC6VCX240T has 12 GTX I/O channels in the FF784/FFG784 package and 16 GTX I/O channels in the FF1156/FFG1156 package.

*Table 8:* **Available I/O Pin/Device/Package Combinations**

| Virtex-6 CXT Device | User I/O Pins | Virtex-6 CXT FPGA Package | | |
|---|---|---|---|---|
| | | FF484 | FF784 | FF1156 |
| XC6VCX75T | Available User I/Os | 240 | 360 | – |
| | Differential I/O Pairs | 120 | 180 | – |
| XC6VCX130T | Available User I/Os | 240 | 400 | 600 |
| | Differential I/O Pairs | 120 | 200 | 300 |
| XC6VCX195T | Available User I/Os | – | 400 | 600 |
| | Differential I/O Pairs | – | 200 | 300 |
| XC6VCX240T | Available User I/Os | – | 400 | 600 |
| | Differential I/O Pairs | – | 200 | 300 |

## GTX Transceivers in CXT Devices

CXT devices have between 8 to 16 gigabit transceiver circuits. Each GTX transceiver is a combined transmitter and receiver capable of operating at a data rate between 480 Mb/s and 3.75 Gb/s. Lower data rates can be achieved using FPGA logic-based oversampling. The transmitter and receiver are independent circuits that use separate PLLs to multiply the reference frequency input by certain programmable numbers between 2 and 25, to become the bit-serial data clock. Each GTX transceiver has a large number of user-definable features and parameters. All of these can be defined during device configuration, and many can also be modified during operation.

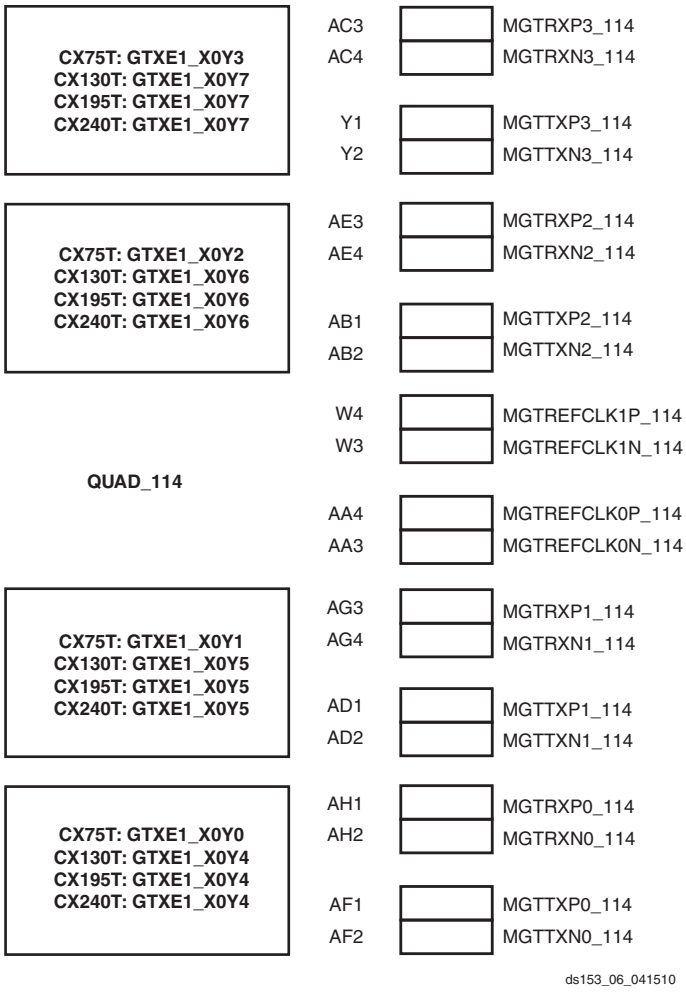


*Figure 6:* **Placement Diagram for the FF784 Package (3 of 3)**

## FF1156 Package Placement Diagrams

Figure 7 through Figure 10 show the placement diagrams for the GTX transceivers in the FF1156 package.

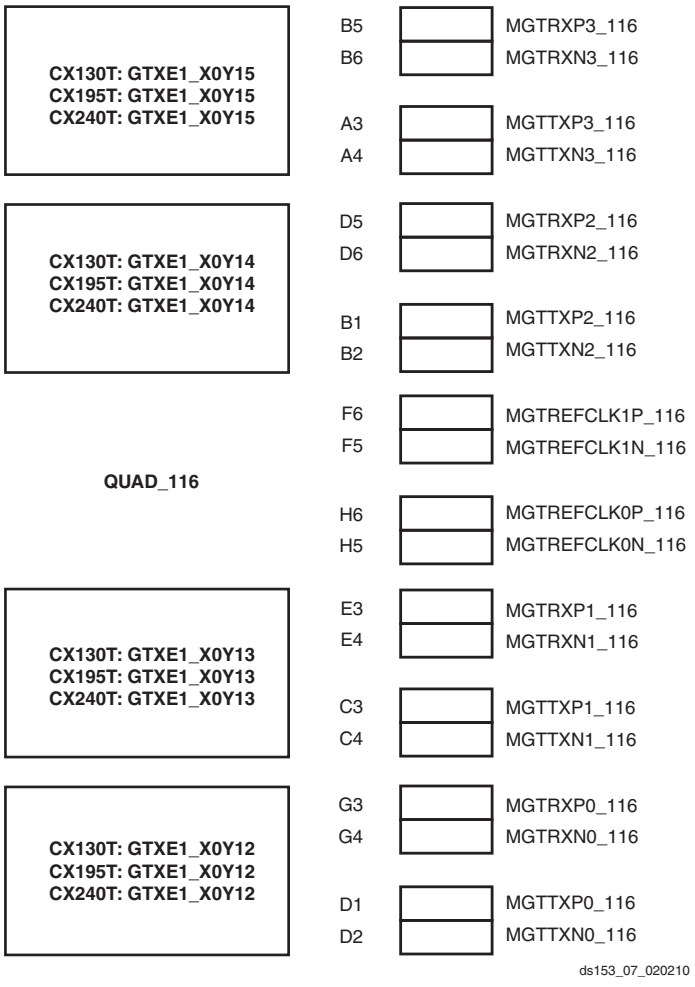


*Figure 7:* **Placement Diagram for the FF1156 Package (1 of 4)**

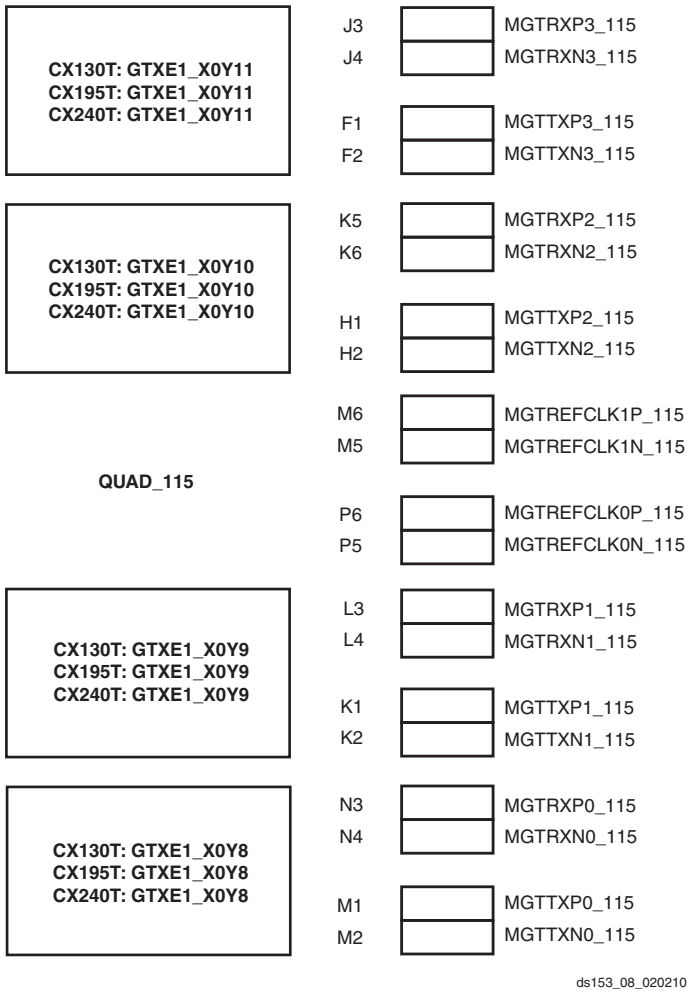


*Figure 8:* **Placement Diagram for the FF1156 Package (2 of 4)**

## SelectIO™ DC Input and Output Levels

Values for $V_{IL}$ and $V_{IH}$ are recommended input voltages. Values for $I_{OL}$ and $I_{OH}$ are guaranteed over the recommended operating conditions at the $V_{OL}$ and $V_{OH}$ test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum $V_{CCO}$ with the respective $V_{OL}$ and $V_{OH}$ voltage levels shown. Other standards are sample tested.

*Table 15:* **SelectIO DC Input and Output Levels**

| I/O Standard | $V_{IL}$ | | $V_{IH}$ | | $V_{OL}$ | $V_{OH}$ | $I_{OL}$ | $I_{OH}$ |
|---|---|---|---|---|---|---|---|---|
| | V, Min | V, Max | V, Min | V, Max | V, Max | V, Min | mA | mA |
| LVCMOS25, LVDCI25 | –0.3 | 0.7 | 1.7 | $V_{CCO}$ + 0.3 | 0.4 | $V_{CCO}$ – 0.4 | Note(3) | Note(3) |
| LVCMOS18, LVDCI18 | –0.3 | 35% $V_{CCO}$ | 65% $V_{CCO}$ | $V_{CCO}$ + 0.3 | 0.45 | $V_{CCO}$ – 0.45 | Note(4) | Note(4) |
| LVCMOS15, LVDCI15 | –0.3 | 35% $V_{CCO}$ | 65% $V_{CCO}$ | $V_{CCO}$ + 0.3 | 25% $V_{CCO}$ | 75% $V_{CCO}$ | Note(4) | Note(4) |
| LVCMOS12 | –0.3 | 35% $V_{CCO}$ | 65% $V_{CCO}$ | $V_{CCO}$ + 0.3 | 25% $V_{CCO}$ | 75% $V_{CCO}$ | Note(5) | Note(5) |
| HSTL I_12 | –0.3 | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | $V_{CCO}$ + 0.3 | 25% $V_{CCO}$ | 75% $V_{CCO}$ | 6.3 | 6.3 |
| HSTL I(2) | –0.3 | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | $V_{CCO}$ + 0.3 | 0.4 | $V_{CCO}$ – 0.4 | 8 | –8 |
| HSTL II(2) | –0.3 | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | $V_{CCO}$ + 0.3 | 0.4 | $V_{CCO}$ – 0.4 | 16 | –16 |
| HSTL III(2) | –0.3 | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | $V_{CCO}$ + 0.3 | 0.4 | $V_{CCO}$ – 0.4 | 24 | –8 |
| DIFF HSTL I(2) | –0.3 | 50% $V_{CCO}$ – 0.1 | 50% $V_{CCO}$ + 0.1 | $V_{CCO}$ + 0.3 | – | – | – | – |
| DIFF HSTL II(2) | –0.3 | 50% $V_{CCO}$ – 0.1 | 50% $V_{CCO}$ + 0.1 | $V_{CCO}$ + 0.3 | – | – | – | – |
| SSTL2 I | –0.3 | $V_{REF}$ – 0.15 | $V_{REF}$ + 0.15 | $V_{CCO}$ + 0.3 | $V_{TT}$ – 0.61 | $V_{TT}$ + 0.61 | 8.1 | –8.1 |
| SSTL2 II | –0.3 | $V_{REF}$ – 0.15 | $V_{REF}$ + 0.15 | $V_{CCO}$ + 0.3 | $V_{TT}$ – 0.81 | $V_{TT}$ + 0.81 | 16.2 | –16.2 |
| DIFF SSTL2 I | –0.3 | 50% $V_{CCO}$ – 0.15 | 50% $V_{CCO}$ + 0.15 | $V_{CCO}$ + 0.3 | – | – | – | – |
| DIFF SSTL2 II | –0.3 | 50% $V_{CCO}$ – 0.15 | 50% $V_{CCO}$ + 0.15 | $V_{CCO}$ + 0.3 | – | – | – | – |
| SSTL18 I | –0.3 | $V_{REF}$ – 0.125 | $V_{REF}$ + 0.125 | $V_{CCO}$ + 0.3 | $V_{TT}$ – 0.47 | $V_{TT}$ + 0.47 | 6.7 | –6.7 |
| SSTL18 II | –0.3 | $V_{REF}$ – 0.125 | $V_{REF}$ + 0.125 | $V_{CCO}$ + 0.3 | $V_{TT}$ – 0.60 | $V_{TT}$ + 0.60 | 13.4 | –13.4 |
| DIFF SSTL18 I | –0.3 | 50% $V_{CCO}$ – 0.125 | 50% $V_{CCO}$ + 0.125 | $V_{CCO}$ + 0.3 | – | – | – | – |
| DIFF SSTL18 II | –0.3 | 50% $V_{CCO}$ – 0.125 | 50% $V_{CCO}$ + 0.125 | $V_{CCO}$ + 0.3 | – | – | – | – |
| SSTL15 | –0.3 | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | $V_{CCO}$ + 0.3 | $V_{TT}$ – 0.175 | $V_{TT}$ + 0.175 | 14.3 | 14.3 |

**Notes:**

1. Tested according to relevant specifications.
2. Applies to both 1.5V and 1.8V HSTL.
3. Using drive strengths of 2, 4, 6, 8, 12, 16, or 24 mA.
4. Using drive strengths of 2, 4, 6, 8, 12, or 16 mA.
5. Supported drive strengths of 2, 4, 6, or 8 mA.
6. For detailed interface specific DC voltage levels, see the *Virtex-6 FPGA SelectIO Resources User Guide*.

## HT DC Specifications (HT_25)

*Table 16:* **HT DC Specifications**

| Symbol | DC Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{CCO}$ | Supply Voltage | | 2.38 | 2.5 | 2.63 | V |
| $V_{OD}$ | Differential Output Voltage | $R_T$ = 100 Ω across Q and $\overline{Q}$ signals | 480 | 600 | 885 | mV |
| $\Delta V_{OD}$ | Change in $V_{OD}$ Magnitude | | –15 | – | 15 | mV |
| $V_{OCM}$ | Output Common Mode Voltage | $R_T$ = 100 Ω across Q and $\overline{Q}$ signals | 480 | 600 | 885 | mV |
| $\Delta V_{OCM}$ | Change in $V_{OCM}$ Magnitude | | –15 | – | 15 | mV |
| $V_{ID}$ | Input Differential Voltage | | 200 | 600 | 1000 | mV |
| $\Delta V_{ID}$ | Change in $V_{ID}$ Magnitude | | –15 | – | 15 | mV |
| $V_{ICM}$ | Input Common Mode Voltage | | 440 | 600 | 780 | mV |
| $\Delta V_{ICM}$ | Change in $V_{ICM}$ Magnitude | | –15 | – | 15 | mV |

## LVDS DC Specifications (LVDS_25)

*Table 17:* **LVDS DC Specifications**

| Symbol | DC Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{CCO}$ | Supply Voltage | | 2.38 | 2.5 | 2.63 | V |
| $V_{OH}$ | Output High Voltage for Q and $\overline{Q}$ | $R_T$ = 100 Ω across Q and $\overline{Q}$ signals | – | – | 1.675 | V |
| $V_{OL}$ | Output Low Voltage for Q and $\overline{Q}$ | $R_T$ = 100 Ω across Q and $\overline{Q}$ signals | 0.825 | – | – | V |
| $V_{ODIFF}$ | Differential Output Voltage (Q – $\overline{Q}$), Q = High (($\overline{Q}$ – Q), $\overline{Q}$ = High | $R_T$ = 100 Ω across Q and $\overline{Q}$ signals | 247 | 350 | 600 | mV |
| $V_{OCM}$ | Output Common-Mode Voltage | $R_T$ = 100 Ω across Q and $\overline{Q}$ signals | 1.075 | 1.250 | 1.425 | V |
| $V_{IDIFF}$ | Differential Input Voltage (Q – $\overline{Q}$), Q = High (($\overline{Q}$ – Q), $\overline{Q}$ = High | | 100 | 350 | 600 | mV |
| $V_{ICM}$ | Input Common-Mode Voltage | | 0.3 | 1.2 | 2.2 | V |

## Extended LVDS DC Specifications (LVDSEXT_25)

*Table 18:* **Extended LVDS DC Specifications**

| Symbol | DC Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{CCO}$ | Supply Voltage | | 2.38 | 2.5 | 2.63 | V |
| $V_{OH}$ | Output High Voltage for Q and $\overline{Q}$ | $R_T$ = 100 Ω across Q and $\overline{Q}$ signals | – | – | 1.785 | V |
| $V_{OL}$ | Output Low Voltage for Q and $\overline{Q}$ | $R_T$ = 100 Ω across Q and $\overline{Q}$ signals | 0.715 | – | – | V |
| $V_{ODIFF}$ | Differential Output Voltage (Q – $\overline{Q}$), Q = High (($\overline{Q}$ – Q), $\overline{Q}$ = High | $R_T$ = 100 Ω across Q and $\overline{Q}$ signals | 350 | – | 840 | mV |
| $V_{OCM}$ | Output Common-Mode Voltage | $R_T$ = 100 Ω across Q and $\overline{Q}$ signals | 1.075 | 1.250 | 1.425 | V |
| $V_{IDIFF}$ | Differential Input Voltage (Q – $\overline{Q}$), Q = High (($\overline{Q}$ – Q), $\overline{Q}$ = High | Common-mode input voltage = 1.25V | 100 | – | 1000 | mV |
| $V_{ICM}$ | Input Common-Mode Voltage | Differential input voltage = ±350 mV | 0.3 | 1.2 | 2.2 | V |

*Table 30:* **GTX Transceiver User Clock Switching Characteristics(1)**

| Symbol | Description | Conditions | Speed Grade | | Units |
|---|---|---|---|---|---|
| | | | -2 | -1 | |
| $F_{TXOUT}$ | TXOUTCLK maximum frequency | Internal 20-bit data path | 187.5 | 187.5 | MHz |
| | | Internal 16-bit data path | 234.38 | 234.38 | MHz |
| $F_{RXREC}$ | RXRECCLK maximum frequency | Internal 20-bit data path | 187.5 | 187.5 | MHz |
| | | Internal 16-bit data path | 234.38 | 234.38 | MHz |
| $T_{RX}$ | RXUSRCLK maximum frequency | | 234.38 | 234.38 | MHz |
| $T_{RX2}$ | RXUSRCLK2 maximum frequency | 1 byte interface | 376 | 312.5 | MHz |
| | | 2 byte interface | 234.38 | 234.38 | MHz |
| | | 4 byte interface | 117.19 | 117.19 | MHz |
| $T_{TX}$ | TXUSRCLK maximum frequency | | 234.38 | 234.38 | MHz |
| $T_{TX2}$ | TXUSRCLK2 maximum frequency | 1 byte interface | 376 | 312.5 | MHz |
| | | 2 byte interface | 234.38 | 234.38 | MHz |
| | | 4 byte interface | 117.19 | 117.19 | MHz |

**Notes:**

1. Clocking must be implemented as described in *Virtex-6 FPGA GTX Transceivers User Guide*.

*Table 31:* **GTX Transceiver Transmitter Switching Characteristics**

| Symbol | Description | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $F_{GTXTX}$ | Serial data rate range | | 0.480 | – | $F_{GTXMAX}$ | Gb/s |
| $T_{RTX}$ | TX Rise time | 20%–80% | – | 120 | – | ps |
| $T_{FTX}$ | TX Fall time | 80%–20% | – | 120 | – | ps |
| $T_{LLSKEW}$ | TX lane-to-lane skew(1) | | – | – | 350 | ps |
| $V_{TXOOBVDPP}$ | Electrical idle amplitude | | – | – | 15 | mV |
| $T_{TXOOBTRANSITION}$ | Electrical idle transition time | | – | – | 75 | ns |
| $T_{J3.75}$ | Total Jitter(2)(3) | 3.75 Gb/s | – | – | 0.34 | UI |
| $D_{J3.75}$ | Deterministic Jitter(2)(3) | | – | – | 0.16 | UI |
| $T_{J3.125}$ | Total Jitter(2)(3) | 3.125 Gb/s | – | – | 0.2 | UI |
| $D_{J3.125}$ | Deterministic Jitter(2)(3) | | – | – | 0.1 | UI |
| $T_{J3.125L}$ | Total Jitter(2)(3) | 3.125 Gb/s(4) | – | – | 0.35 | UI |
| $D_{J3.125L}$ | Deterministic Jitter(2)(3) | | – | – | 0.16 | UI |
| $T_{J2.5}$ | Total Jitter(2)(3) | 2.5 Gb/s(5) | – | – | 0.20 | UI |
| $D_{J2.5}$ | Deterministic Jitter(2)(3) | | – | – | 0.08 | UI |
| $T_{J1.25}$ | Total Jitter(2)(3) | 1.25 Gb/s(6) | – | – | 0.15 | UI |
| $D_{J1.25}$ | Deterministic Jitter(2)(3) | | – | – | 0.06 | UI |
| $T_{J600}$ | Total Jitter(2)(3) | 600 Mb/s | – | – | 0.1 | UI |
| $D_{J600}$ | Deterministic Jitter(2)(3) | | – | – | 0.03 | UI |

## Ethernet MAC Switching Characteristics

Consult *Virtex-6 FPGA Embedded Tri-mode Ethernet MAC User Guide* for further information.

*Table 33:* **Maximum Ethernet MAC Performance**

| Symbol | Description | Conditions | Speed Grade | | Units |
|---|---|---|---|---|---|
| | | | -2 | -1 | |
| $F_{TEMACCLIENT}$ | Client interface maximum frequency | 10 Mb/s – 8-bit width | 2.5(1) | 2.5(1) | MHz |
| | | 100 Mb/s – 8-bit width | 25(2) | 25(2) | MHz |
| | | 1000 Mb/s – 8-bit width | 125 | 125 | MHz |
| | | 1000 Mb/s – 16-bit width | 62.5 | 62.5 | MHz |
| $F_{TEMACPHY}$ | Physical interface maximum frequency | 10 Mb/s – 4-bit width | 2.5 | 2.5 | MHz |
| | | 100 Mb/s – 4-bit width | 25 | 25 | MHz |
| | | 1000 Mb/s – 8-bit width | 125 | 125 | MHz |

**Notes:**

1. When not using clock enable, the $F_{MAX}$ is lowered to 1.25 MHz.
2. When not using clock enable, the $F_{MAX}$ is lowered to 12.5 MHz.

## Integrated Interface Block for PCI Express Designs Switching Characteristics

More information and documentation on solutions for PCI Express designs can be found at:
http://www.xilinx.com/technology/protocols/pciexpress.htm

*Table 34:* **Maximum Performance for PCI Express Designs**

| Symbol | Description | Speed Grade | | Units |
|---|---|---|---|---|
| | | -2 | -1 | |
| $F_{PIPECLK}$ | Pipe clock maximum frequency | 125 | 125 | MHz |
| $F_{USERCLK}$ | User clock maximum frequency | 250 | 250 | MHz |
| $F_{DRPCLK}$ | DRP clock maximum frequency | 250 | 250 | MHz |

## IOB Pad Input/Output/3-State Switching Characteristics

Table 38 summarizes the values of standard-specific data input delay adjustments, output delays terminating at pads (based on standard) and 3-state delays.

$T_{IOPI}$ is described as the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.

$T_{IOOP}$ is described as the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.

$T_{IOTP}$ is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer.

Table 39 summarizes the value of $T_{IOTPHZ}$. $T_{IOTPHZ}$ is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is enabled (i.e., a high impedance state).

*Table 38:* **IOB Switching Characteristics**

| I/O Standard | $T_{IOPI}$ | | $T_{IOOP}$ | | $T_{IOTP}$ | | Units |
|---|---|---|---|---|---|---|---|
| | Speed Grade | | Speed Grade | | Speed Grade | | |
| | -2 | -1 | -2 | -1 | -2 | -1 | |
| LVDS_25 | 1.09 | 1.09 | 1.68 | 1.68 | 1.68 | 1.68 | ns |
| LVDSEXT_25 | 1.09 | 1.09 | 1.84 | 1.84 | 1.84 | 1.84 | ns |
| HT_25 | 1.09 | 1.09 | 1.78 | 1.78 | 1.78 | 1.78 | ns |
| BLVDS_25 | 1.09 | 1.09 | 1.67 | 1.67 | 1.67 | 1.67 | ns |
| RSDS_25 (point to point) | 1.09 | 1.09 | 1.68 | 1.68 | 1.68 | 1.68 | ns |
| HSTL_I | 1.06 | 1.06 | 1.73 | 1.73 | 1.73 | 1.73 | ns |
| HSTL_II | 1.06 | 1.06 | 1.74 | 1.74 | 1.74 | 1.74 | ns |
| HSTL_III | 1.06 | 1.06 | 1.71 | 1.71 | 1.71 | 1.71 | ns |
| HSTL_I_18 | 1.06 | 1.06 | 1.75 | 1.75 | 1.75 | 1.75 | ns |
| HSTL_II_18 | 1.06 | 1.06 | 1.81 | 1.81 | 1.81 | 1.81 | ns |
| HSTL_III_18 | 1.06 | 1.06 | 1.71 | 1.71 | 1.71 | 1.71 | ns |
| SSTL2_I | 1.06 | 1.06 | 1.77 | 1.77 | 1.77 | 1.77 | ns |
| SSTL2_II | 1.06 | 1.06 | 1.72 | 1.72 | 1.72 | 1.72 | ns |
| SSTL15 | 1.06 | 1.06 | 1.71 | 1.71 | 1.71 | 1.71 | ns |
| LVCMOS25, Slow, 2 mA | 0.66 | 0.66 | 6.01 | 6.01 | 6.01 | 6.01 | ns |
| LVCMOS25, Slow, 4 mA | 0.66 | 0.66 | 3.79 | 3.79 | 3.79 | 3.79 | ns |
| LVCMOS25, Slow, 6 mA | 0.66 | 0.66 | 3.08 | 3.08 | 3.08 | 3.08 | ns |
| LVCMOS25, Slow, 8 mA | 0.66 | 0.66 | 2.72 | 2.72 | 2.72 | 2.72 | ns |
| LVCMOS25, Slow, 12 mA | 0.66 | 0.66 | 2.17 | 2.17 | 2.17 | 2.17 | ns |
| LVCMOS25, Slow, 16 mA | 0.66 | 0.66 | 2.29 | 2.29 | 2.29 | 2.29 | ns |
| LVCMOS25, Slow, 24 mA | 0.66 | 0.66 | 2.02 | 2.02 | 2.02 | 2.02 | ns |
| LVCMOS25, Fast, 2 mA | 0.66 | 0.66 | 6.04 | 6.04 | 6.04 | 6.04 | ns |
| LVCMOS25, Fast, 4 mA | 0.66 | 0.66 | 3.82 | 3.82 | 3.82 | 3.82 | ns |
| LVCMOS25, Fast, 6 mA | 0.66 | 0.66 | 2.99 | 2.99 | 2.99 | 2.99 | ns |
| LVCMOS25, Fast, 8 mA | 0.66 | 0.66 | 2.65 | 2.65 | 2.65 | 2.65 | ns |
| LVCMOS25, Fast, 12 mA | 0.66 | 0.66 | 2.08 | 2.08 | 2.08 | 2.08 | ns |
| LVCMOS25, Fast, 16 mA | 0.66 | 0.66 | 2.13 | 2.13 | 2.13 | 2.13 | ns |
| LVCMOS25, Fast, 24 mA | 0.66 | 0.66 | 1.99 | 1.99 | 1.99 | 1.99 | ns |

*Table 38:* **IOB Switching Characteristics *(Cont'd)***

| I/O Standard | $T_{IOPI}$ | | $T_{IOOP}$ | | $T_{IOTP}$ | | Units |
|---|---|---|---|---|---|---|---|
| | Speed Grade | | Speed Grade | | Speed Grade | | |
| | -2 | -1 | -2 | -1 | -2 | -1 | |
| LVPECL_25 | 1.09 | 1.09 | 1.65 | 1.65 | 1.65 | 1.65 | ns |
| HSTL_I_12 | 1.06 | 1.06 | 1.78 | 1.78 | 1.78 | 1.78 | ns |
| HSTL_I_DCI | 1.06 | 1.06 | 1.66 | 1.66 | 1.66 | 1.66 | ns |
| HSTL_II_DCI | 1.06 | 1.06 | 1.68 | 1.68 | 1.68 | 1.68 | ns |
| HSTL_II_T_DCI | 1.06 | 1.06 | 1.66 | 1.66 | 1.66 | 1.66 | ns |
| HSTL_III_DCI | 1.06 | 1.06 | 1.62 | 1.62 | 1.62 | 1.62 | ns |
| HSTL_I_DCI_18 | 1.06 | 1.06 | 1.68 | 1.68 | 1.68 | 1.68 | ns |
| HSTL_II_DCI_18 | 1.06 | 1.06 | 1.62 | 1.62 | 1.62 | 1.62 | ns |
| HSTL_II _T_DCI_18 | 1.06 | 1.06 | 1.68 | 1.68 | 1.68 | 1.68 | ns |
| HSTL_III_DCI_18 | 1.06 | 1.06 | 1.69 | 1.69 | 1.69 | 1.69 | ns |
| DIFF_HSTL_I_18 | 1.09 | 1.09 | 1.75 | 1.75 | 1.75 | 1.75 | ns |
| DIFF_HSTL_I_DCI_18 | 1.09 | 1.09 | 1.68 | 1.68 | 1.68 | 1.68 | ns |
| DIFF_HSTL_I | 1.09 | 1.09 | 1.73 | 1.73 | 1.73 | 1.73 | ns |
| DIFF_HSTL_I_DCI | 1.09 | 1.09 | 1.66 | 1.66 | 1.66 | 1.66 | ns |
| DIFF_HSTL_II_18 | 1.09 | 1.09 | 1.81 | 1.81 | 1.81 | 1.81 | ns |
| DIFF_HSTL_II_DCI_18 | 1.09 | 1.09 | 1.62 | 1.62 | 1.62 | 1.62 | ns |
| DIFF_HSTL_II _T_DCI_18 | 1.09 | 1.09 | 1.68 | 1.68 | 1.68 | 1.68 | ns |
| DIFF_HSTL_II | 1.09 | 1.09 | 1.74 | 1.74 | 1.74 | 1.74 | ns |
| DIFF_HSTL_II_DCI | 1.09 | 1.09 | 1.68 | 1.68 | 1.68 | 1.68 | ns |
| SSTL2_I_DCI | 1.06 | 1.06 | 1.70 | 1.70 | 1.70 | 1.70 | ns |
| SSTL2_II_DCI | 1.06 | 1.06 | 1.67 | 1.67 | 1.67 | 1.67 | ns |
| SSTL2_II_T_DCI | 1.06 | 1.06 | 1.70 | 1.70 | 1.70 | 1.70 | ns |
| SSTL18_I | 1.06 | 1.06 | 1.75 | 1.75 | 1.75 | 1.75 | ns |
| SSTL18_II | 1.06 | 1.06 | 1.67 | 1.67 | 1.67 | 1.67 | ns |
| SSTL18_I_DCI | 1.06 | 1.06 | 1.67 | 1.67 | 1.67 | 1.67 | ns |
| SSTL18_II_DCI | 1.06 | 1.06 | 1.63 | 1.63 | 1.63 | 1.63 | ns |
| SSTL18_II_T_DCI | 1.06 | 1.06 | 1.67 | 1.67 | 1.67 | 1.67 | ns |
| SSTL15_T_DCI | 1.06 | 1.06 | 1.68 | 1.68 | 1.68 | 1.68 | ns |
| SSTL15_DCI | 1.06 | 1.06 | 1.68 | 1.68 | 1.68 | 1.68 | ns |
| DIFF_SSTL2_I | 1.09 | 1.09 | 1.77 | 1.77 | 1.77 | 1.77 | ns |
| DIFF_SSTL2_I_DCI | 1.09 | 1.09 | 1.70 | 1.70 | 1.70 | 1.70 | ns |
| DIFF_SSTL2_II | 1.09 | 1.09 | 1.72 | 1.72 | 1.72 | 1.72 | ns |
| DIFF_SSTL2_II_DCI | 1.09 | 1.09 | 1.67 | 1.67 | 1.67 | 1.67 | ns |
| DIFF_SSTL2_II_T_DCI | 1.09 | 1.09 | 1.70 | 1.70 | 1.70 | 1.70 | ns |
| DIFF_SSTL18_I | 1.09 | 1.09 | 1.75 | 1.75 | 1.75 | 1.75 | ns |
| DIFF_SSTL18_I_DCI | 1.09 | 1.09 | 1.67 | 1.67 | 1.67 | 1.67 | ns |
| DIFF_SSTL18_II | 1.09 | 1.09 | 1.67 | 1.67 | 1.67 | 1.67 | ns |
| DIFF_SSTL18_II_DCI | 1.09 | 1.09 | 1.63 | 1.63 | 1.63 | 1.63 | ns |

## Output Serializer/Deserializer Switching Characteristics

*Table 45:* **OSERDES Switching Characteristics**

| Symbol | Description | Speed Grade | | Units |
|---|---|---|---|---|
| | | -2 | -1 | |
| **Setup/Hold** | | | | |
| $T_{OSDCK\_D}/T_{OSCKD\_D}$ | D input Setup/Hold with respect to CLKDIV | 0.31/–0.12 | 0.31/–0.12 | ns |
| $T_{OSDCK\_T}/T_{OSCKD\_T}$(1) | T input Setup/Hold with respect to CLK | 0.56/–0.08 | 0.56/–0.08 | ns |
| $T_{OSDCK\_T2}/T_{OSCKD\_T2}$(1) | T input Setup/Hold with respect to CLKDIV | 0.31/–0.08 | 0.31/–0.08 | ns |
| $T_{OSCCK\_OCE}/T_{OSCKC\_OCE}$ | OCE input Setup/Hold with respect to CLK | 0.22/–0.05 | 0.22/–0.05 | ns |
| $T_{OSCCK\_S}$ | SR (Reset) input Setup with respect to CLKDIV | 0.07 | 0.07 | ns |
| $T_{OSCCK\_TCE}/T_{OSCKC\_TCE}$ | TCE input Setup/Hold with respect to CLK | 0.21/–0.05 | 0.21/–0.05 | ns |
| **Sequential Delays** | | | | |
| $T_{OSCKO\_OQ}$ | Clock to out from CLK to OQ | 0.82 | 0.82 | ns |
| $T_{OSCKO\_TQ}$ | Clock to out from CLK to TQ | 0.82 | 0.82 | ns |
| **Combinatorial** | | | | |
| $T_{OSDO\_TTQ}$ | T input to TQ Out | 0.97 | 0.97 | ns |

**Notes:**

1. $T_{OSDCK\_T2}$ and $T_{OSCKD\_T2}$ are reported as $T_{OSDCK\_T}/T_{OSCKD\_T}$ in the TRACE report.

*Table 50:* **Block RAM and FIFO Switching Characteristics *(Cont'd)***

| Symbol | Description | Speed Grade | | Units |
|---|---|---|---|---|
| | | -2 | -1 | |
| **Maximum Frequency** | | | | |
| $F_{MAX}$ | Block RAM (Write First and No Change modes) | 400 | 350 | MHz |
| | Block RAM (Read First mode) | 400 | 347 | MHz |
| | Block RAM (SDP mode)(12) | 400 | 347 | MHz |
| $F_{MAX\_CASCADE}$ | Block RAM Cascade (Write First and No Change modes) | 400 | 347 | MHz |
| | Block RAM Cascade (Read First mode) | 350 | 304 | MHz |
| $F_{MAX\_FIFO}$ | FIFO in all modes | 400 | 350 | MHz |
| $F_{MAX\_ECC}$ | Block RAM and FIFO in ECC configuration | 325 | 282 | MHz |

**Notes:**

1. TRACE will report all of these parameters as $T_{RCKO\_DO}$.
2. $T_{RCKO\_DOR}$ includes $T_{RCKO\_DOW}$, $T_{RCKO\_DOPR}$, and $T_{RCKO\_DOPW}$ as well as the B port equivalent timing parameters.
3. These parameters also apply to synchronous FIFO with DO_REG = 0.
4. $T_{RCKO\_DO}$ includes $T_{RCKO\_DOP}$ as well as the B port equivalent timing parameters.
5. These parameters also apply to multirate (asynchronous) and synchronous FIFO with DO_REG = 1.
6. $T_{RCKO\_FLAGS}$ includes the following parameters: $T_{RCKO\_AEMPTY}$, $T_{RCKO\_AFULL}$, $T_{RCKO\_EMPTY}$, $T_{RCKO\_FULL}$, $T_{RCKO\_RDERR}$, $T_{RCKO\_WRERR}$.
7. $T_{RCKO\_POINTERS}$ includes both $T_{RCKO\_RDCOUNT}$ and $T_{RCKO\_WRCOUNT}$.
8. The ADDR setup and hold must be met when EN is asserted (even when WE is deasserted). Otherwise, block RAM data corruption is possible.
9. $T_{RCKO\_DI}$ includes both A and B inputs as well as the parity inputs of A and B.
10. $T_{RCO\_FLAGS}$ includes the following flags: AEMPTY, AFULL, EMPTY, FULL, RDERR, WRERR, RDCOUNT, and WRCOUNT.
11. The FIFO reset must be asserted for at least three positive clock edges.
12. When using ISE software v12.4 or later, if the RDARRDR_COLLISION_HWCONFIG attribute is set to PERFORMANCE or the block RAM is in single-port operation, then the faster $F_{MAX}$ for WRITE_FIRST/NO_CHANGE modes apply.

*Table 51:* **DSP48E1 Switching Characteristics *(Cont'd)***

| Symbol | Description | Speed Grade | | Units |
|---|---|---|---|---|
| | | -2 | -1 | |
| **Combinatorial Delays from Input Pins to Cascading Output Pins** | | | | |
| $T_{DSPDO\_\{A; B\}\_\{ACOUT; BCOUT\}}$ | {A, B} input to {ACOUT, BCOUT} output | 0.65 | 0.75 | ns |
| $T_{DSPDO\_\{A, B\}\_\{PCOUT, CARRYCASCOUT, MULTSIGNOUT\}\_MULT}$ | {A, B} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output using multiplier | 5.24 | 6.03 | ns |
| $T_{DSPDO\_D\_\{PCOUT, CARRYCASCOUT, MULTSIGNOUT\}\_MULT}$ | D input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output using multiplier | 4.94 | 5.68 | ns |
| $T_{DSPDO\_\{A, B\}\_\{PCOUT, CARRYCASCOUT, MULTSIGNOUT\}}$ | {A, B} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output not using multiplier | 2.19 | 2.52 | ns |
| $T_{DSPDO\_\_\{C, CARRYIN\}\_\{PCOUT, CARRYCASCOUT,MULTSIGNOUT\}}$ | {C, CARRYIN} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output | 1.95 | 2.25 | ns |
| **Combinatorial Delays from Cascading Input Pins to All Output Pins** | | | | |
| $T_{DSPDO\_\{ACIN, BCIN\}\_\{P, CARRYOUT\}\_MULT}$ | {ACIN, BCIN} input to {P, CARRYOUT} output using multiplier | 4.97 | 5.72 | ns |
| $T_{DSPDO\_\{ACIN, BCIN\}\_\{P, CARRYOUT}$ | {ACIN, BCIN} input to {P, CARRYOUT} output not using multiplier | 1.92 | 2.21 | ns |
| $T_{DSPDO\_\{ACIN; BCIN\}\_\{ACOUT; BCOUT\}}$ | {ACIN, BCIN} input to {ACOUT, BCOUT} output | 0.49 | 0.57 | ns |
| $T_{DSPDO\_\{ACIN, BCIN\}\_\{PCOUT, CARRYCASCOUT, MULTSIGNOUT\}\_MULT}$ | {ACIN, BCIN} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output using multiplier | 5.10 | 5.86 | ns |
| $T_{DSPDO\_\{ACIN, BCIN\}\_\{PCOUT, CARRYCASCOUT, MULTSIGNOUT\}}$ | {ACIN, BCIN} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output not using multiplier | 2.05 | 2.35 | ns |
| $T_{DSPDO\_\{PCIN, CARRYCASCIN, MULTSIGNIN\}\_ \{P, CARRYOUT\}}$ | {PCIN, CARRYCASCIN, MULTSIGNIN} input to {P, CARRYOUT} output | 1.60 | 1.83 | ns |
| $T_{DSPDO\_\{PCIN, CARRYCASCIN, MULTSIGNIN\}\_ \{PCOUT, CARRYCASCOUT, MULTSIGNOUT\}}$ | {PCIN, CARRYCASCIN, MULTSIGNIN} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output | 1.72 | 1.98 | ns |
| **Clock to Outs from Output Register Clock to Output Pins** | | | | |
| $T_{DSPCKO\_\{P, CARRYOUT\}\_PREG}$ | CLK (PREG) to {P, CARRYOUT} output | 0.50 | 0.57 | ns |
| $T_{DSPCKO\_\{PCOUT, CARRYCASCOUT, MULTSIGNOUT\}\_PREG}$ | CLK (PREG) to {CARRYCASCOUT, PCOUT, MULTSIGNOUT} output | 0.50 | 0.66 | ns |
| **Clock to Outs from Pipeline Register Clock to Output Pins** | | | | |
| $T_{DSPCKO\_\{P, CARRYOUT\}\_MREG}$ | CLK (MREG) to {P, CARRYOUT} output | 2.30 | 2.65 | ns |
| $T_{DSPCKO\_\{PCOUT, CARRYCASCOUT, MULTSIGNOUT\}\_MREG}$ | CLK (MREG) to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output | 2.43 | 2.79 | ns |
| $T_{DSPCKO\_\{P, CARRYOUT\}\_ADREG\_MULT}$ | CLK (ADREG) to {P, CARRYOUT} output | 3.72 | 4.72 | ns |
| $T_{DSPCKO\_\{PCOUT, CARRYCASCOUT, MULTSIGNOUT\}\_ADREG\_MULT}$ | CLK (ADREG) to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output | 3.84 | 4.42 | ns |
| **Clock to Outs from Input Register Clock to Output Pins** | | | | |
| $T_{DSPCKO\_\{P, CARRYOUT\}\_\{AREG, BREG\}\_MULT}$ | CLK (AREG, BREG) to {P, CARRYOUT} output using multiplier | 5.36 | 6.16 | ns |
| $T_{DSPCKO\_\{P, CARRYOUT\}\_\{AREG, BREG\}}$ | CLK (AREG, BREG) to {P, CARRYOUT} output not using multiplier | 2.27 | 2.61 | ns |
| $T_{DSPCKO\_\{P, CARRYOUT\}\_CREG}$ | CLK (CREG) to {P, CARRYOUT} output | 2.27 | 2.61 | ns |
| $T_{DSPCKO\_\{P, CARRYOUT\}\_DREG\_MULT}$ | CLK (DREG) to {P, CARRYOUT} output | 5.25 | 6.04 | ns |

*Table 51:* **DSP48E1 Switching Characteristics *(Cont'd)***

| Symbol | Description | Speed Grade | | Units |
|---|---|---|---|---|
| | | -2 | -1 | |
| **Clock to Outs from Input Register Clock to Cascading Output Pins** | | | | |
| $T_{DSPCKO\_\{ACOUT;\ BCOUT\}\_\{AREG;\ BREG\}}$ | CLK (AREG, BREG) to {P, CARRYOUT} output | 0.89 | 1.02 | ns |
| $T_{DSPCKO\_\{PCOUT,\ CARRYCASCOUT,\ MULTSIGNOUT\}\_\{AREG,\ BREG\}\_MULT}$ | CLK (AREG, BREG) to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output using multiplier | 5.49 | 6.31 | ns |
| $T_{DSPCKO\_\{PCOUT,\ CARRYCASCOUT,\ MULTSIGNOUT\}\_\{AREG,\ BREG\}}$ | CLK (AREG, BREG) to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output not using multiplier | 2.40 | 2.76 | ns |
| $T_{DSPCKO\_\{PCOUT,\ CARRYCASCOUT,\ MULTSIGNOUT\}\_DREG\_MULT}$ | CLK (DREG) to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output using multiplier | 5.38 | 6.18 | ns |
| $T_{DSPCKO\_\{PCOUT,\ CARRYCASCOUT,\ MULTSIGNOUT\}\_CREG}$ | CLK (CREG) to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output | 2.40 | 2.76 | ns |
| **Maximum Frequency** | | | | |
| $F_{MAX}$ | With all registers used | 350 | 275 | MHz |
| $F_{MAX\_PATDET}$ | With pattern detector | 350 | 275 | MHz |
| $F_{MAX\_MULT\_NOMREG}$ | Two register multiply without MREG | 262 | 227 | MHz |
| $F_{MAX\_MULT\_NOMREG\_PATDET}$ | Two register multiply without MREG with pattern detect | 241 | 209 | MHz |
| $F_{MAX\_PREADD\_MULT\_NOADREG}$ | Without ADREG | 292 | 253 | MHz |
| $F_{MAX\_PREADD\_MULT\_NOADREG\_PATDET}$ | Without ADREG with pattern detect | 292 | 253 | MHz |
| $F_{MAX\_NOPIPELINEREG}$ | Without pipeline registers (MREG, ADREG) | 196 | 170 | MHz |
| $F_{MAX\_NOPIPELINEREG\_PATDET}$ | Without pipeline registers (MREG, ADREG) with pattern detect | 184 | 160 | MHz |

## Configuration Switching Characteristics

*Table 52:* **Configuration Switching Characteristics**

| Symbol | Description | Speed Grade | | Units |
|---|---|---|---|---|
| | | -2 | -1 | |
| **Power-up Timing Characteristics** | | | | |
| $T_{PL}$ (1) | Program Latency | 3 | 3 | ms, Max |
| $T_{POR}$ (1) | Power-on-Reset | 15/55 | 15/55 | ms, Min/Max |
| $T_{ICCK}$ | CCLK (output) delay | 400 | 400 | ns, Min |
| $T_{PROGRAM}$ | Program Pulse Width | 250 | 250 | ns, Min |
| **Master/Slave Serial Mode Programming Switching** (1) | | | | |
| $T_{DCCK}/T_{CCKD}$ | DIN Setup/Hold, slave mode | 4.0/0.0 | 4.0/0.0 | ns, Min |
| $T_{DSCCK}/T_{SCCKD}$ | DIN Setup/Hold, master mode | 4.0/0.0 | 4.0/0.0 | ns, Min |
| $T_{CCO}$ | DOUT at 2.5V | 6 | 6 | ns, Max |
| | DOUT at 1.8V | 6 | 6 | ns, Max |
| $F_{MCCK}$ | Maximum CCLK frequency, serial modes | 100 | 100 | MHz, Max |
| $F_{MCCKTOL}$ | Frequency Tolerance, master mode with respect to nominal CCLK | 55 | 55 | % |
| $F_{MSCCK}$ | Slave mode external CCLK | 100 | 100 | MHz |
| **SelectMAP Mode Programming Switching** | | | | |
| $T_{SMDCCK}/T_{SMCCKD}$ | SelectMAP Data Setup/Hold | 4.0/0.0 | 4.0/0.0 | ns, Min |
| $T_{SMCSCCK}/T_{SMCCKCS}$ | CSI_B Setup/Hold | 4.0/0.0 | 4.0/0.0 | ns, Min |
| $T_{SMCCKW}/T_{SMWCCK}$ | RDWR_B Setup/Hold | 10.0/0.0 | 10.0/0.0 | ns, Min |
| $T_{SMCKCSO}$ | CSO_B clock to out (330 Ω pull-up resistor required) | 7 | 7 | ns, Min |
| $T_{SMCO}$ | CCLK to DATA out in readback at 2.5V | 8 | 8 | ns, Max |
| | CCLK to DATA out in readback at 1.8V | 8 | 8 | ns, Max |
| $T_{SMCKBY}$ | CCLK to BUSY out in readback at 2.5V | 6 | 6 | ns, Max |
| | CCLK to BUSY out in readback at 1.8V | 6 | 6 | ns, Max |
| $F_{SMCCK}$ | Maximum Frequency with respect to nominal CCLK | 100 | 100 | MHz, Max |
| $F_{RBCCK}$ | Maximum Readback Frequency with respect to nominal CCLK | 100 | 100 | MHz, Max |
| $F_{MCCKTOL}$ | Frequency Tolerance with respect to nominal CCLK | 55 | 55 | % |
| **Boundary-Scan Port Timing Specifications** | | | | |
| $T_{TAPTCK}/T_{TCKTAP}$ | TMS and TDI Setup time before TCK/ Hold time after TCK | 3.0/2.0 | 3.0/2.0 | ns, Min |
| $T_{TCKTDO}$ | TCK falling edge to TDO output valid at 2.5V | 6 | 6 | ns, Max |
| | TCK falling edge to TDO output valid at 1.8V | 6 | 6 | ns, Max |
| $F_{TCK}$ | Maximum configuration TCK clock frequency | 66 | 66 | MHz, Max |
| $F_{TCKB\_MIN}$ | Minimum boundary-scan TCK clock frequency when using IEEE Std 1149.6 (AC-JTAG). Minimum operating temperature for IEEE Std 1149.6 is 0°C. | 15 | 15 | MHz, Min |
| $F_{TCKB}$ | Maximum boundary-scan TCK clock frequency | 66 | 66 | MHz, Max |

## Clock Buffers and Networks

*Table 53:* **Global Clock Switching Characteristics (Including BUFGCTRL)**

| Symbol | Description | Speed Grade | | Units |
|---|---|---|---|---|
| | | -2 | -1 | |
| $T_{BCCCK\_CE}/T_{BCCKC\_CE}$(1) | CE pins Setup/Hold | 0.16/0.00 | 0.16/0.00 | ns |
| $T_{BCCCK\_S}/T_{BCCKC\_S}$(1) | S pins Setup/Hold | 0.16/0.00 | 0.16/0.00 | ns |
| $T_{BCCKO\_O}$(2) | BUFGCTRL delay from I0/I1 to O | 0.10 | 0.10 | ns |
| **Maximum Frequency** | | | | |
| $F_{MAX}$ | Global clock tree (BUFG) | 700 | 700 | MHz |

**Notes:**

1. $T_{BCCCK\_CE}$ and $T_{BCCKC\_CE}$ must be satisfied to assure glitch-free operation of the global clock when switching between clocks. These parameters do not apply to the BUFGMUX_VIRTEX4 primitive that assures glitch-free operation. The other global clock setup and hold times are optional; only needing to be satisfied if device operation requires simulation matches on a cycle-for-cycle basis when switching between clocks.
2. $T_{BGCKO\_O}$ (BUFG delay from I0 to O) values are the same as $T_{BCCKO\_O}$ values.

*Table 54:* **Input/Output Clock Switching Characteristics (BUFIO)**

| Symbol | Description | Speed Grade | | Units |
|---|---|---|---|---|
| | | -2 | -1 | |
| $T_{BIOCKO\_O}$ | Clock to out delay from I to O | 0.18 | 0.18 | ns |
| **Maximum Frequency** | | | | |
| $F_{MAX}$ | I/O clock tree (BUFIO) | 710 | 710 | MHz |

## Virtex-6 CXT Device Pin-to-Pin Output Parameter Guidelines

All devices are 100% functionally tested. The representative values for typical pin locations and normal clock loading are listed in Table 58. Values are expressed in nanoseconds unless otherwise noted.

*Table 58:* **Global Clock Input to Output Delay Without MMCM**

| Symbol | Description | Device | Speed Grade | | Units |
|---|---|---|---|---|---|
| | | | -2 | -1 | |
| LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, *without* MMCM. | | | | | |
| $T_{ICKOF}$ | Global Clock input and OUTFF *without* MMCM | XC6VCX75T | 5.88 | 5.88 | ns |
| | | XC6VCX130T | 6.00 | 6.00 | ns |
| | | XC6VCX195T | 6.13 | 6.13 | ns |
| | | XC6VCX240T | 6.13 | 6.13 | ns |

**Notes:**

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

*Table 59:* **Global Clock Input to Output Delay With MMCM**

| Symbol | Description | Device | Speed Grade | | Units |
|---|---|---|---|---|---|
| | | | -2 | -1 | |
| LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, *with* MMCM. | | | | | |
| $T_{ICKOFMMCMGC}$ | Global Clock Input and OUTFF *with* MMCM | XC6VCX75T | 2.77 | 2.77 | ns |
| | | XC6VCX130T | 2.78 | 2.78 | ns |
| | | XC6VCX195T | 2.78 | 2.78 | ns |
| | | XC6VCX240T | 2.79 | 2.79 | ns |

**Notes:**

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. MMCM output jitter is already included in the timing calculation.

*Table 60:* **Clock-Capable Clock Input to Output Delay With MMCM**

| Symbol | Description | Device | Speed Grade | | Units |
|---|---|---|---|---|---|
| | | | -2 | -1 | |
| LVCMOS25 Clock-capable Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, *with* MMCM. | | | | | |
| $T_{ICKOFMMCMCC}$ | Clock-capable Clock Input and OUTFF *with* MMCM | XC6VCX75T | 2.63 | 2.63 | ns |
| | | XC6VCX130T | 2.65 | 2.65 | ns |
| | | XC6VCX195T | 2.65 | 2.65 | ns |
| | | XC6VCX240T | 2.65 | 2.65 | ns |

**Notes:**

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. MMCM output jitter is already included in the timing calculation.

## Clock Switching Characteristics

The parameters in this section provide the necessary values for calculating timing budgets for Virtex-6 CXT FPGA clock transmitter and receiver data-valid windows.

*Table 64:* **Duty Cycle Distortion and Clock-Tree Skew**

| Symbol | Description | Device | Speed Grade | | Units |
|---|---|---|---|---|---|
| | | | -2 | -1 | |
| $T_{DCD\_CLK}$ | Global Clock Tree Duty Cycle Distortion(1) | All | 0.12 | 0.12 | ns |
| $T_{CKSKEW}$ | Global Clock Tree Skew(2) | XC6VCX75T | 0.18 | 0.18 | ns |
| | | XC6VCX130T | 0.29 | 0.29 | ns |
| | | XC6VCX195T | 0.31 | 0.31 | ns |
| | | XC6VCX240T | 0.31 | 0.31 | ns |
| $T_{DCD\_BUFIO}$ | I/O clock tree duty cycle distortion | All | 0.08 | 0.08 | ns |
| $T_{BUFIOSKEW}$ | I/O clock tree skew across one clock region | All | 0.03 | 0.03 | ns |
| $T_{BUFIOSKEW2}$ | I/O clock tree skew across three clock regions | All | 0.22 | 0.22 | ns |
| $T_{DCD\_BUFR}$ | Regional clock tree duty cycle distortion | All | 0.15 | 0.15 | ns |

**Notes:**

1. These parameters represent the worst-case duty cycle distortion observable at the pins of the device using LVDS output buffers. For cases where other I/O standards are used, IBIS can be used to calculate any additional duty cycle distortion that might be caused by asymmetrical rise/fall times.
2. The $T_{CKSKEW}$ value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx FPGA_Editor and Timing Analyzer tools to evaluate clock skew specific to your application.

*Table 65:* **Package Skew**

| Symbol | Description | Device | Package | Value | Units |
|---|---|---|---|---|---|
| $T_{PKGSKEW}$ | Package Skew(1) | XC6VCX75T | FF484 | | ps |
| | | | FF784 | | ps |
| | | XC6VCX130T | FF484 | 95 | ps |
| | | | FF784 | 146 | ps |
| | | | FF1156 | 165 | ps |
| | | XC6VCX195T | FF784 | | ps |
| | | | FF1156 | | ps |
| | | XC6VCX240T | FF784 | 146 | ps |
| | | | FF1156 | 182 | ps |

**Notes:**

1. These values represent the worst-case skew between any two SelectIO resources in the package: shortest flight time to longest flight time from Pad to Ball (7.0 ps per mm).
2. Package trace length information is available for these device/package combinations. This information can be used to deskew the package.

| Date | Version | Description of Revisions |
|---|---|---|
| 06/08/10 | 1.2 | Revised GTX Transceivers in CXT Devices, page 5.<br>Added $V_{FS}$ and revised the $V_{IN}$ and $V_{TS}$ values in Table 9, page 11.<br>Added $V_{FS}$ and note 6 to Table 10. Revised description of $C_{IN}$ in Table 11, including adding note 3.<br>Updated Table 13 including adding note 2.<br>Removed DIFF SSTL15 and added values to SSTL15 in Table 15.<br>Updated Table 16 through Table 19.<br>Added eFUSE Read Endurance section.<br>Updated entire GTX Transceivers in CXT Devices section.<br>Changed specifications of PCI Express in Table 34.<br>In Table 35, removed RLDRAM II and revised and added values to other interface performance specifications.<br>Updated speed specification to v1.04 with appropriate changes to Table 36.<br>Revised the IOB switching characteristics in Table 38.<br>Updated values in Table 39 and note 4 in Table 41.<br>ILOGIC (Table 42), OLOGIC (Table 43), ISERDES (Table 44), and OSERDES (Table 45) switching characteristics changes.<br>Revised $T_{IODELAY\_CLK\_MAX}$ and $T_{IDELAYPAT\_JIT}$ in Table 46.<br>Revised CLB switching characteristics and added $T_{SHCKO}$ to Table 47and revised CLB switching characteristics in Table 48 and Table 49.<br>In Table 50, removed $T_{RCKO\_RDCOUNT}$ and $T_{RCKO\_WRCOUNT}$, removed $T_{RCKO\_PARITY\_ECC}$: Clock CLK to ECCPARITY in standard ECC mode, revised $T_{RDCK\_DI\_ECC}$/$T_{RCKD\_DI\_ECC}$, $T_{RCKO\_POINTERS}$, and revised $F_{MAX}$ and $F_{MAX\_CASCADE}$ switching characteristics.<br>Multiple changes to configuration specifications in Table 52.<br>Revised switching characteristics and global clock tree (BUFG) $F_{MAX}$ in Table 53.<br>Revised switching characteristics and I/O clock tree (BUFIO) $F_{MAX}$ in Table 54.<br>Added note 1 to Table 55.<br>Revised the $F_{MAX}$ horizontal clock tree (BUFH) in Table 56.<br>Multiple changes to MMCM specifications in Table 57 including $F_{INMAX}$ and $F_{OUTMAX}$.<br>Updated switching characteristics in Table 58 through Table 63.<br>Removed $T_{DCD\_BUFH}$ and $T_{BUFHSKEW}$ from Table 64. |
| 06/30/10 | 1.3 | Production release of XC6VCX130T and XC6VCX240T in Table 36 and Table 37. Updated -1 speed grade SDR values in Table 35. Updated BUFIO $F_{MAX}$ specification in Table 54. Added Note 6 to Table 57. |
| 07/28/10 | 1.4 | Production release of XC6VCX75T and XC6VCX195T in Table 36 and Table 37 using ISE 12.2 software with speed file v1.06 using the *Speed File Patch*. Updated PCI compliance on page 1. Added values to Table 13. In Table 25, update $V_{CMOUTDC}$ equation to MGTAVTT – $DV_{PPOUT}$/4. Updated $F_{MAX}$ in Table 53, Table 54, and Table 56. Updated $F_{INMAX}$ and $F_{OUTMAX}$ in Table 57. Updated values in Table 61, Table 62, and Table 63. |
| 10/14/10 | 1.5 | Moved data sheet to Production status on the first page. Updated speed file with ISE 12.3 software with speed file v1.08 using the *Speed File Patch.* In Table 51, updated values for $T_{DSPCKO\_\{PCOUT,}$ CARRYCASCOUT, MULTSIGNOUT}_PREG. |
| 02/11/11 | 1.6 | Updated Table 10 to include the industrial range specifications. Added Note 12 to Table 50. Revised $T_{BPICCO}$ values in Table 52. Updated range description for $F_{INDUTY}$ in Table 57 and added note 8.<br>The following revisions are due to specification changes as described in XCN11009, *Virtex-6 FPGA: Data Sheet, User Guides, and JTAG ID Updates*.<br>In Table 52, updated the values for $T_{SMCCKW}$, $T_{SPIDCC}$, $T_{SPICCM}$, and $T_{SPICCFC}$. In Table 57: MMCM Specification, added bandwidth settings to $F_{PFDMIN}$ and added note 1. |