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Virtex-6 CXT FPGA Documentation

In addition to the data sheet information found herein, complete and up-to-date documentation of the Virtex-6 family of FPGAs is available on the Xilinx website and available for download:

Virtex-6 FPGA Configuration Guide **(UG360)**

This all-encompassing configuration guide includes chapters on configuration interfaces (serial and parallel), multi-bitstream management, bitstream encryption, boundary-scan and JTAG configuration, and reconfiguration techniques.

Virtex-6 FPGA SelectIO Resources User Guide **(UG361)**

This guide describes the SelectIO™ resources available in all the Virtex-6 CXT devices.

Virtex-6 FPGA Clocking Resources User Guide **(UG362)**

This guide describes the clocking resources available in all the Virtex-6 CXT devices, including the MMCM and clock buffers.

Virtex-6 FPGA Memory Resources User Guide **(UG363)**

This guide describes the Virtex-6 CXT device block RAM and FIFO capabilities.

Virtex-6 FPGA CLB User Guide **(UG364)**

This guide describes the capabilities of the configurable logic blocks (CLB) available in all Virtex-6 CXT devices.

Virtex-6 FPGA DSP48E1 Slice User Guide **(UG369)**

This guide describes the architecture of the DSP48E1 slice in Virtex-6 CXT FPGAs and provides configuration examples.

Virtex-6 FPGA GTX Transceivers User Guide **(UG366)**

This guide describes the GTX transceivers available in all the Virtex-6 CXT FPGAs.

Virtex-6 FPGA Tri-Mode Ethernet MAC User Guide **(UG368)**

This guide describes the dedicated tri-mode Ethernet media access controller (TEMAC) available in all the Virtex-6 CXT FPGAs.

Virtex-6 FPGA Data Sheet: DC and Switching Characteristics **(DS152)**

Reference this data sheet when considering device migration to the Virtex-6 LXT and SXT families. It contains the DC and Switching Characteristic specifications specifically for the Virtex-6 LXT and SXT families.

Virtex-6 FPGA Packaging and Pinout Specifications **(UG365)**

These specifications includes the tables for device/package combinations and maximum I/Os, pin definitions, pinout tables, pinout diagrams, mechanical drawings, and thermal specifications of the Virtex-6 LXT and SXT families. Reference these specifications when considering device migration to the Virtex-6 LXT and SXT families.

Configuration Bitstream Overview for CXT Devices

This section contains two tables similar to those in the *Virtex-6 FPGA Configuration Guide* only updated for the CXT family. The Virtex-6 CXT FPGA bitstream contains commands to the FPGA configuration logic as well as configuration data. Table 3 gives a typical bitstream length and Table 4 gives the specific device ID codes for the Virtex-6 CXT devices.

Table 3: **Virtex-6 CXT FPGA Bitstream Length**

Device	Total Number of Configuration Bits
XC6VCX75T	26,239,328
XC6VCX130T	43,719,776
XC6VCX195T	61,552,736
XC6VCX240T	73,859,552

Table 4: **Virtex-6 CXT FPGA Device ID Codes**

Device	ID Code (Hex)
XC6VCX75T	0x042C4093
XC6VCX130T	0x042CA093
XC6VCX195T	0x042CC093
XC6VCX240T	0x042D0093

FF784 Package Placement Diagrams

Figure 4 through Figure 6 show the placement diagrams for the GTX transceivers in the FF784 package.

Note: Unbonded locations in the FF784 package are:

- CX130T: X0Y0, X0Y1, X0Y2, X0Y3
- CX195T: X0Y0, X0Y1, X0Y2, X0Y3
- CX240T: X0Y0, X0Y1, X0Y2, X0Y3

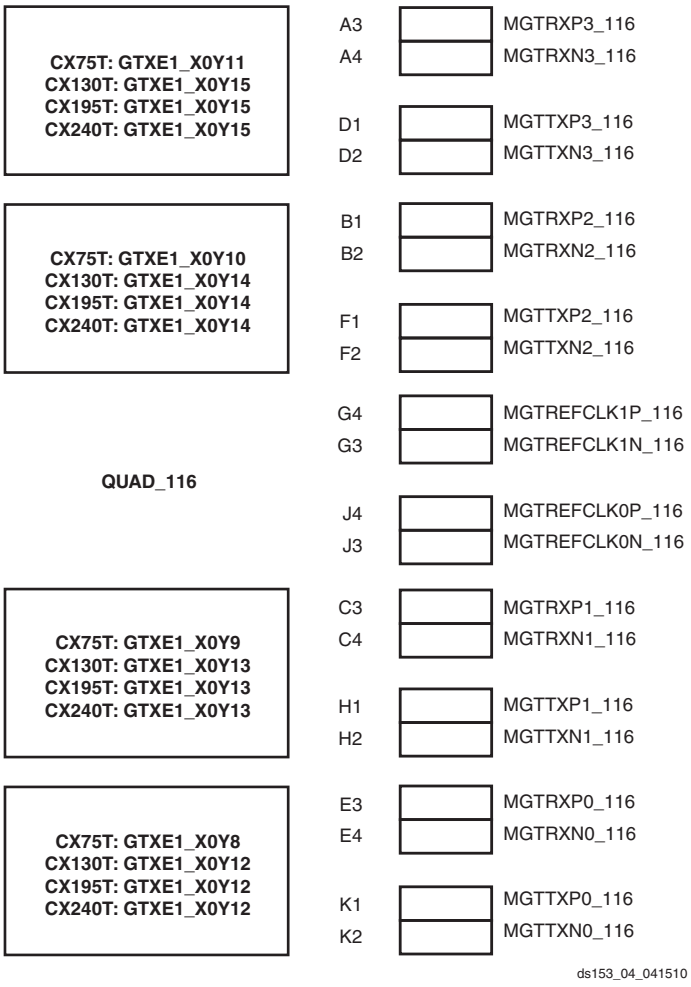

Figure 4: **Placement Diagram for the FF784 Package (1 of 3)**

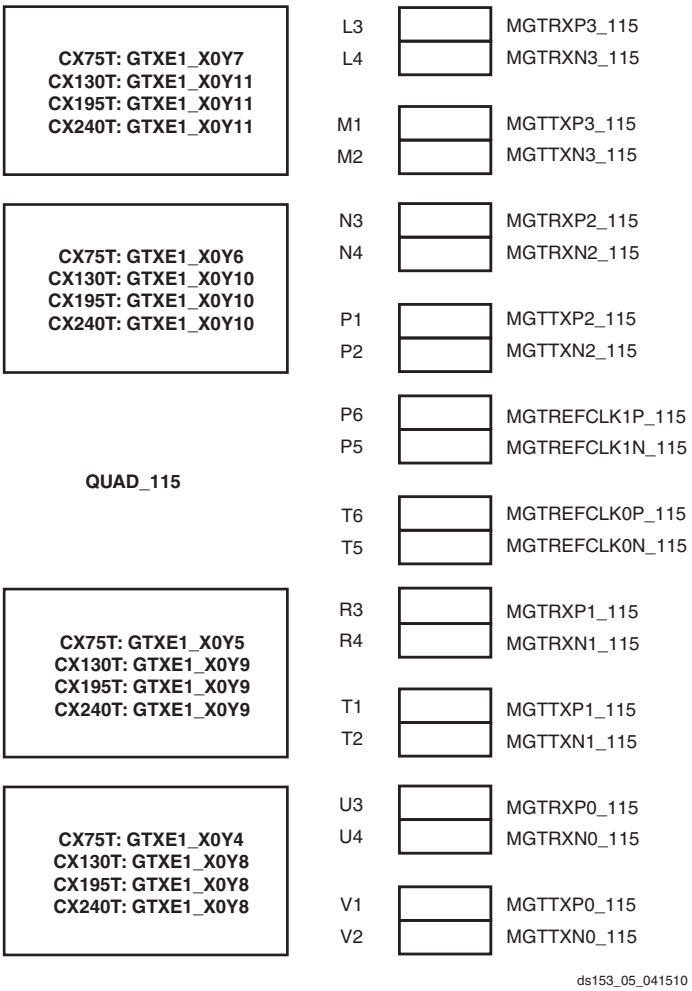

Figure 5: **Placement Diagram for the FF784 Package (2 of 3)**

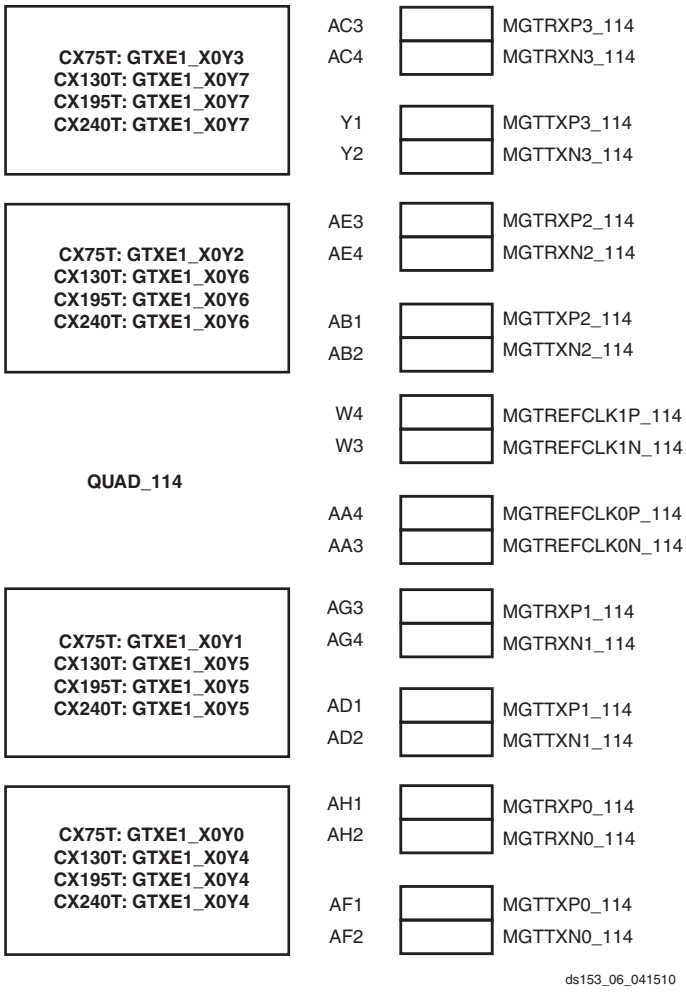

Figure 6: **Placement Diagram for the FF784 Package (3 of 3)**

Virtex-6 CXT FPGA Electrical Characteristics Introduction

Virtex-6 CXT FPGAs are available in -2 and -1 speed grades, with -2 having the highest performance. Virtex-6 CXT FPGA DC and AC characteristics are specified for both commercial and industrial grades. Except the operating temperature range or unless otherwise noted, all the DC and AC electrical parameters are the same for a particular speed grade (that is, the timing characteristics of a -1 speed grade industrial device are the same as for a -1 speed grade commercial device). However, only selected speed grades and/or devices might be available in the industrial range.

All supply voltage and junction temperature specifications are representative of worst-case conditions. The parameters included are common to popular designs and typical applications.

All specifications are subject to change without notice.

Virtex-6 CXT FPGA DC Characteristics

Table 9: **Absolute Maximum Ratings(1)**

Symbol	Description		Units
V_{CCINT}	Internal supply voltage relative to GND	–0.5 to 1.1	V
V_{CCAUX}	Auxiliary supply voltage relative to GND	–0.5 to 3.0	V
V_{CCO}	Output drivers supply voltage relative to GND	–0.5 to 3.0	V
V_{BATT}	Key memory battery backup supply	–0.5 to 3.0	V
V_{FS}	External voltage supply for eFUSE programming(2)	–0.5 to 3.0	V
V_{REF}	Input reference voltage	–0.5 to 3.0	V
V_{IN}(3)	2.5V or below I/O input voltage relative to GND(4) (user and dedicated I/Os)	–0.5 to V_{CCO} + 0.5	V
V_{TS}	Voltage applied to 3-state 2.5V or below output(4) (user and dedicated I/Os)	–0.5 to V_{CCO} + 0.5	V
T_{STG}	Storage temperature (ambient)	–65 to 150	°C
T_{SOL}	Maximum soldering temperature(5)	+220	°C
T_j	Maximum junction temperature(5)	+125	°C

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
2. When not programming eFUSE, connect V_{FS} to GND.
3. 2.5V I/O absolute maximum limit applied to DC and AC signals.
4. For I/O operation, refer to the *Virtex-6 FPGA SelectIO Resources User Guide*.
5. For soldering guidelines and thermal considerations, see *Virtex-6 FPGA Packaging and Pinout Specification*.

Table 10: **Recommended Operating Conditions**

Symbol	Description	Min	Max	Units
V_{CCINT}	Internal supply voltage relative to GND, T_j = 0°C to +85°C	0.95	1.05	V
	Internal supply voltage relative to GND, T_j = –40°C to +100°C	0.95	1.05	V
V_{CCAUX}	Auxiliary supply voltage relative to GND, T_j = 0°C to +85°C	2.375	2.625	V
	Auxiliary supply voltage relative to GND, T_j = –40°C to +100°C	2.375	2.625	V
V_{CCO}(1)(2)(3)	Supply voltage relative to GND, T_j = 0°C to +85°C	1.14	2.625	V
	Supply voltage relative to GND, T_j = –40°C to +100°C	1.14	2.625	V
V_{IN}	2.5V supply voltage relative to GND, T_j = 0°C to +85°C	GND – 0.20	2.625	V
	2.5V supply voltage relative to GND, T_j = –40°C to +100°C	GND – 0.20	2.625	V
	2.5V and below supply voltage relative to GND, T_j = 0°C to +85°C	GND – 0.20	V_{CCO} + 0.2	V
	2.5V and below supply voltage relative to GND, T_j = –40°C to +100°C	GND – 0.20	V_{CCO} + 0.2	V
I_{IN}(4)	Maximum current through any pin in a powered or unpowered bank when forward biasing the clamp diode.	–	10	mA
V_{BATT}(5)	Battery voltage relative to GND, T_j = 0°C to +85°C	1.0	2.5	V
	Battery voltage relative to GND, T_j = –40°C to +100°C	1.0	2.5	V
V_{FS}(6)	External voltage supply for eFUSE programming	2.375	2.625	V

Notes:

1. Configuration data is retained even if V_{CCO} drops to 0V.
2. Includes V_{CCO} of 1.2V, 1.5V, 1.8V, and 2.5V.
3. The configuration supply voltage V_{CC_CONFIG} is also known as V_{CCO_0}.
4. A total of 100 mA per bank should not be exceeded.
5. V_{BATT} is required only when using bitstream encryption. If battery is not used, connect V_{BATT} to either ground or V_{CCAUX}.
6. When not programming eFUSE, connect V_{FS} to GND.
7. All voltages are relative to ground.

Table 11: **DC Characteristics Over Recommended Operating Conditions(1)(2)**

Symbol	Description	Min	Typ	Max	Units
V_{DRINT}	Data retention V_{CCINT} voltage (below which configuration data might be lost)	0.75	–	–	V
V_{DRI}	Data retention V_{CCAUX} voltage (below which configuration data might be lost)	2.0	–	–	V
I_{REF}	V_{REF} leakage current per pin	–	–	10	µA
I_L	Input or output leakage current per pin (sample-tested)	–	–	10	µA
C_{IN}(3)	Die input capacitance at the pad	–	–	8	pF
I_{RPU}	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 2.5V	20	–	80	µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 1.8V	8	–	40	µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 1.5V	5	–	30	µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 1.2V	1	–	20	µA
I_{RPD}	Pad pull-down (when selected) @ V_{IN} = 2.5V	3	–	80	µA
I_{BATT}	Battery supply current	–	–	150	nA
n	Temperature diode ideality factor	–	1.0002	–	n
r	Series resistance	–	5	–	Ω

Notes:

1. Typical values are specified at nominal voltage, 25°C.
2. Maximum value specified for worst case process at 25°C.
3. This measurement represents the die capacitance at the pad, not including the package.

SelectIO™ DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

Table 15: **SelectIO DC Input and Output Levels**

I/O Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
LVCMOS25, LVDCI25	–0.3	0.7	1.7	V_{CCO} + 0.3	0.4	V_{CCO} – 0.4	Note(3)	Note(3)
LVCMOS18, LVDCI18	–0.3	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.3	0.45	V_{CCO} – 0.45	Note(4)	Note(4)
LVCMOS15, LVDCI15	–0.3	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.3	25% V_{CCO}	75% V_{CCO}	Note(4)	Note(4)
LVCMOS12	–0.3	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.3	25% V_{CCO}	75% V_{CCO}	Note(5)	Note(5)
HSTL I_12	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.3	25% V_{CCO}	75% V_{CCO}	6.3	6.3
HSTL I(2)	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.3	0.4	V_{CCO} – 0.4	8	–8
HSTL II(2)	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.3	0.4	V_{CCO} – 0.4	16	–16
HSTL III(2)	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.3	0.4	V_{CCO} – 0.4	24	–8
DIFF HSTL I(2)	–0.3	50% V_{CCO} – 0.1	50% V_{CCO} + 0.1	V_{CCO} + 0.3	–	–	–	–
DIFF HSTL II(2)	–0.3	50% V_{CCO} – 0.1	50% V_{CCO} + 0.1	V_{CCO} + 0.3	–	–	–	–
SSTL2 I	–0.3	V_{REF} – 0.15	V_{REF} + 0.15	V_{CCO} + 0.3	V_{TT} – 0.61	V_{TT} + 0.61	8.1	–8.1
SSTL2 II	–0.3	V_{REF} – 0.15	V_{REF} + 0.15	V_{CCO} + 0.3	V_{TT} – 0.81	V_{TT} + 0.81	16.2	–16.2
DIFF SSTL2 I	–0.3	50% V_{CCO} – 0.15	50% V_{CCO} + 0.15	V_{CCO} + 0.3	–	–	–	–
DIFF SSTL2 II	–0.3	50% V_{CCO} – 0.15	50% V_{CCO} + 0.15	V_{CCO} + 0.3	–	–	–	–
SSTL18 I	–0.3	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.3	V_{TT} – 0.47	V_{TT} + 0.47	6.7	–6.7
SSTL18 II	–0.3	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.3	V_{TT} – 0.60	V_{TT} + 0.60	13.4	–13.4
DIFF SSTL18 I	–0.3	50% V_{CCO} – 0.125	50% V_{CCO} + 0.125	V_{CCO} + 0.3	–	–	–	–
DIFF SSTL18 II	–0.3	50% V_{CCO} – 0.125	50% V_{CCO} + 0.125	V_{CCO} + 0.3	–	–	–	–
SSTL15	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.3	V_{TT} – 0.175	V_{TT} + 0.175	14.3	14.3

Notes:

1. Tested according to relevant specifications.
2. Applies to both 1.5V and 1.8V HSTL.
3. Using drive strengths of 2, 4, 6, 8, 12, 16, or 24 mA.
4. Using drive strengths of 2, 4, 6, 8, 12, or 16 mA.
5. Supported drive strengths of 2, 4, 6, or 8 mA.
6. For detailed interface specific DC voltage levels, see the *Virtex-6 FPGA SelectIO Resources User Guide*.

Table 22: **Recommended Operating Conditions for GTX Transceivers(1)(2)**

Symbol	Description	Min	Typ	Max	Units
MGTAVCC	Analog supply voltage for the GTX transmitter and receiver circuits relative to GND	0.95	1.0	1.06	V
MGTAVTT	Analog supply voltage for the GTX transmitter and receiver termination circuits relative to GND	1.14	1.2	1.26	V
MGTAVTTRCAL	Analog supply voltage for the resistor calibration circuit of the GTX transceiver column	1.14	1.2	1.26	V

Notes:

1. Each voltage listed requires the filter circuit described in *Virtex-6 FPGA GTX Transceivers User Guide*.
2. Voltages are specified for the temperature range of T_j = –40°C to +100°C.

Table 23: **GTX Transceiver Supply Current (per Lane) (1)(2)**

Symbol	Description	Typ	Max	Units
$I_{MGTAVTT}$	MGTAVTT supply current for one GTX transceiver	55.9	Note 2	mA
$I_{MGTAVCC}$	MGTAVCC supply current for one GTX transceiver	56.1		mA
$MGTR_{REF}$	Precision reference resistor for internal calibration termination	100.0 ± 1% tolerance		Ω

Notes:

1. Typical values are specified at nominal voltage, 25°C, with a 3.125 Gb/s line rate.
2. Values for currents other than the values specified in this table can be obtained by using the XPOWER Estimator (XPE) or XPOWER Analyzer (XPA) tools.

Table 24: **GTX Transceiver Quiescent Supply Current (per Lane)(1)(2)(3)**

Symbol	Description	Typ(4)	Max	Units
$I_{MGTAVTTQ}$	Quiescent MGTAVTT supply current for one GTX transceiver	0.9	Note 2	mA
$I_{MGTAVCCQ}$	Quiescent MGTAVCC supply current for one GTX transceiver	3.5		mA

Notes:

1. Device powered and unconfigured.
2. Currents for conditions other than values specified in this table can be obtained by using the XPOWER Estimator (XPE) or XPOWER Analyzer (XPA) tools.
3. GTX transceiver quiescent supply current for an entire device can be calculated by multiplying the values in this table by the number of available GTX transceivers.
4. Typical values are specified at nominal voltage, 25°C.

Table 26 summarizes the DC specifications of the clock input of the GTX transceiver. Consult the *Virtex-6 FPGA GTX Transceivers User Guide* for further details.

Table 26: **GTX Transceiver Clock DC Input Level Specification**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{IDIFF}	Differential peak-to-peak input voltage		210	800	2000	mV
R_{IN}	Differential input resistance		90	100	130	Ω
C_{EXT}	Required external AC coupling capacitor		–	100	–	nF

GTX Transceiver Switching Characteristics

Consult *Virtex-6 FPGA GTX Transceivers User Guide* for further information.

Table 27: **GTX Transceiver Performance**

Symbol	Description	Speed Grade		Units
		-2	-1	
F_{GTXMAX}	Maximum GTX transceiver data rate	3.75	3.75	Gb/s
$F_{GPLLMAX}$	Maximum PLL frequency	2.5	2.5	GHz
$F_{GPLLMIN}$	Minimum PLL frequency	1.2	1.2	GHz

Table 28: **GTX Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics**

Symbol	Description	Speed Grade		Units
		-2	-1	
$F_{GTXDRPCLK}$	GTXDRPCLK maximum frequency	100	100	MHz

Table 29: **GTX Transceiver Reference Clock Switching Characteristics**

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
F_{GCLK}	Reference clock frequency range		67.5	–	375	MHz
T_{RCLK}	Reference clock rise time	20% – 80%	–	200	–	ps
T_{FCLK}	Reference clock fall time	80% – 20%	–	200	–	ps
T_{DCREF}	Reference clock duty cycle	Transceiver PLL only	45	50	55	%
T_{LOCK}	Clock recovery frequency acquisition time	Initial PLL lock	–	–	1	ms
T_{PHASE}	Clock recovery phase acquisition time	Lock to data after PLL has locked to the reference clock	–	–	200	µs

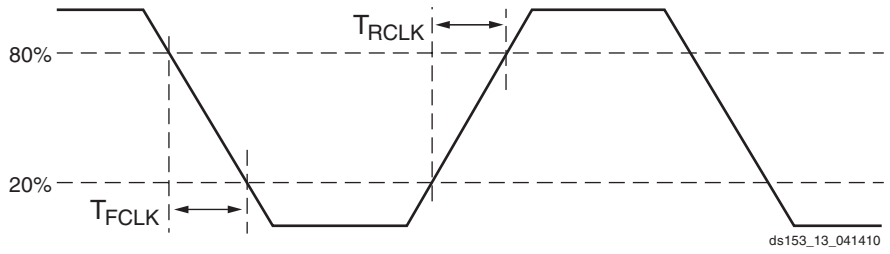

Figure 13: **Reference Clock Timing Parameters**

Switching Characteristics

All values represented in this data sheet are based on the speed specification (version 1.08). Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

Advance

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary

These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

Production

These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

All specifications are always representative of worst-case supply voltage and junction temperature conditions.

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device.

Table 36 correlates the current status of each Virtex-6 CXT device on a per speed grade basis.

Table 36: **Virtex-6 CXT Device/Speed Grade Designations**

Device	Speed Grade Designations		
	Advance	Preliminary	Production
XC6VCX75T			-2, -1
XC6VCX130T			-2, -1
XC6VCX195T			-2, -1
XC6VCX240T			-2, -1

Testing of Switching Characteristics

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Virtex-6 CXT devices.

Production Silicon and ISE Software Status

In some cases, a particular family member (and speed grade) is released to production before a speed specification is released with the correct label (Advance, Preliminary, Production). Any labeling discrepancies are corrected in subsequent speed specification releases. Table 37 lists the production released Virtex-6 family member, speed grade, and the minimum corresponding supported speed specification version and ISE software revisions. The ISE® software and speed specifications listed are the minimum releases required for production. All subsequent releases of software and speed specifications are valid.

Table 37: **Virtex-6 CXT Device/Production Software and Speed Specification Release**

Device	Speed Grade Designations	
	-2	-1
XC6VCX75T	ISE 12.2 (with speed file patch) v1.06	
XC6VCX130T	ISE 12.1 v1.04	
XC6VCX195T	ISE 12.2 (with speed file patch) v1.06	
XC6VCX240T	ISE 12.1 v1.04	

Notes:

1. Blank entries indicate a device and/or speed grade in advance or preliminary status.

IOB Pad Input/Output/3-State Switching Characteristics

Table 38 summarizes the values of standard-specific data input delay adjustments, output delays terminating at pads (based on standard) and 3-state delays.

T_{IOPI} is described as the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.

T_{IOOP} is described as the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.

T_{IOTP} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer.

Table 39 summarizes the value of T_{IOTPHZ}. T_{IOTPHZ} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is enabled (i.e., a high impedance state).

Table 38: **IOB Switching Characteristics**

I/O Standard	T_{IOPI}		T_{IOOP}		T_{IOTP}		Units
	Speed Grade		Speed Grade		Speed Grade		
	-2	-1	-2	-1	-2	-1	
LVDS_25	1.09	1.09	1.68	1.68	1.68	1.68	ns
LVDSEXT_25	1.09	1.09	1.84	1.84	1.84	1.84	ns
HT_25	1.09	1.09	1.78	1.78	1.78	1.78	ns
BLVDS_25	1.09	1.09	1.67	1.67	1.67	1.67	ns
RSDS_25 (point to point)	1.09	1.09	1.68	1.68	1.68	1.68	ns
HSTL_I	1.06	1.06	1.73	1.73	1.73	1.73	ns
HSTL_II	1.06	1.06	1.74	1.74	1.74	1.74	ns
HSTL_III	1.06	1.06	1.71	1.71	1.71	1.71	ns
HSTL_I_18	1.06	1.06	1.75	1.75	1.75	1.75	ns
HSTL_II_18	1.06	1.06	1.81	1.81	1.81	1.81	ns
HSTL_III_18	1.06	1.06	1.71	1.71	1.71	1.71	ns
SSTL2_I	1.06	1.06	1.77	1.77	1.77	1.77	ns
SSTL2_II	1.06	1.06	1.72	1.72	1.72	1.72	ns
SSTL15	1.06	1.06	1.71	1.71	1.71	1.71	ns
LVCMOS25, Slow, 2 mA	0.66	0.66	6.01	6.01	6.01	6.01	ns
LVCMOS25, Slow, 4 mA	0.66	0.66	3.79	3.79	3.79	3.79	ns
LVCMOS25, Slow, 6 mA	0.66	0.66	3.08	3.08	3.08	3.08	ns
LVCMOS25, Slow, 8 mA	0.66	0.66	2.72	2.72	2.72	2.72	ns
LVCMOS25, Slow, 12 mA	0.66	0.66	2.17	2.17	2.17	2.17	ns
LVCMOS25, Slow, 16 mA	0.66	0.66	2.29	2.29	2.29	2.29	ns
LVCMOS25, Slow, 24 mA	0.66	0.66	2.02	2.02	2.02	2.02	ns
LVCMOS25, Fast, 2 mA	0.66	0.66	6.04	6.04	6.04	6.04	ns
LVCMOS25, Fast, 4 mA	0.66	0.66	3.82	3.82	3.82	3.82	ns
LVCMOS25, Fast, 6 mA	0.66	0.66	2.99	2.99	2.99	2.99	ns
LVCMOS25, Fast, 8 mA	0.66	0.66	2.65	2.65	2.65	2.65	ns
LVCMOS25, Fast, 12 mA	0.66	0.66	2.08	2.08	2.08	2.08	ns
LVCMOS25, Fast, 16 mA	0.66	0.66	2.13	2.13	2.13	2.13	ns
LVCMOS25, Fast, 24 mA	0.66	0.66	1.99	1.99	1.99	1.99	ns

Table 38: **IOB Switching Characteristics *(Cont'd)***

I/O Standard	T_{IOPI}		T_{IOOP}		T_{IOTP}		Units
	Speed Grade		Speed Grade		Speed Grade		
	-2	-1	-2	-1	-2	-1	
LVCMOS18, Slow, 2 mA	0.71	0.71	4.87	4.87	4.87	4.87	ns
LVCMOS18, Slow, 4 mA	0.71	0.71	3.21	3.21	3.21	3.21	ns
LVCMOS18, Slow, 6 mA	0.71	0.71	2.64	2.64	2.64	2.64	ns
LVCMOS18, Slow, 8 mA	0.71	0.71	2.27	2.27	2.27	2.27	ns
LVCMOS18, Slow, 12 mA	0.71	0.71	2.15	2.15	2.15	2.15	ns
LVCMOS18, Slow, 16 mA	0.71	0.71	2.11	2.11	2.11	2.11	ns
LVCMOS18, Fast, 2 mA	0.71	0.71	4.57	4.57	4.57	4.57	ns
LVCMOS18, Fast, 4 mA	0.71	0.71	2.97	2.97	2.97	2.97	ns
LVCMOS18, Fast, 6 mA	0.71	0.71	2.46	2.46	2.46	2.46	ns
LVCMOS18, Fast, 8 mA	0.71	0.71	2.13	2.13	2.13	2.13	ns
LVCMOS18, Fast, 12 mA	0.71	0.71	1.97	1.97	1.97	1.97	ns
LVCMOS18, Fast, 16 mA	0.71	0.71	1.91	1.91	1.91	1.91	ns
LVCMOS15, Slow, 2 mA	0.85	0.85	4.29	4.29	4.29	4.29	ns
LVCMOS15, Slow, 4 mA	0.85	0.85	3.10	3.10	3.10	3.10	ns
LVCMOS15, Slow, 6 mA	0.85	0.85	2.68	2.68	2.68	2.68	ns
LVCMOS15, Slow, 8 mA	0.85	0.85	2.23	2.23	2.23	2.23	ns
LVCMOS15, Slow, 12 mA	0.85	0.85	2.13	2.13	2.13	2.13	ns
LVCMOS15, Slow, 16 mA	0.85	0.85	2.04	2.04	2.04	2.04	ns
LVCMOS15, Fast, 2 mA	0.85	0.85	4.28	4.28	4.28	4.28	ns
LVCMOS15, Fast, 4 mA	0.85	0.85	2.78	2.78	2.78	2.78	ns
LVCMOS15, Fast, 6 mA	0.85	0.85	2.42	2.42	2.42	2.42	ns
LVCMOS15, Fast, 8 mA	0.85	0.85	2.11	2.11	2.11	2.11	ns
LVCMOS15, Fast, 12 mA	0.85	0.85	1.97	1.97	1.97	1.97	ns
LVCMOS15, Fast, 16 mA	0.85	0.85	1.96	1.96	1.96	1.96	ns
LVCMOS12, Slow, 2 mA	0.93	0.93	3.75	3.75	3.75	3.75	ns
LVCMOS12, Slow, 4 mA	0.93	0.93	2.93	2.93	2.93	2.93	ns
LVCMOS12, Slow, 6 mA	0.93	0.93	2.41	2.41	2.41	2.41	ns
LVCMOS12, Slow, 8 mA	0.93	0.93	2.25	2.25	2.25	2.25	ns
LVCMOS12, Fast, 2 mA	0.93	0.93	3.39	3.39	3.39	3.39	ns
LVCMOS12, Fast, 4 mA	0.93	0.93	2.51	2.51	2.51	2.51	ns
LVCMOS12, Fast, 6 mA	0.93	0.93	2.11	2.11	2.11	2.11	ns
LVCMOS12, Fast, 8 mA	0.93	0.93	2.02	2.02	2.02	2.02	ns
LVDCI_25	0.66	0.66	2.26	2.26	2.26	2.26	ns
LVDCI_18	0.71	0.71	2.47	2.47	2.47	2.47	ns
LVDCI_15	0.85	0.85	2.24	2.24	2.24	2.24	ns
LVDCI_DV2_25	0.66	0.66	2.01	2.01	2.01	2.01	ns
LVDCI_DV2_18	0.71	0.71	2.00	2.00	2.00	2.00	ns
LVDCI_DV2_15	0.85	0.85	1.91	1.91	1.91	1.91	ns

Table 38: **IOB Switching Characteristics *(Cont'd)***

I/O Standard	T_{IOPI}		T_{IOOP}		T_{IOTP}		Units
	Speed Grade		Speed Grade		Speed Grade		
	-2	-1	-2	-1	-2	-1	
LVPECL_25	1.09	1.09	1.65	1.65	1.65	1.65	ns
HSTL_I_12	1.06	1.06	1.78	1.78	1.78	1.78	ns
HSTL_I_DCI	1.06	1.06	1.66	1.66	1.66	1.66	ns
HSTL_II_DCI	1.06	1.06	1.68	1.68	1.68	1.68	ns
HSTL_II_T_DCI	1.06	1.06	1.66	1.66	1.66	1.66	ns
HSTL_III_DCI	1.06	1.06	1.62	1.62	1.62	1.62	ns
HSTL_I_DCI_18	1.06	1.06	1.68	1.68	1.68	1.68	ns
HSTL_II_DCI_18	1.06	1.06	1.62	1.62	1.62	1.62	ns
HSTL_II _T_DCI_18	1.06	1.06	1.68	1.68	1.68	1.68	ns
HSTL_III_DCI_18	1.06	1.06	1.69	1.69	1.69	1.69	ns
DIFF_HSTL_I_18	1.09	1.09	1.75	1.75	1.75	1.75	ns
DIFF_HSTL_I_DCI_18	1.09	1.09	1.68	1.68	1.68	1.68	ns
DIFF_HSTL_I	1.09	1.09	1.73	1.73	1.73	1.73	ns
DIFF_HSTL_I_DCI	1.09	1.09	1.66	1.66	1.66	1.66	ns
DIFF_HSTL_II_18	1.09	1.09	1.81	1.81	1.81	1.81	ns
DIFF_HSTL_II_DCI_18	1.09	1.09	1.62	1.62	1.62	1.62	ns
DIFF_HSTL_II _T_DCI_18	1.09	1.09	1.68	1.68	1.68	1.68	ns
DIFF_HSTL_II	1.09	1.09	1.74	1.74	1.74	1.74	ns
DIFF_HSTL_II_DCI	1.09	1.09	1.68	1.68	1.68	1.68	ns
SSTL2_I_DCI	1.06	1.06	1.70	1.70	1.70	1.70	ns
SSTL2_II_DCI	1.06	1.06	1.67	1.67	1.67	1.67	ns
SSTL2_II_T_DCI	1.06	1.06	1.70	1.70	1.70	1.70	ns
SSTL18_I	1.06	1.06	1.75	1.75	1.75	1.75	ns
SSTL18_II	1.06	1.06	1.67	1.67	1.67	1.67	ns
SSTL18_I_DCI	1.06	1.06	1.67	1.67	1.67	1.67	ns
SSTL18_II_DCI	1.06	1.06	1.63	1.63	1.63	1.63	ns
SSTL18_II_T_DCI	1.06	1.06	1.67	1.67	1.67	1.67	ns
SSTL15_T_DCI	1.06	1.06	1.68	1.68	1.68	1.68	ns
SSTL15_DCI	1.06	1.06	1.68	1.68	1.68	1.68	ns
DIFF_SSTL2_I	1.09	1.09	1.77	1.77	1.77	1.77	ns
DIFF_SSTL2_I_DCI	1.09	1.09	1.70	1.70	1.70	1.70	ns
DIFF_SSTL2_II	1.09	1.09	1.72	1.72	1.72	1.72	ns
DIFF_SSTL2_II_DCI	1.09	1.09	1.67	1.67	1.67	1.67	ns
DIFF_SSTL2_II_T_DCI	1.09	1.09	1.70	1.70	1.70	1.70	ns
DIFF_SSTL18_I	1.09	1.09	1.75	1.75	1.75	1.75	ns
DIFF_SSTL18_I_DCI	1.09	1.09	1.67	1.67	1.67	1.67	ns
DIFF_SSTL18_II	1.09	1.09	1.67	1.67	1.67	1.67	ns
DIFF_SSTL18_II_DCI	1.09	1.09	1.63	1.63	1.63	1.63	ns

Output Delay Measurements

Output delays are measured using a Tektronix P6245 TDS500/600 probe (< 1 pF) across approximately 4" of FR4 microstrip trace. Standard termination was used for all testing. The propagation delay of the 4" trace is characterized separately and subtracted from the final measurement, and is therefore not included in the generalized test setups shown in Figure 14 and Figure 15.

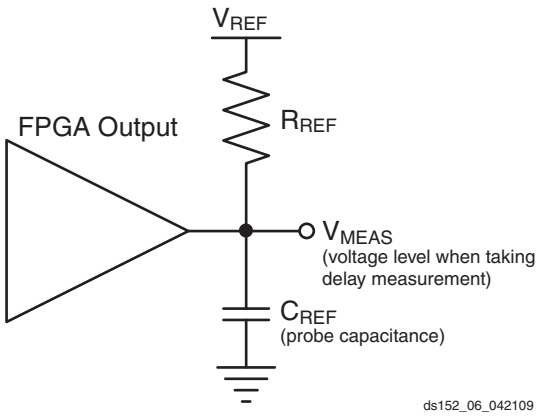

Figure 14: **Single Ended Test Setup**

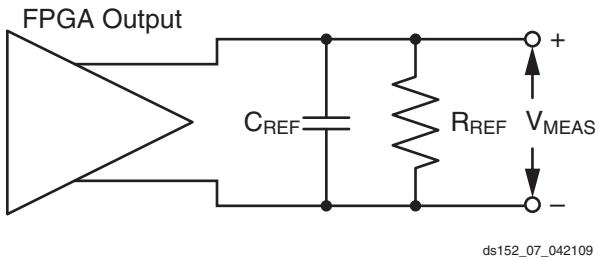

Figure 15: **Differential Test Setup**

Measurements and test conditions are reflected in the IBIS models except where the IBIS format precludes it. Parameters V_{REF}, R_{REF}, C_{REF}, and V_{MEAS} fully describe the test conditions for each I/O standard. The most accurate prediction of propagation delay in any given application can be obtained through IBIS simulation, using the following method:

1. Simulate the output driver of choice into the generalized test setup, using values from Table 41.
2. Record the time to V_{MEAS}.
3. Simulate the output driver of choice into the actual PCB trace and load, using the appropriate IBIS model or capacitance value to represent the load.
4. Record the time to V_{MEAS}.
5. Compare the results of steps 2 and 4. The increase or decrease in delay yields the actual propagation delay of the PCB trace.

Table 41: **Output Delay Measurement Methodology**

Description	I/O Standard Attribute	R_{REF} (Ω)	C_{REF} (1) (pF)	V_{MEAS} (V)	V_{REF} (V)
LVCMOS, 2.5V	LVCMOS25	1M	0	1.25	0
LVCMOS, 1.8V	LVCMOS18	1M	0	0.9	0
LVCMOS, 1.5V	LVCMOS15	1M	0	0.75	0
LVCMOS, 1.2V	LVCMOS12	1M	0	0.75	0
HSTL (High-Speed Transceiver Logic), Class I	HSTL_I	50	0	V_{REF}	0.75
HSTL, Class II	HSTL_II	25	0	V_{REF}	0.75
HSTL, Class III	HSTL_III	50	0	0.9	1.5
HSTL, Class I, 1.8V	HSTL_I_18	50	0	V_{REF}	0.9
HSTL, Class II, 1.8V	HSTL_II_18	25	0	V_{REF}	0.9
HSTL, Class III, 1.8V	HSTL_III_18	50	0	1.1	1.8
SSTL (Stub Series Terminated Logic), Class I, 1.8V	SSTL18_I	50	0	V_{REF}	0.9
SSTL, Class II, 1.8V	SSTL18_II	25	0	V_{REF}	0.9
SSTL, Class I, 2.5V	SSTL2_I	50	0	V_{REF}	1.25
SSTL, Class II, 2.5V	SSTL2_II	25	0	V_{REF}	1.25
LVDS (Low-Voltage Differential Signaling), 2.5V	LVDS_25	100	0	0 (2)	1.2
LVDSEXT (LVDS Extended Mode), 2.5V	LVDS_25	100	0	0 (2)	1.2
BLVDS (Bus LVDS), 2.5V	BLVDS_25	100	0	0 (2)	0

Table 43: **OLOGIC Switching Characteristics**

Symbol	Description	Speed Grade		Units
		-2	-1	
Setup/Hold				
T_{ODCK}/T_{OCKD}	D1/D2 pins Setup/Hold with respect to CLK	0.54/–0.11	0.54/–0.11	ns
T_{OOCECK}/T_{OCKOCE}	OCE pin Setup/Hold with respect to CLK	0.22/–0.05	0.22/–0.05	ns
T_{OSRCK}/T_{OCKSR}	SR pin Setup/Hold with respect to CLK	0.71/–0.29	0.71/–0.29	ns
T_{OTCK}/T_{OCKT}	T1/T2 pins Setup/Hold with respect to CLK	0.56/–0.10	0.56/–0.10	ns
T_{OTCECK}/T_{OCKTCE}	TCE pin Setup/Hold with respect to CLK	0.21/–0.05	0.21/–0.05	ns
Combinatorial				
T_{DOQ}	D1 to OQ out or T1 to TQ out	1.01	1.01	ns
Sequential Delays				
T_{OCKQ}	CLK to OQ/TQ out	0.71	0.71	ns
T_{RQ}	SR pin to OQ/TQ out	1.05	1.05	ns
T_{GSRQ}	Global Set/Reset to Q outputs	10.51	10.51	ns
Set/Reset				
T_{RPW}	Minimum Pulse Width, SR inputs	1.20	1.20	ns, Min

Input Serializer/Deserializer Switching Characteristics

Table 44: **ISERDES Switching Characteristics**

Symbol	Description	Speed Grade		Units
		-2	-1	
Setup/Hold for Control Lines				
$T_{ISCCK\_BITSLIP}/T_{ISCKC\_BITSLIP}$	BITSLIP pin Setup/Hold with respect to CLKDIV	0.09/0.17	0.09/0.17	ns
$T_{ISCCK\_CE}/T_{ISCKC\_CE}$ (2)	CE pin Setup/Hold with respect to CLK (for CE1)	0.27/0.04	0.27/0.04	ns
$T_{ISCCK\_CE2}/T_{ISCKC\_CE2}$ (2)	CE pin Setup/Hold with respect to CLKDIV (for CE2)	–0.06/0.31	–0.06/0.31	ns
Setup/Hold for Data Lines				
T_{ISDCK_D}/T_{ISCKD_D}	D pin Setup/Hold with respect to CLK	0.09/0.11	0.09/0.11	ns
$T_{ISDCK\_DDLY}/T_{ISCKD\_DDLY}$	DDLY pin Setup/Hold with respect to CLK (using IODELAY) (1)	0.14/0.07	0.14/0.07	ns
$T_{ISDCK\_D\_DDR}/T_{ISCKD\_D\_DDR}$	D pin Setup/Hold with respect to CLK at DDR mode	0.09/0.11	0.09/0.11	ns
$T_{ISDCK\_DDLY\_DDR}$ $T_{ISCKD\_DDLY\_DDR}$	D pin Setup/Hold with respect to CLK at DDR mode (using IODELAY) (1)	0.14/0.07	0.14/0.07	ns
Sequential Delays				
T_{ISCKO_Q}	CLKDIV to out at Q pin	0.75	0.75	ns
Propagation Delays				
T_{ISDO_DO}	D input to DO output pin	0.25	0.25	ns

Notes:

1. Recorded at 0 tap value.
2. T_{ISCCK_CE2} and T_{ISCKC_CE2} are reported as $T_{ISCCK\_CE}/T_{ISCKC\_CE}$ in a TRACE report.

Output Serializer/Deserializer Switching Characteristics

Table 45: **OSERDES Switching Characteristics**

Symbol	Description	Speed Grade		Units
		-2	-1	
Setup/Hold				
T_{OSDCK_D}/T_{OSCKD_D}	D input Setup/Hold with respect to CLKDIV	0.31/–0.12	0.31/–0.12	ns
T_{OSDCK_T}/T_{OSCKD_T}(1)	T input Setup/Hold with respect to CLK	0.56/–0.08	0.56/–0.08	ns
$T_{OSDCK\_T2}/T_{OSCKD\_T2}$(1)	T input Setup/Hold with respect to CLKDIV	0.31/–0.08	0.31/–0.08	ns
$T_{OSCCK\_OCE}/T_{OSCKC\_OCE}$	OCE input Setup/Hold with respect to CLK	0.22/–0.05	0.22/–0.05	ns
T_{OSCCK_S}	SR (Reset) input Setup with respect to CLKDIV	0.07	0.07	ns
$T_{OSCCK\_TCE}/T_{OSCKC\_TCE}$	TCE input Setup/Hold with respect to CLK	0.21/–0.05	0.21/–0.05	ns
Sequential Delays				
T_{OSCKO_OQ}	Clock to out from CLK to OQ	0.82	0.82	ns
T_{OSCKO_TQ}	Clock to out from CLK to TQ	0.82	0.82	ns
Combinatorial				
T_{OSDO_TTQ}	T input to TQ Out	0.97	0.97	ns

Notes:

1. T_{OSDCK_T2} and T_{OSCKD_T2} are reported as T_{OSDCK_T}/T_{OSCKD_T} in the TRACE report.

Table 47: **CLB Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade		Units
		-2	-1	
T_{BXB}	BX inputs to BMUX output	0.39	0.45	ns, Max
T_{BXD}	BX inputs to DMUX output	0.50	0.58	ns, Max
T_{CXB}	CX inputs to CMUX output	0.34	0.38	ns, Max
T_{CXD}	CX inputs to DMUX output	0.40	0.45	ns, Max
T_{DXD}	DX inputs to DMUX output	0.38	0.44	ns, Max
T_{OPCYA}	An input to COUT output	0.42	0.47	ns, Max
T_{OPCYB}	Bn input to COUT output	0.42	0.47	ns, Max
T_{OPCYC}	Cn input to COUT output	0.35	0.39	ns, Max
T_{OPCYD}	Dn input to COUT output	0.33	0.37	ns, Max
T_{AXCY}	AX input to COUT output	0.33	0.38	ns, Max
T_{BXCY}	BX input to COUT output	0.28	0.32	ns, Max
T_{CXCY}	CX input to COUT output	0.20	0.23	ns, Max
T_{DXCY}	DX input to COUT output	0.19	0.22	ns, Max
T_{BYP}	CIN input to COUT output	0.08	0.09	ns, Max
T_{CINA}	CIN input to AMUX output	0.28	0.32	ns, Max
T_{CINB}	CIN input to BMUX output	0.29	0.34	ns, Max
T_{CINC}	CIN input to CMUX output	0.30	0.34	ns, Max
T_{CIND}	CIN input to DMUX output	0.33	0.38	ns, Max
Sequential Delays				
T_{CKO}	Clock to AQ – DQ outputs	0.39	0.44	ns, Max
T_{SHCKO}	Clock to AMUX – DMUX outputs	0.47	0.54	ns, Max
Setup and Hold Times of CLB Flip-Flops Before/After Clock CLK				
T_{DICK}/T_{CKDI}	A – D input to CLK on A – D Flip Flops	0.43/0.20	0.50/0.23	ns, Min
$T_{CECK\_CLB}/T_{CKCE\_CLB}$	CE input to CLK on A – D Flip Flops	0.32/–0.01	0.37/–0.01	ns, Min
T_{SRCK}/T_{CKSR}	SR input to CLK on A – D Flip Flops	0.52/–0.08	0.60/–0.08	ns, Min
T_{CINCK}/T_{CKCIN}	CIN input to CLK on A – D Flip Flops	0.24/0.17	0.27/0.19	ns, Min
Set/Reset				
T_{SRMIN}	SR input minimum pulse width	0.97	0.97	ns, Min
T_{RQ}	Delay from SR input to AQ – DQ flip-flops	0.68	0.78	ns, Max
T_{CEO}	Delay from CE input to AQ – DQ flip-flops	0.59	0.67	ns, Max
F_{TOG}	Toggle frequency (for export control)	1098.00	1098.00	MHz

Notes:

1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.
2. These items are of interest for Carry Chain applications.

Block RAM and FIFO Switching Characteristics

Table 50: **Block RAM and FIFO Switching Characteristics**

Symbol	Description	Speed Grade		Units
		-2	-1	
Block RAM and FIFO Clock-to-Out Delays				
T_{RCKO_DO} and $T_{RCKO\_DO\_REG}$[1]	Clock CLK to DOUT output (without output register)[2][3]	2.08	2.39	ns, Max
	Clock CLK to DOUT output (with output register)[4][5]	0.75	0.86	ns, Max
$T_{RCKO\_DO\_ECC}$ and $T_{RCKO\_DO\_ECC\_REG}$	Clock CLK to DOUT output with ECC (without output register)[2][3]	3.30	3.79	ns, Max
	Clock CLK to DOUT output with ECC (with output register)[4][5]	0.86	0.98	ns, Max
T_{RCKO_CASC} and $T_{RCKO\_CASC\_REG}$	Clock CLK to DOUT output with Cascade (without output register)[2]	3.18	3.65	ns, Max
	Clock CLK to DOUT output with Cascade (with output register)[4]	1.58	1.81	ns, Max
T_{RCKO_FLAGS}	Clock CLK to FIFO flags outputs[6]	0.91	1.05	ns, Max
$T_{RCKO\_POINTERS}$	Clock CLK to FIFO pointers outputs[7]	1.09	1.25	ns, Max
$T_{RCKO\_RDCOUNT}$	Clock CLK to FIFO Read Counter	1.09	1.25	ns, Max
$T_{RCKO\_WRCOUNT}$	Clock CLK to FIFO Write Counter	1.09	1.25	ns, Max
$T_{RCKO\_SDBIT\_ECC}$ and $T_{RCKO\_SDBIT\_ECC\_REG}$	Clock CLK to BITERR (with output register)	0.76	0.87	ns, Max
	Clock CLK to BITERR (without output register)	2.84	3.26	ns, Max
$T_{RCKO\_PARITY\_ECC}$	Clock CLK to ECCPARITY in ECC encode only mode	1.06	1.21	ns, Max
$T_{RCKO\_RDADDR\_ECC}$ and $T_{RCKO\_RDADDR\_ECC\_REG}$	Clock CLK to RDADDR output with ECC (without output register)	0.90	1.03	ns, Max
	Clock CLK to RDADDR output with ECC (with output register)	0.92	1.06	ns, Max
Setup and Hold Times Before/After Clock CLK				
$T_{RCCK\_ADDR}/T_{RCKC\_ADDR}$	ADDR inputs[8]	0.62/0.32	0.72/0.37	ns, Min
T_{RDCK_DI}/T_{RCKD_DI}	DIN inputs[9]	1.11/0.34	1.28/0.39	ns, Min
$T_{RDCK\_DI\_ECC}/T_{RCKD\_DI\_ECC}$	DIN inputs with block RAM ECC in standard mode[9]	0.59/0.34	0.68/0.39	ns, Min
	DIN inputs with block RAM ECC encode only[9]	0.85/0.34	0.97/0.39	ns, Min
	DIN inputs with FIFO ECC in standard mode[9]	1.02/0.34	1.17/0.39	ns, Min
$T_{RCCK\_CLK}/T_{RCKC\_CLK}$	Inject single/double bit error in ECC mode	1.20/0.29	1.38/0.33	ns, Min
$T_{RCCK\_RDEN}/T_{RCKC\_RDEN}$	Block RAM Enable (EN) input	0.41/0.30	0.47/0.34	ns, Min
$T_{RCCK\_REGCE}/T_{RCKC\_REGCE}$	CE input of output register	0.22/0.31	0.25/0.35	ns, Min
$T_{RCCK\_RSTREG}/T_{RCKC\_RSTREG}$	Synchronous RSTREG input	0.28/0.26	0.32/0.29	ns, Min
$T_{RCCK\_RSTRAM}/T_{RCKC\_RSTRAM}$	Synchronous RSTRAM input	0.41/0.27	0.47/0.31	ns, Min
T_{RCCK_WE}/T_{RCKC_WE}	Write Enable (WE) input (block RAM only)	0.52/0.35	0.60/0.40	ns, Min
$T_{RCCK\_WREN}/T_{RCKC\_WREN}$	WREN FIFO inputs	0.55/0.30	0.64/0.34	ns, Min
$T_{RCCK\_RDEN}/T_{RCKC\_RDEN}$	RDEN FIFO inputs	0.55/0.30	0.63/0.34	ns, Min
Reset Delays				
T_{RCO_FLAGS}	Reset RST to FIFO Flags/Pointers[10]	1.10	1.27	ns, Max
$T_{RCCK\_RSTREG}/T_{RCKC\_RSTREG}$	FIFO reset timing[11]	0.28/0.26	0.32/0.29	ns, Min

Table 51: **DSP48E1 Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade		Units
		-2	-1	
Combinatorial Delays from Input Pins to Cascading Output Pins				
$T_{DSPDO\_\{A; B\}\_\{ACOUT; BCOUT\}}$	{A, B} input to {ACOUT, BCOUT} output	0.65	0.75	ns
$T_{DSPDO\_\{A, B\}\_\{PCOUT, CARRYCASCOUT, MULTSIGNOUT\}\_MULT}$	{A, B} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output using multiplier	5.24	6.03	ns
$T_{DSPDO\_D\_\{PCOUT, CARRYCASCOUT, MULTSIGNOUT\}\_MULT}$	D input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output using multiplier	4.94	5.68	ns
$T_{DSPDO\_\{A, B\}\_\{PCOUT, CARRYCASCOUT, MULTSIGNOUT\}}$	{A, B} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output not using multiplier	2.19	2.52	ns
$T_{DSPDO\_\_\{C, CARRYIN\}\_\{PCOUT, CARRYCASCOUT,MULTSIGNOUT\}}$	{C, CARRYIN} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output	1.95	2.25	ns
Combinatorial Delays from Cascading Input Pins to All Output Pins				
$T_{DSPDO\_\{ACIN, BCIN\}\_\{P, CARRYOUT\}\_MULT}$	{ACIN, BCIN} input to {P, CARRYOUT} output using multiplier	4.97	5.72	ns
$T_{DSPDO\_\{ACIN, BCIN\}\_\{P, CARRYOUT}$	{ACIN, BCIN} input to {P, CARRYOUT} output not using multiplier	1.92	2.21	ns
$T_{DSPDO\_\{ACIN; BCIN\}\_\{ACOUT; BCOUT\}}$	{ACIN, BCIN} input to {ACOUT, BCOUT} output	0.49	0.57	ns
$T_{DSPDO\_\{ACIN, BCIN\}\_\{PCOUT, CARRYCASCOUT, MULTSIGNOUT\}\_MULT}$	{ACIN, BCIN} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output using multiplier	5.10	5.86	ns
$T_{DSPDO\_\{ACIN, BCIN\}\_\{PCOUT, CARRYCASCOUT, MULTSIGNOUT\}}$	{ACIN, BCIN} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output not using multiplier	2.05	2.35	ns
$T_{DSPDO\_\{PCIN, CARRYCASCIN, MULTSIGNIN\}\_ \{P, CARRYOUT\}}$	{PCIN, CARRYCASCIN, MULTSIGNIN} input to {P, CARRYOUT} output	1.60	1.83	ns
$T_{DSPDO\_\{PCIN, CARRYCASCIN, MULTSIGNIN\}\_ \{PCOUT, CARRYCASCOUT, MULTSIGNOUT\}}$	{PCIN, CARRYCASCIN, MULTSIGNIN} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output	1.72	1.98	ns
Clock to Outs from Output Register Clock to Output Pins				
$T_{DSPCKO\_\{P, CARRYOUT\}\_PREG}$	CLK (PREG) to {P, CARRYOUT} output	0.50	0.57	ns
$T_{DSPCKO\_\{PCOUT, CARRYCASCOUT, MULTSIGNOUT\}\_PREG}$	CLK (PREG) to {CARRYCASCOUT, PCOUT, MULTSIGNOUT} output	0.50	0.66	ns
Clock to Outs from Pipeline Register Clock to Output Pins				
$T_{DSPCKO\_\{P, CARRYOUT\}\_MREG}$	CLK (MREG) to {P, CARRYOUT} output	2.30	2.65	ns
$T_{DSPCKO\_\{PCOUT, CARRYCASCOUT, MULTSIGNOUT\}\_MREG}$	CLK (MREG) to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output	2.43	2.79	ns
$T_{DSPCKO\_\{P, CARRYOUT\}\_ADREG\_MULT}$	CLK (ADREG) to {P, CARRYOUT} output	3.72	4.72	ns
$T_{DSPCKO\_\{PCOUT, CARRYCASCOUT, MULTSIGNOUT\}\_ADREG\_MULT}$	CLK (ADREG) to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output	3.84	4.42	ns
Clock to Outs from Input Register Clock to Output Pins				
$T_{DSPCKO\_\{P, CARRYOUT\}\_\{AREG, BREG\}\_MULT}$	CLK (AREG, BREG) to {P, CARRYOUT} output using multiplier	5.36	6.16	ns
$T_{DSPCKO\_\{P, CARRYOUT\}\_\{AREG, BREG\}}$	CLK (AREG, BREG) to {P, CARRYOUT} output not using multiplier	2.27	2.61	ns
$T_{DSPCKO\_\{P, CARRYOUT\}\_CREG}$	CLK (CREG) to {P, CARRYOUT} output	2.27	2.61	ns
$T_{DSPCKO\_\{P, CARRYOUT\}\_DREG\_MULT}$	CLK (DREG) to {P, CARRYOUT} output	5.25	6.04	ns

Configuration Switching Characteristics

Table 52: **Configuration Switching Characteristics**

Symbol	Description	Speed Grade		Units
		-2	-1	
Power-up Timing Characteristics				
T_{PL} (1)	Program Latency	3	3	ms, Max
T_{POR} (1)	Power-on-Reset	15/55	15/55	ms, Min/Max
T_{ICCK}	CCLK (output) delay	400	400	ns, Min
$T_{PROGRAM}$	Program Pulse Width	250	250	ns, Min
Master/Slave Serial Mode Programming Switching (1)				
T_{DCCK}/T_{CCKD}	DIN Setup/Hold, slave mode	4.0/0.0	4.0/0.0	ns, Min
T_{DSCCK}/T_{SCCKD}	DIN Setup/Hold, master mode	4.0/0.0	4.0/0.0	ns, Min
T_{CCO}	DOUT at 2.5V	6	6	ns, Max
	DOUT at 1.8V	6	6	ns, Max
F_{MCCK}	Maximum CCLK frequency, serial modes	100	100	MHz, Max
$F_{MCCKTOL}$	Frequency Tolerance, master mode with respect to nominal CCLK	55	55	%
F_{MSCCK}	Slave mode external CCLK	100	100	MHz
SelectMAP Mode Programming Switching				
T_{SMDCCK}/T_{SMCCKD}	SelectMAP Data Setup/Hold	4.0/0.0	4.0/0.0	ns, Min
$T_{SMCSCCK}/T_{SMCCKCS}$	CSI_B Setup/Hold	4.0/0.0	4.0/0.0	ns, Min
T_{SMCCKW}/T_{SMWCCK}	RDWR_B Setup/Hold	10.0/0.0	10.0/0.0	ns, Min
$T_{SMCKCSO}$	CSO_B clock to out (330 Ω pull-up resistor required)	7	7	ns, Min
T_{SMCO}	CCLK to DATA out in readback at 2.5V	8	8	ns, Max
	CCLK to DATA out in readback at 1.8V	8	8	ns, Max
T_{SMCKBY}	CCLK to BUSY out in readback at 2.5V	6	6	ns, Max
	CCLK to BUSY out in readback at 1.8V	6	6	ns, Max
F_{SMCCK}	Maximum Frequency with respect to nominal CCLK	100	100	MHz, Max
F_{RBCCK}	Maximum Readback Frequency with respect to nominal CCLK	100	100	MHz, Max
$F_{MCCKTOL}$	Frequency Tolerance with respect to nominal CCLK	55	55	%
Boundary-Scan Port Timing Specifications				
T_{TAPTCK}/T_{TCKTAP}	TMS and TDI Setup time before TCK/ Hold time after TCK	3.0/2.0	3.0/2.0	ns, Min
T_{TCKTDO}	TCK falling edge to TDO output valid at 2.5V	6	6	ns, Max
	TCK falling edge to TDO output valid at 1.8V	6	6	ns, Max
F_{TCK}	Maximum configuration TCK clock frequency	66	66	MHz, Max
F_{TCKB_MIN}	Minimum boundary-scan TCK clock frequency when using IEEE Std 1149.6 (AC-JTAG). Minimum operating temperature for IEEE Std 1149.6 is 0°C.	15	15	MHz, Min
F_{TCKB}	Maximum boundary-scan TCK clock frequency	66	66	MHz, Max

Clock Buffers and Networks

Table 53: **Global Clock Switching Characteristics (Including BUFGCTRL)**

Symbol	Description	Speed Grade		Units
		-2	-1	
$T_{BCCCK\_CE}/T_{BCCKC\_CE}$(1)	CE pins Setup/Hold	0.16/0.00	0.16/0.00	ns
T_{BCCCK_S}/T_{BCCKC_S}(1)	S pins Setup/Hold	0.16/0.00	0.16/0.00	ns
T_{BCCKO_O}(2)	BUFGCTRL delay from I0/I1 to O	0.10	0.10	ns
Maximum Frequency				
F_{MAX}	Global clock tree (BUFG)	700	700	MHz

Notes:

1. T_{BCCCK_CE} and T_{BCCKC_CE} must be satisfied to assure glitch-free operation of the global clock when switching between clocks. These parameters do not apply to the BUFGMUX_VIRTEX4 primitive that assures glitch-free operation. The other global clock setup and hold times are optional; only needing to be satisfied if device operation requires simulation matches on a cycle-for-cycle basis when switching between clocks.
2. T_{BGCKO_O} (BUFG delay from I0 to O) values are the same as T_{BCCKO_O} values.

Table 54: **Input/Output Clock Switching Characteristics (BUFIO)**

Symbol	Description	Speed Grade		Units
		-2	-1	
T_{BIOCKO_O}	Clock to out delay from I to O	0.18	0.18	ns
Maximum Frequency				
F_{MAX}	I/O clock tree (BUFIO)	710	710	MHz